APEC

EPC EFFICIENT POWER CONVERSION

Getting from 48 V to Load Voltage: Improving Low Voltage DC-DC Converter Performance with GaN Transistors

Alex Lidow

David Reusch

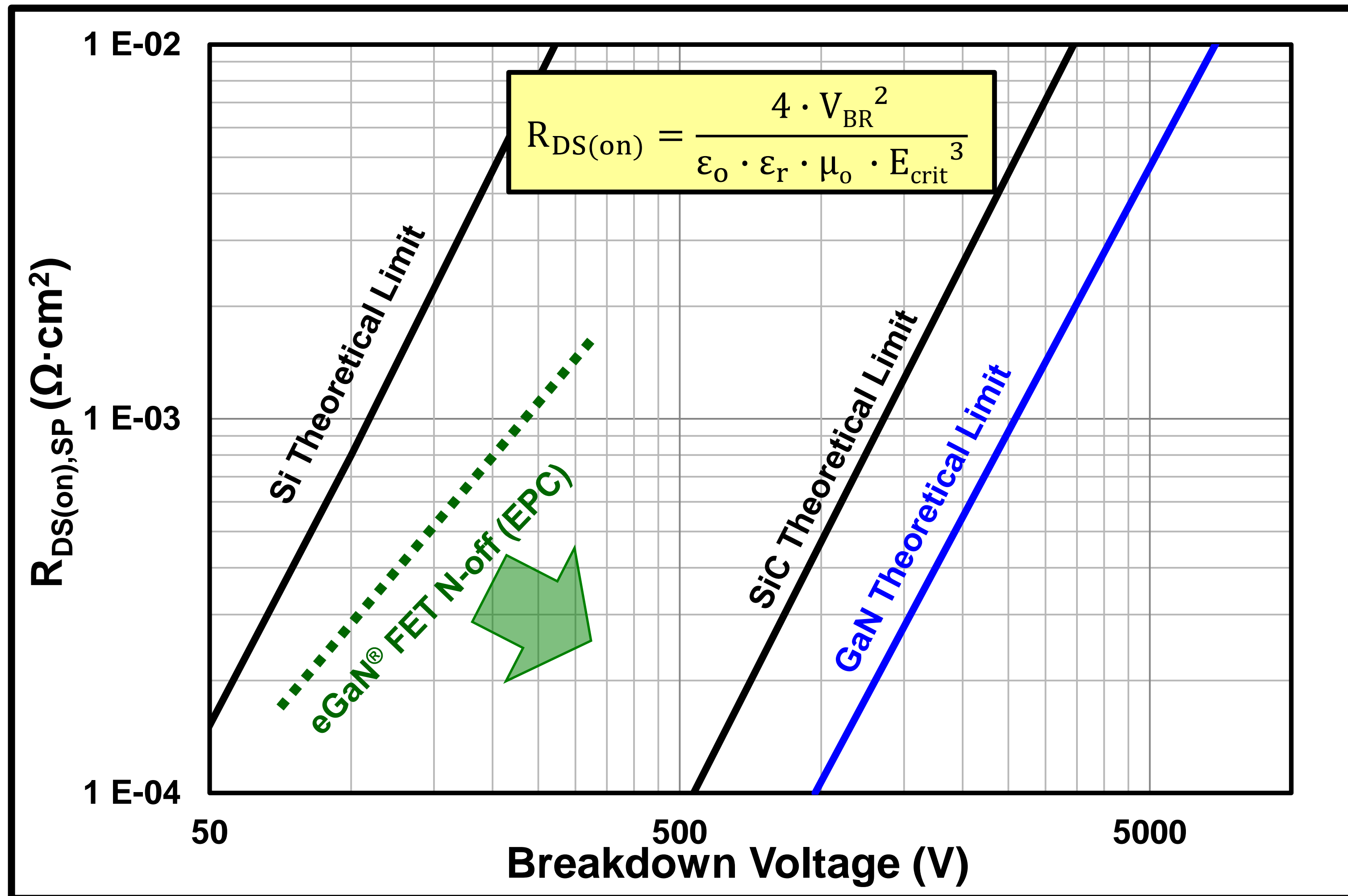
John Glaser

Agenda

- State of the Art in GaN
- Design Basics
- Design Examples
- What is in the Future?

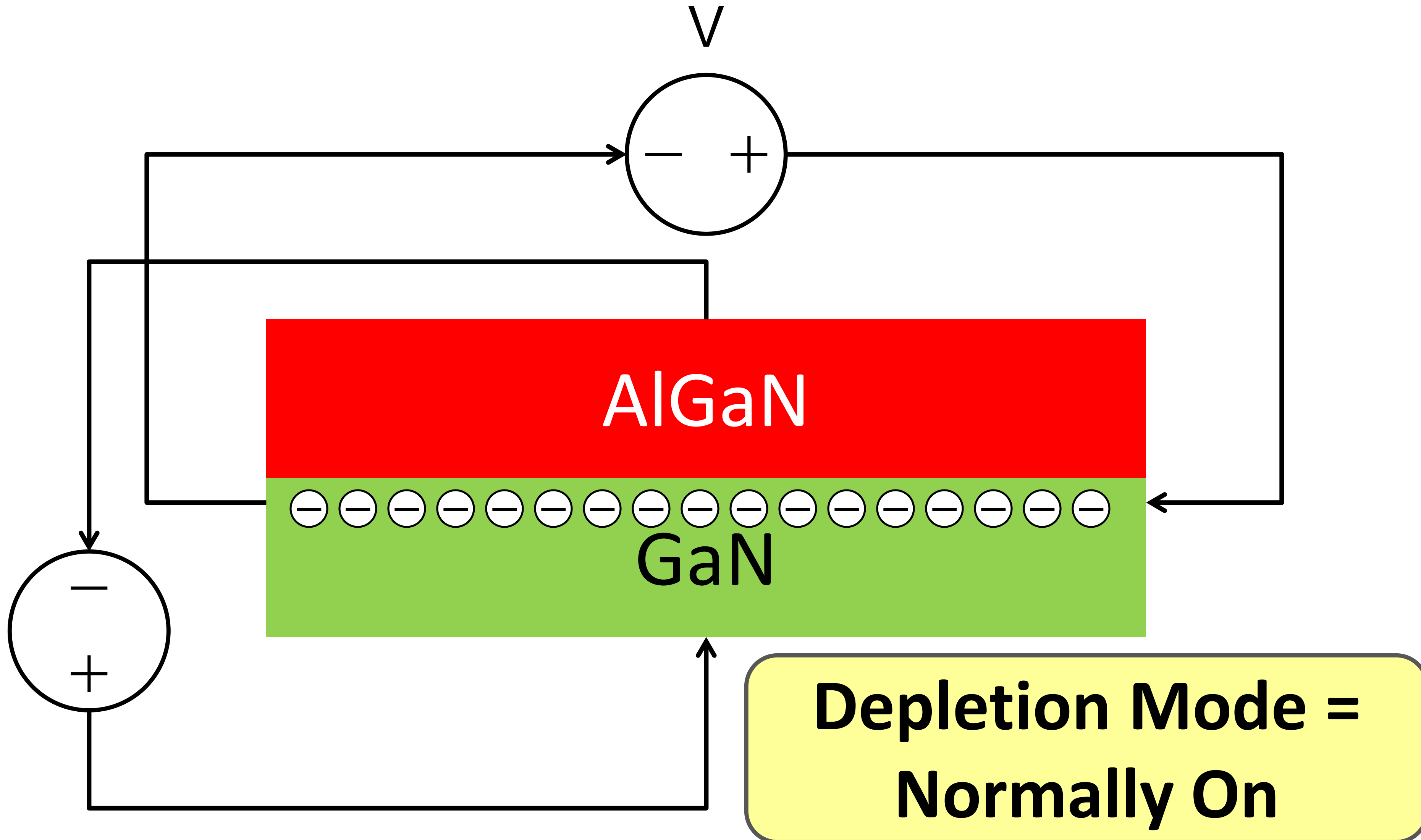
State of the Art

Why GaN

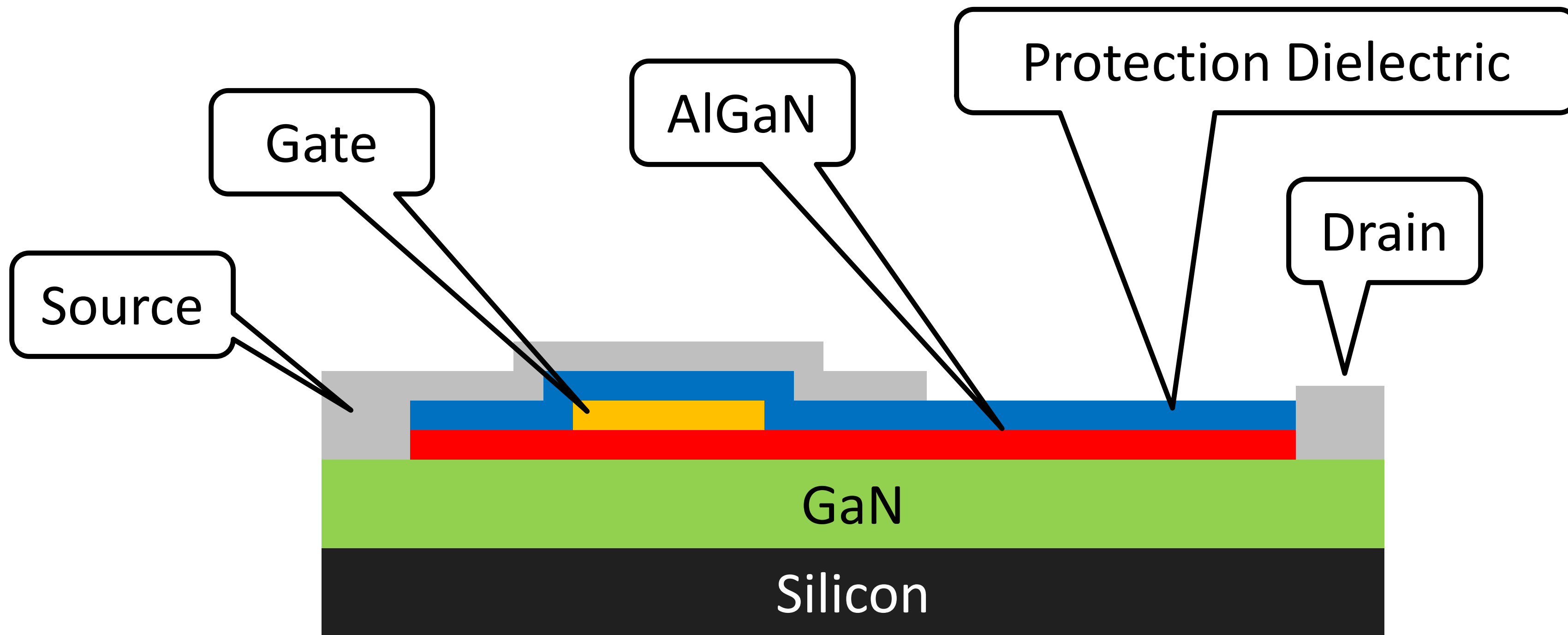


Theoretical Channel Resistance

GaN Switch

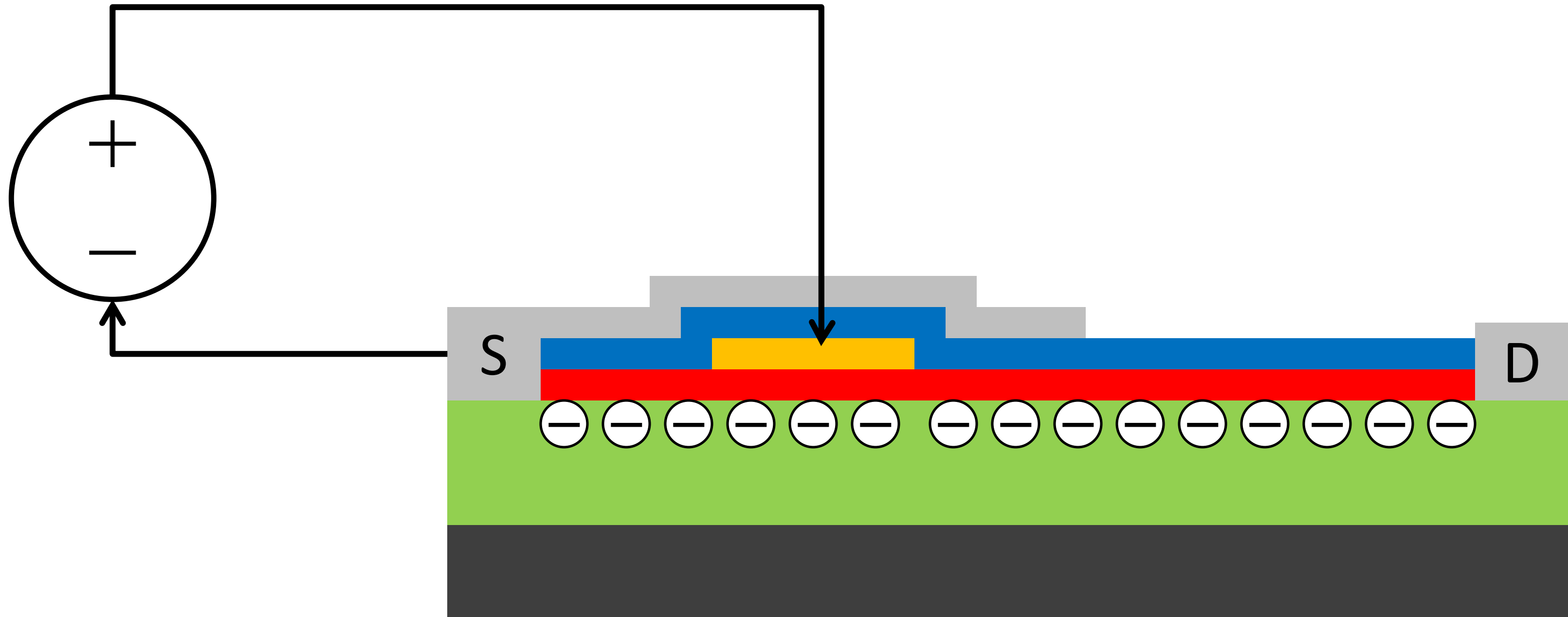


Device Construction Concept



Forms the foundation for a Depletion Mode device

Enhancement Mode – eGaN FET



A positive voltage from Gate-To-Source establishes an electron gas under the gate

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Cross Section of an eGaN® FET

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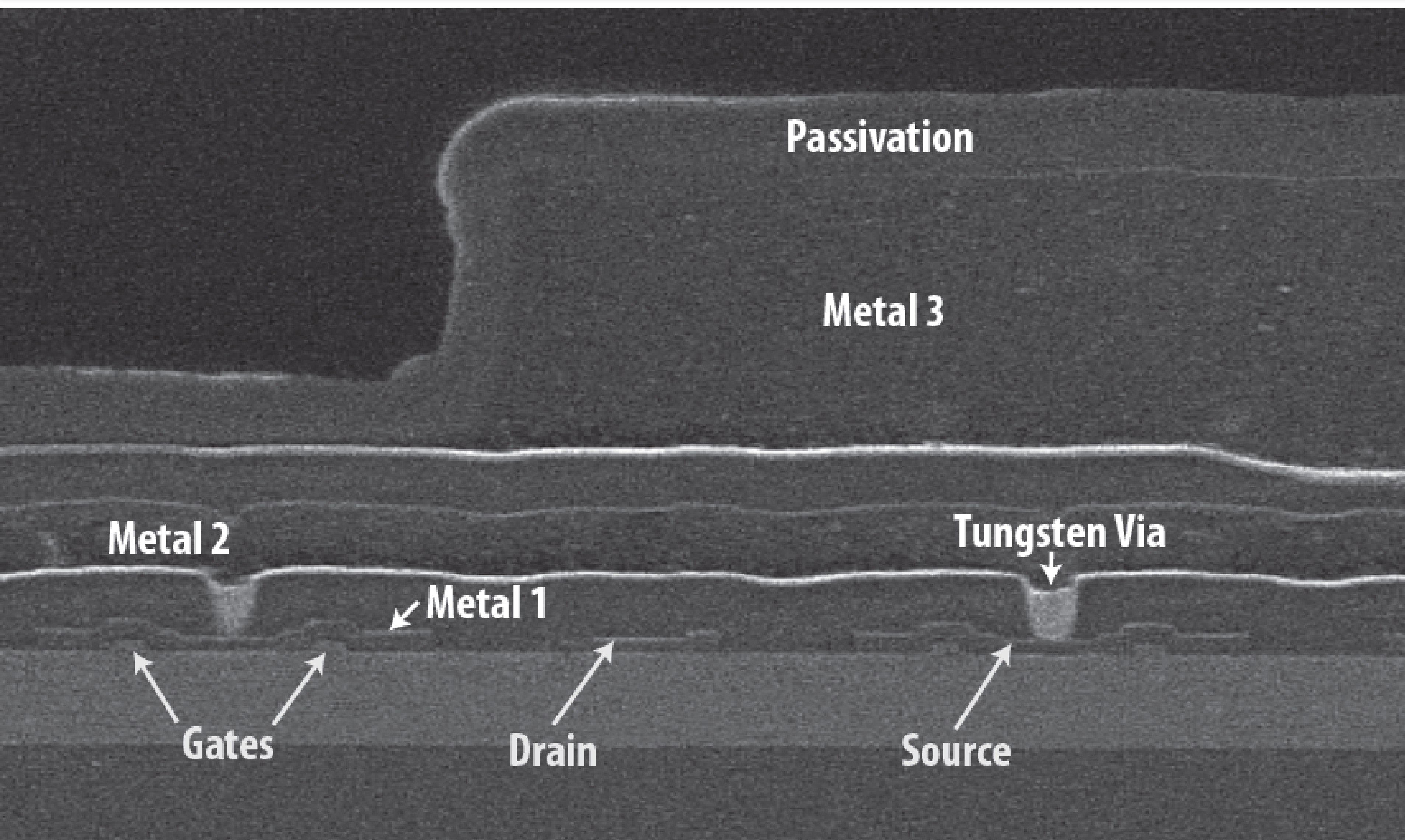
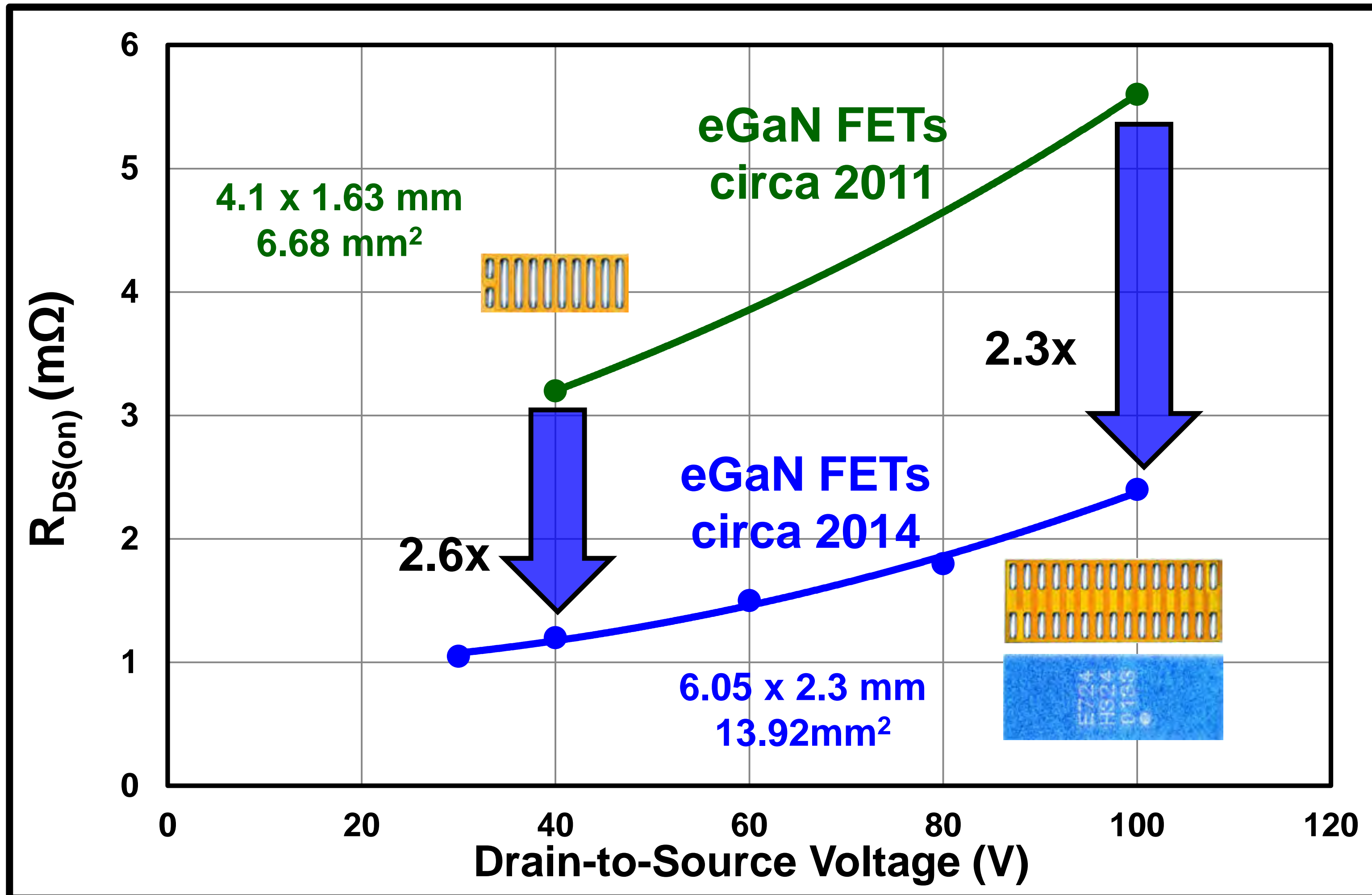


Power Device Wish List

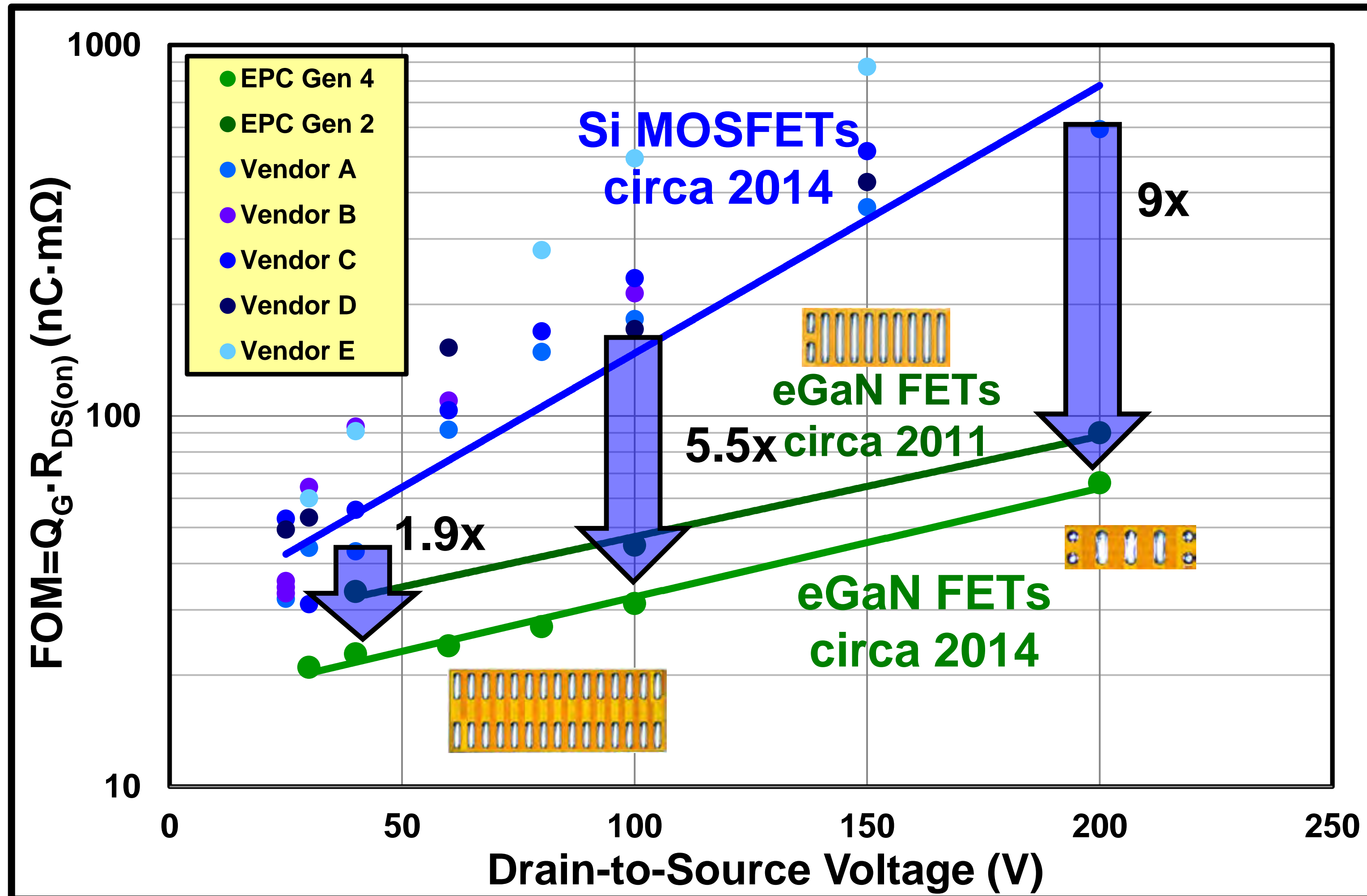
- Lower On Resistance
- Faster
- Smaller
- Lower Thermal Impedance
- Lower Cost

Lower On Resistance



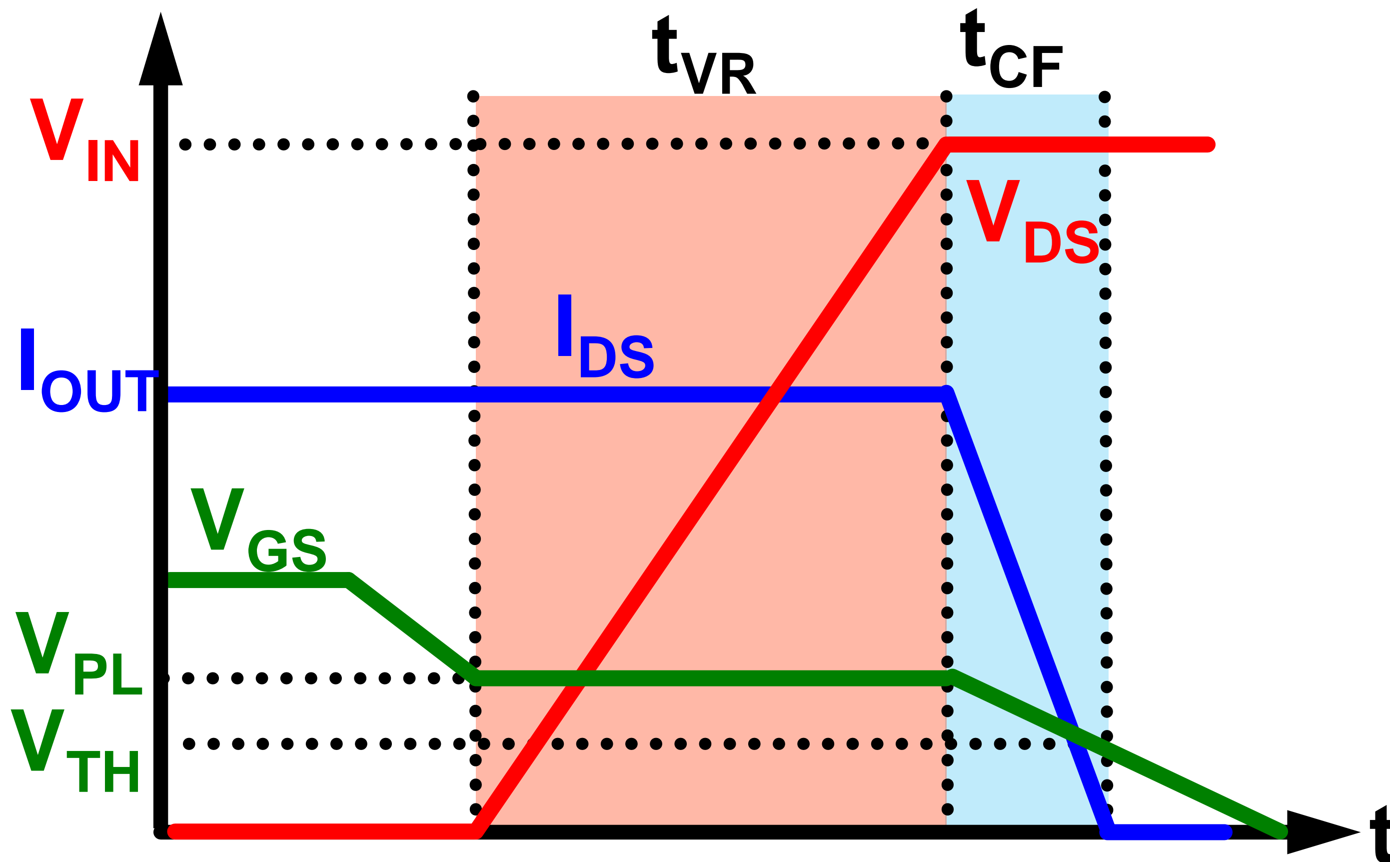
V_{GS}=5 V

Faster Switching



$V_{DS}=0.5 \cdot V_{DSS}$

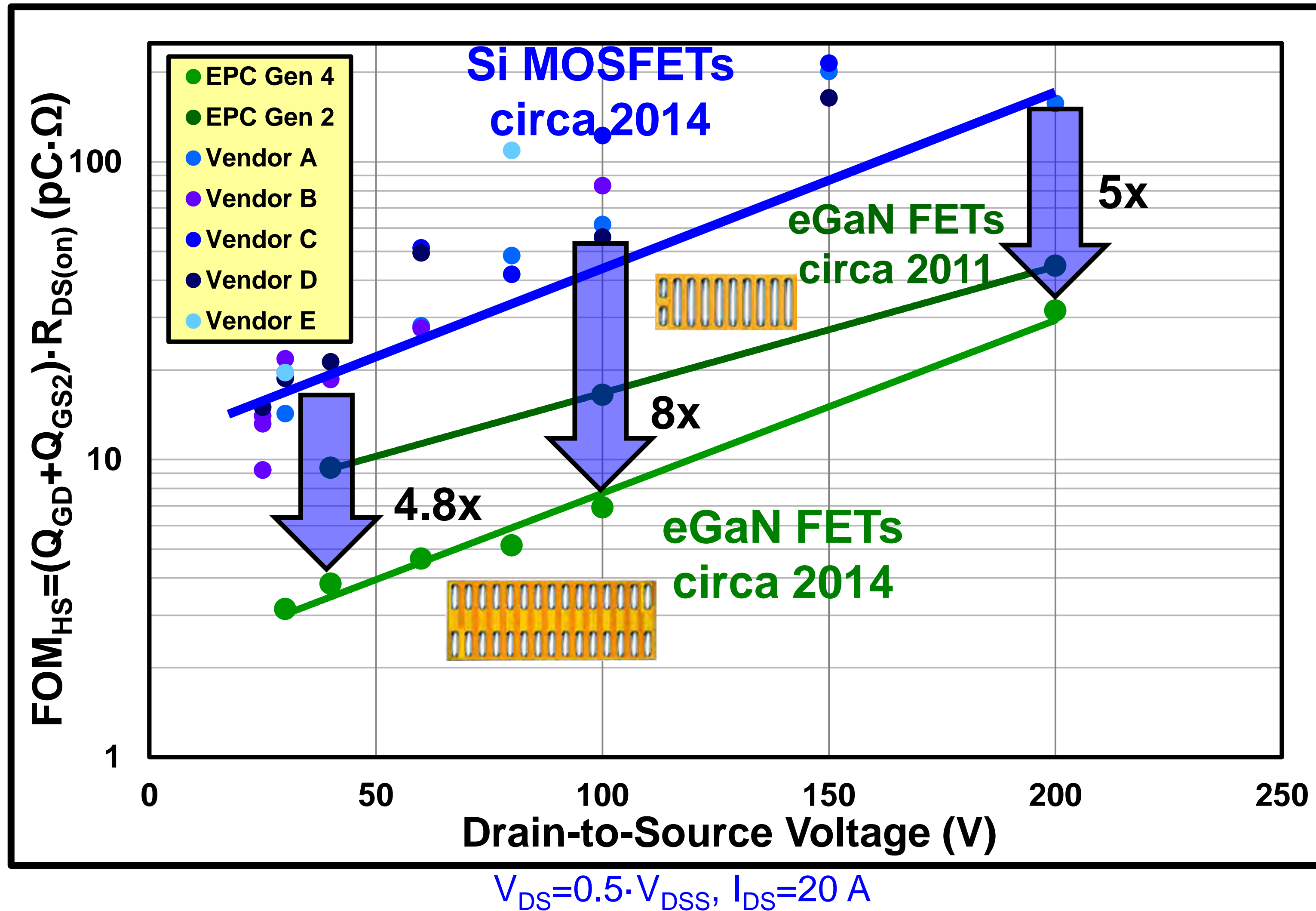
Ideal Hard Switching Turn Off



$$P_{t_{VR}} \approx \frac{V_{IN} \cdot I_{OUT} \cdot Q_{GD}}{2 \cdot I_G}$$

$$P_{t_{CF}} \approx \frac{V_{IN} \cdot I_{OUT} \cdot Q_{GS2}}{2 \cdot I_G}$$

Faster Switching



$V_{DS}=0.5 \cdot V_{DSS}$, $I_{DS}=20$ A

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High Speed Switching

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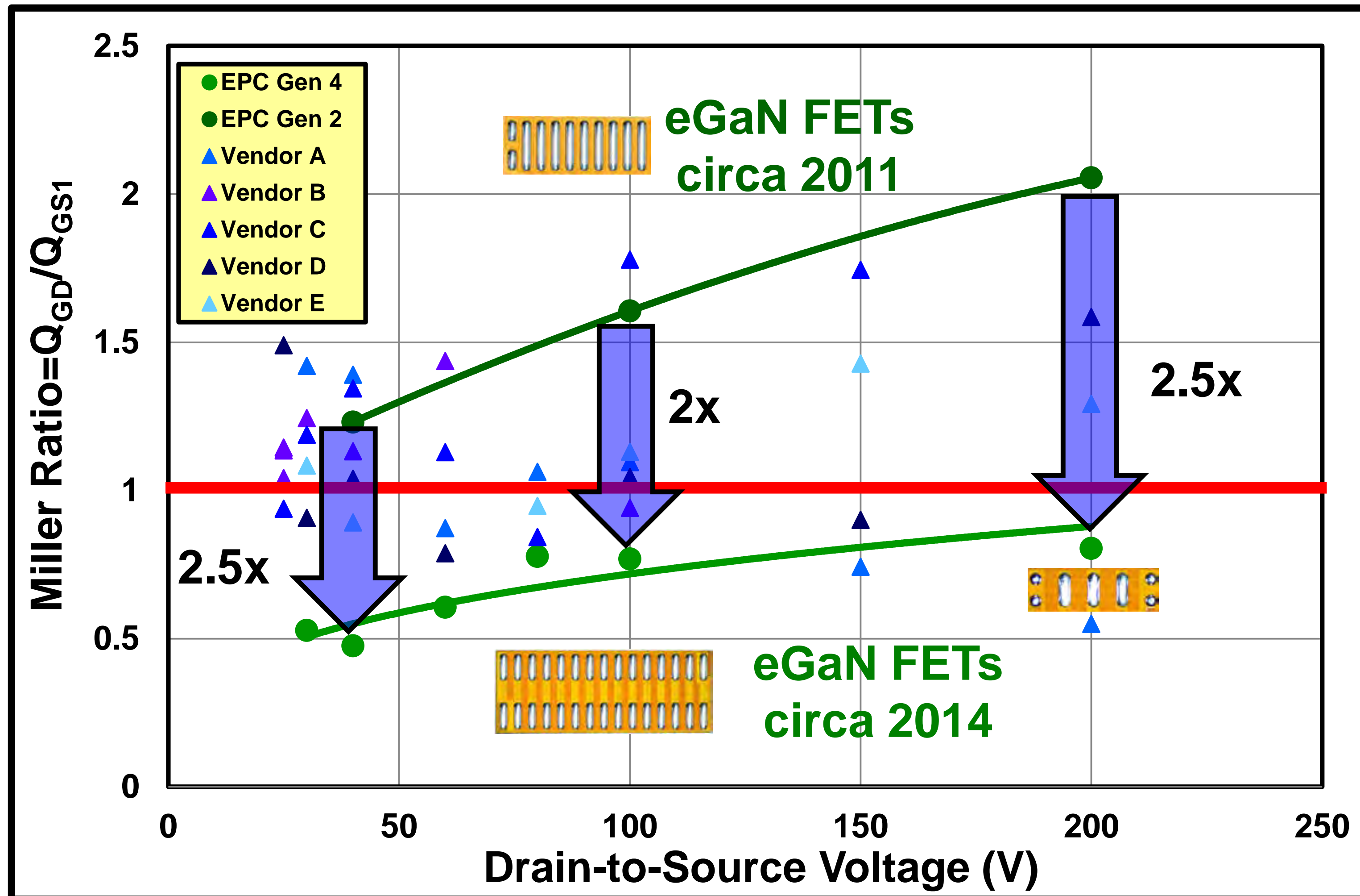
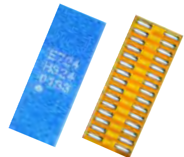


$V_{DS}=0.5 \cdot V_{DSS}$, $I_{DS}=20$ A

High Speed Switching



80 V eGaN FET
1.8 mΩ
13.9 mm²

$V_{DS_eGaN\ FET}$
$V_{GS_eGaN\ FET}$

80 V Si MOSFET
3.7 mΩ
31 mm²

V_{GS_MOSFET}
V_{DS_MOSFET}

V_{DS_MOSFET}

$V_{DS_eGaN\ FET}$

dv/dt bump

V_{DS} 10 V/Div   20 ns/ div V_{GS} 2 V/Div

File Edit Vertical Digital Horiz/Acq Trig Display Cursors Measure Mask Math MyScope Analyze Utilities Help Tek

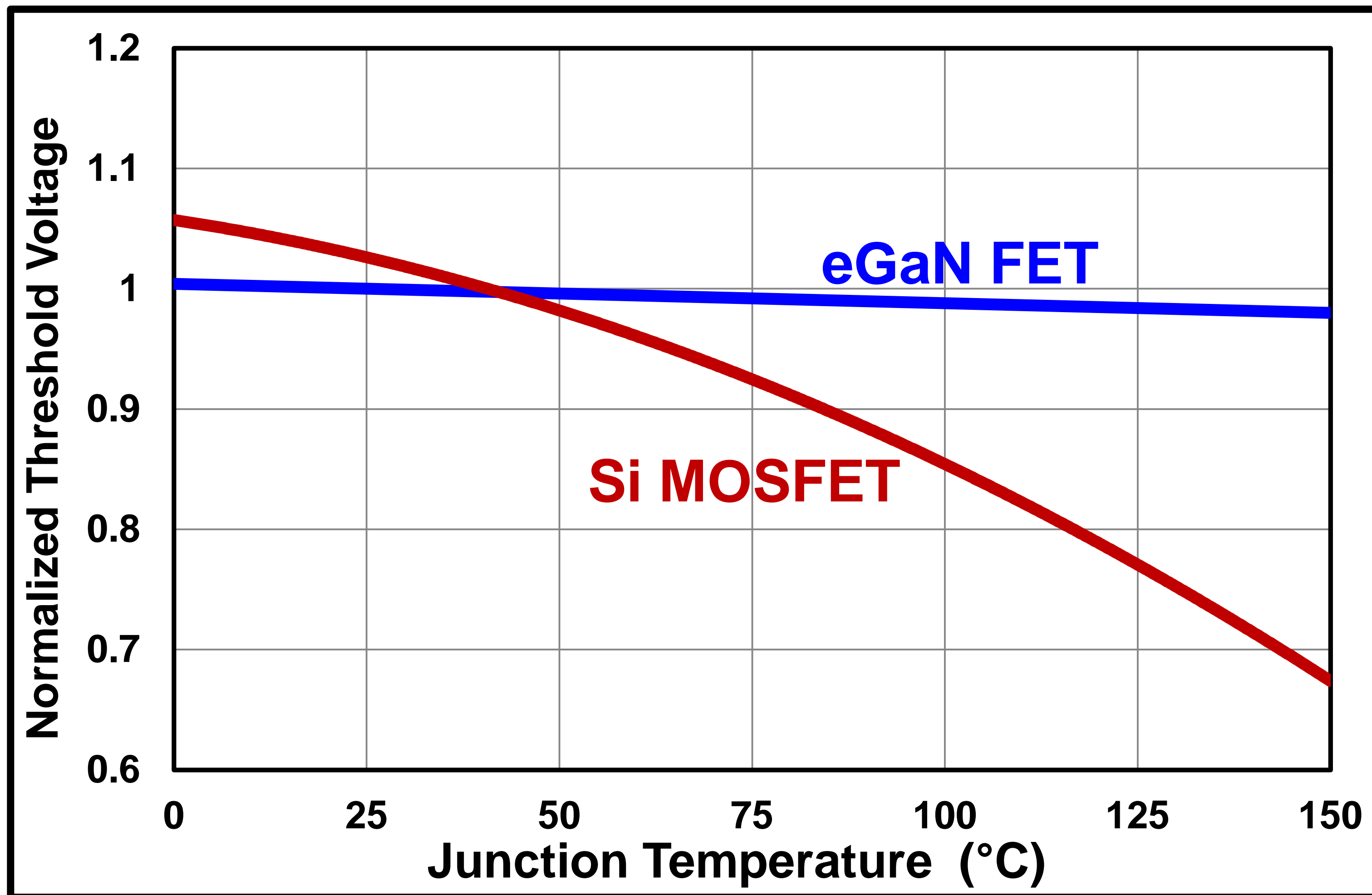
C1 10.0V/div B_W:500M
C2 2.0V/div 50Ω B_W:500M

A' C1 26.4V
None Auto

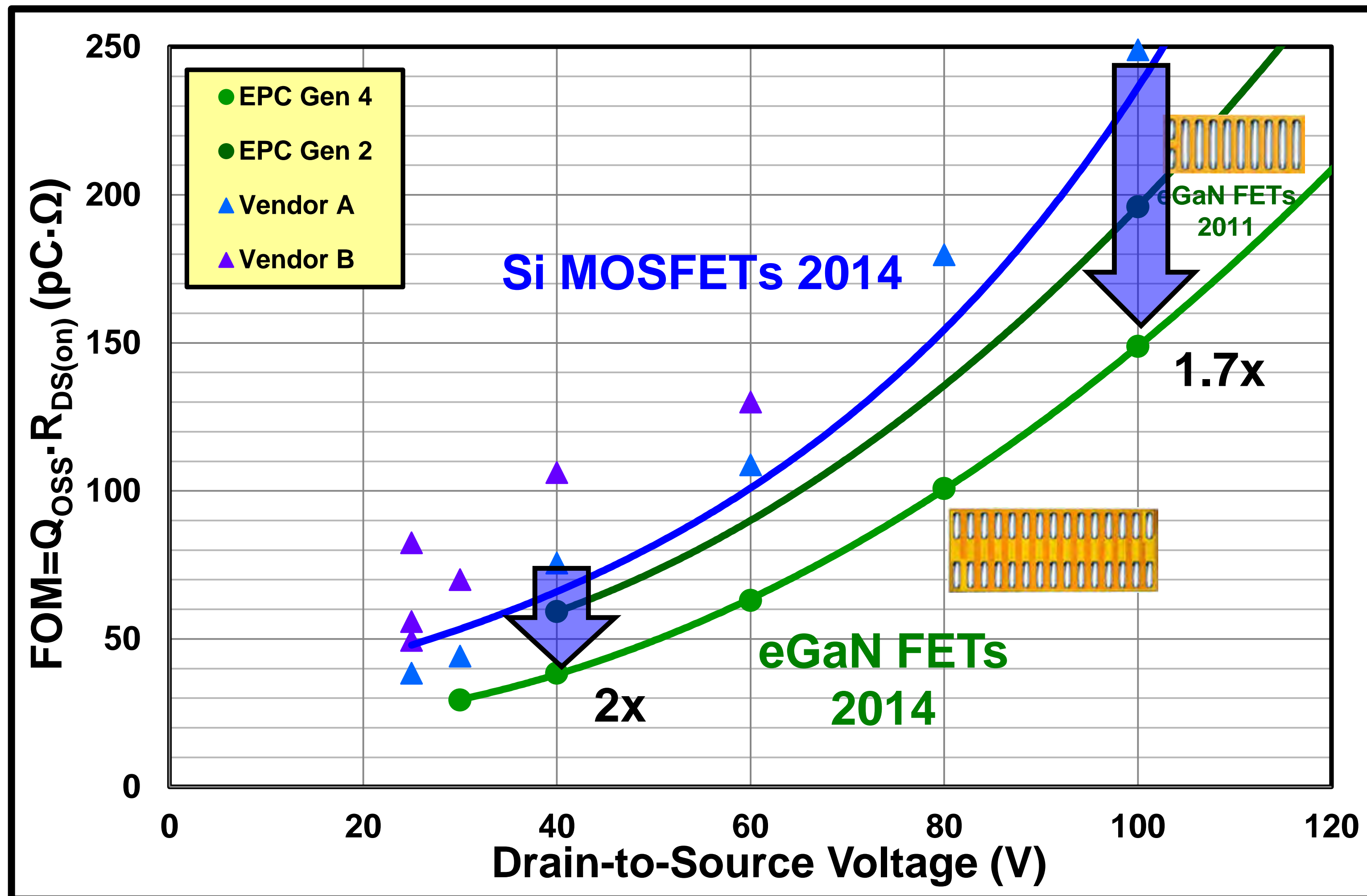
20.0ns/div 10.0GS/s 100ps/pt
Stopped
1 085 acqs RL:2.0k
Auto April 10, 2015 13:37:34

V_{IN}=48 V V_{OUT}=1 V I_{OUT}=30 A

Threshold vs. Temperature

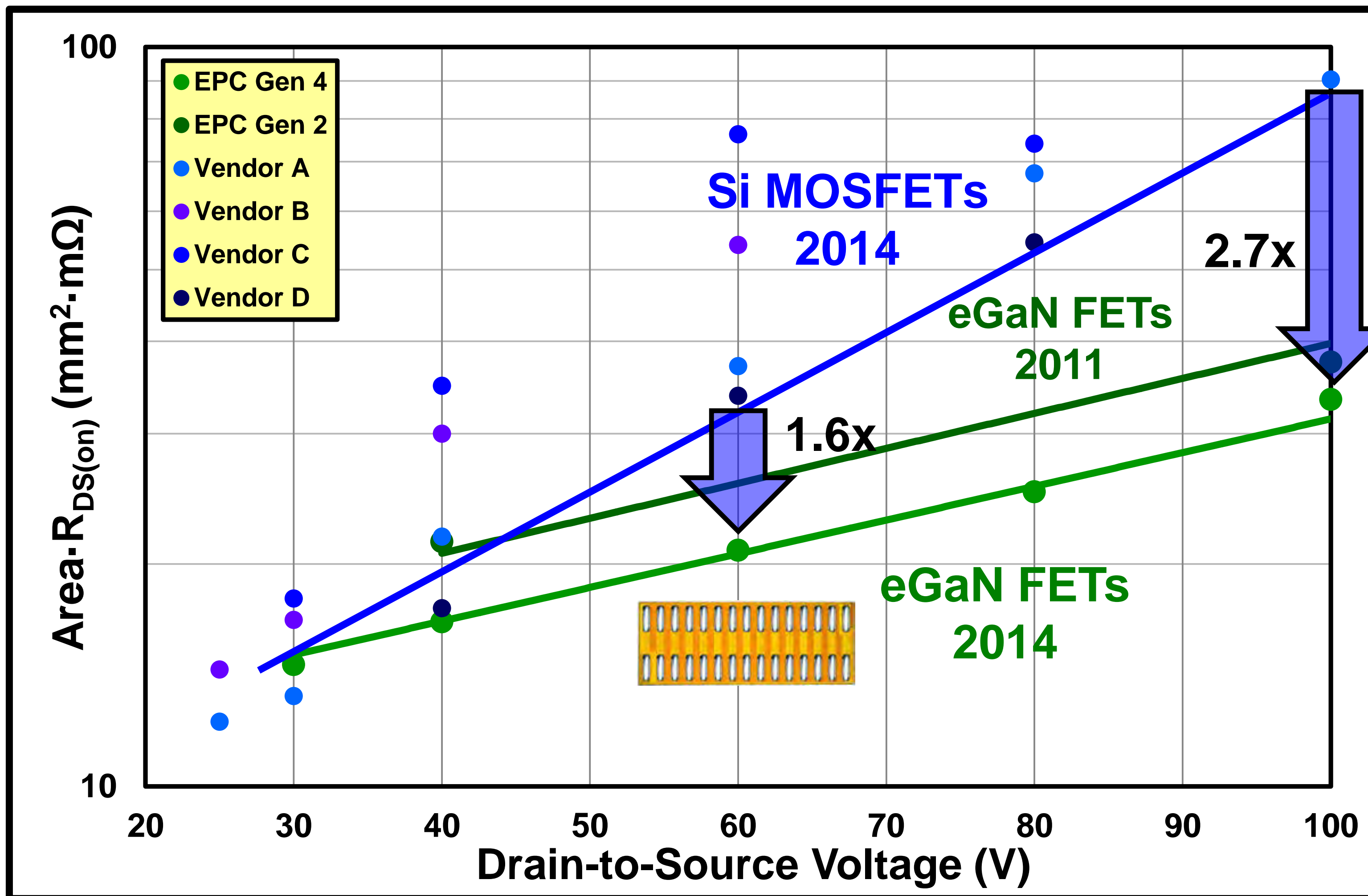


Lower Output Charge



$V_{DS}=0.5 \cdot V_{DSS}$

Smaller Size



Actual Product Resistance

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Thermal Management

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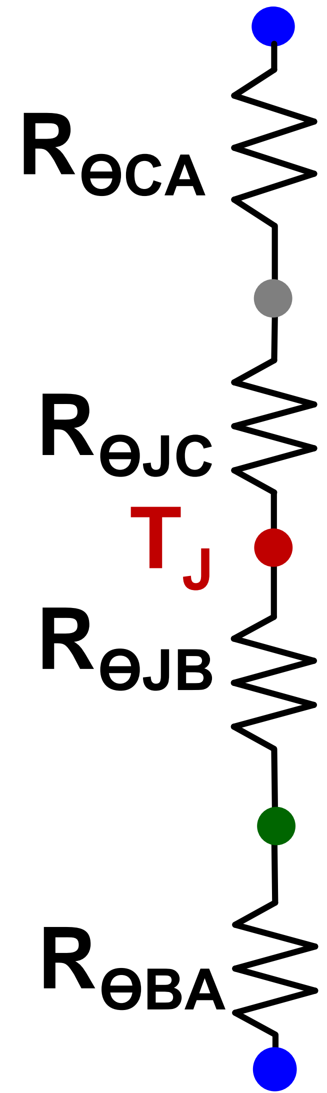
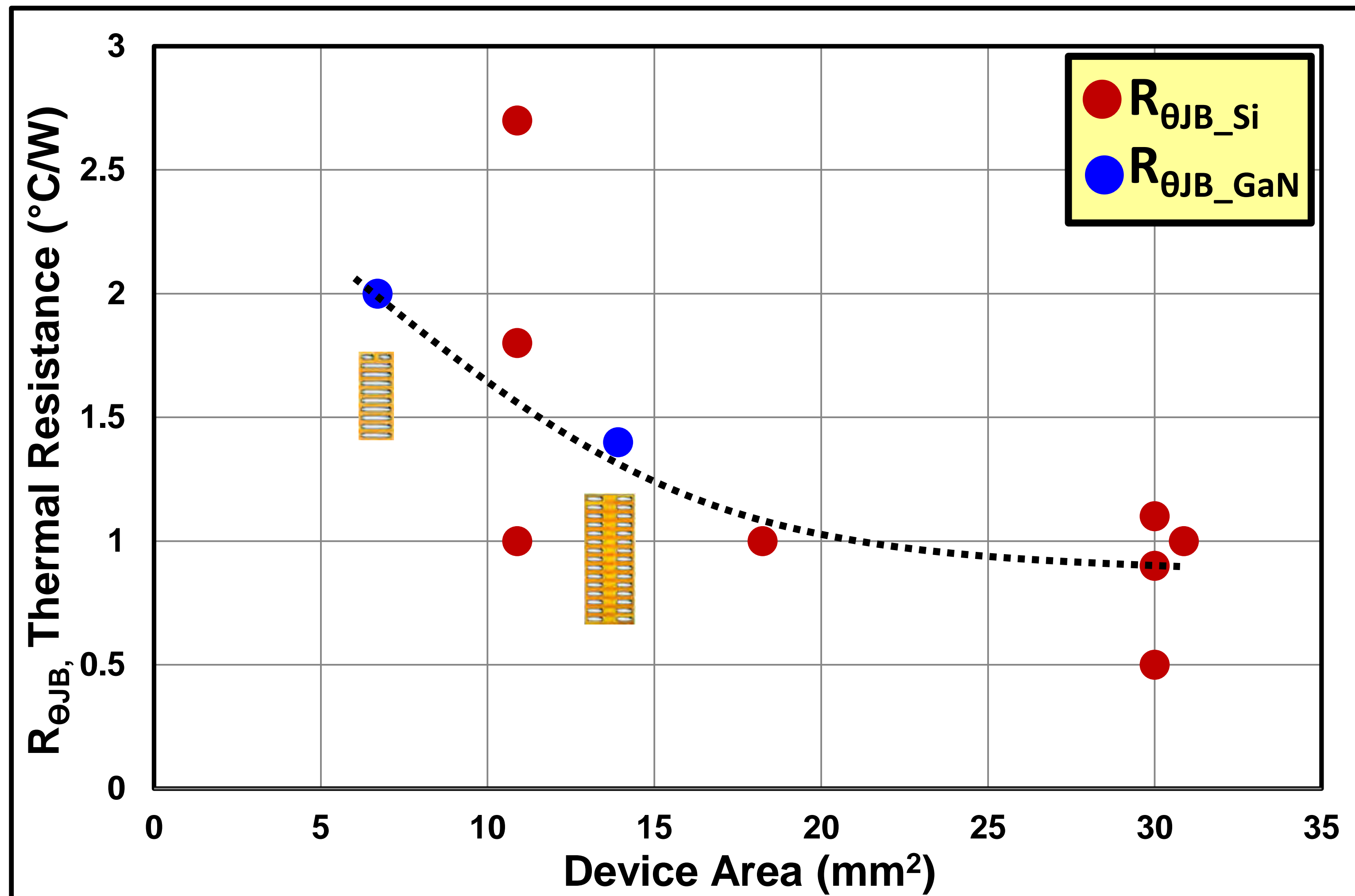
Silicon Substrate

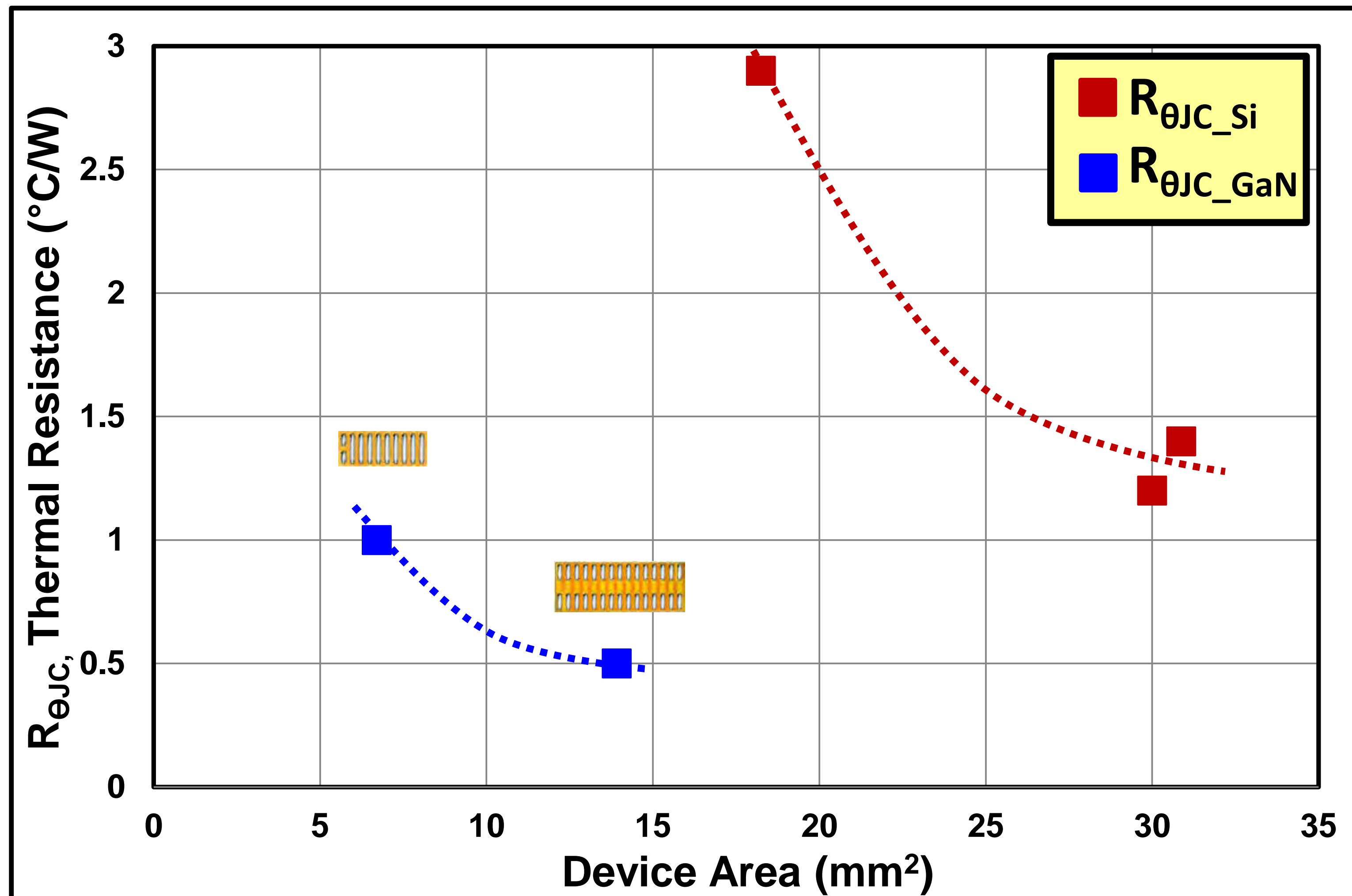
Active GaN Device Region



Thermal Comparisons



Thermal Comparisons



MOSFET vs. eGaN Costs*

	2010	2016
Starting Material	lower	lower
Epi Growth	***~higher***	***~same?***
Wafer Fab	lower	lower
Test	same	same
Assembly	lower	lower
OVERALL	**~higher**	***lower!***

* Product with the same on resistance and voltage rating

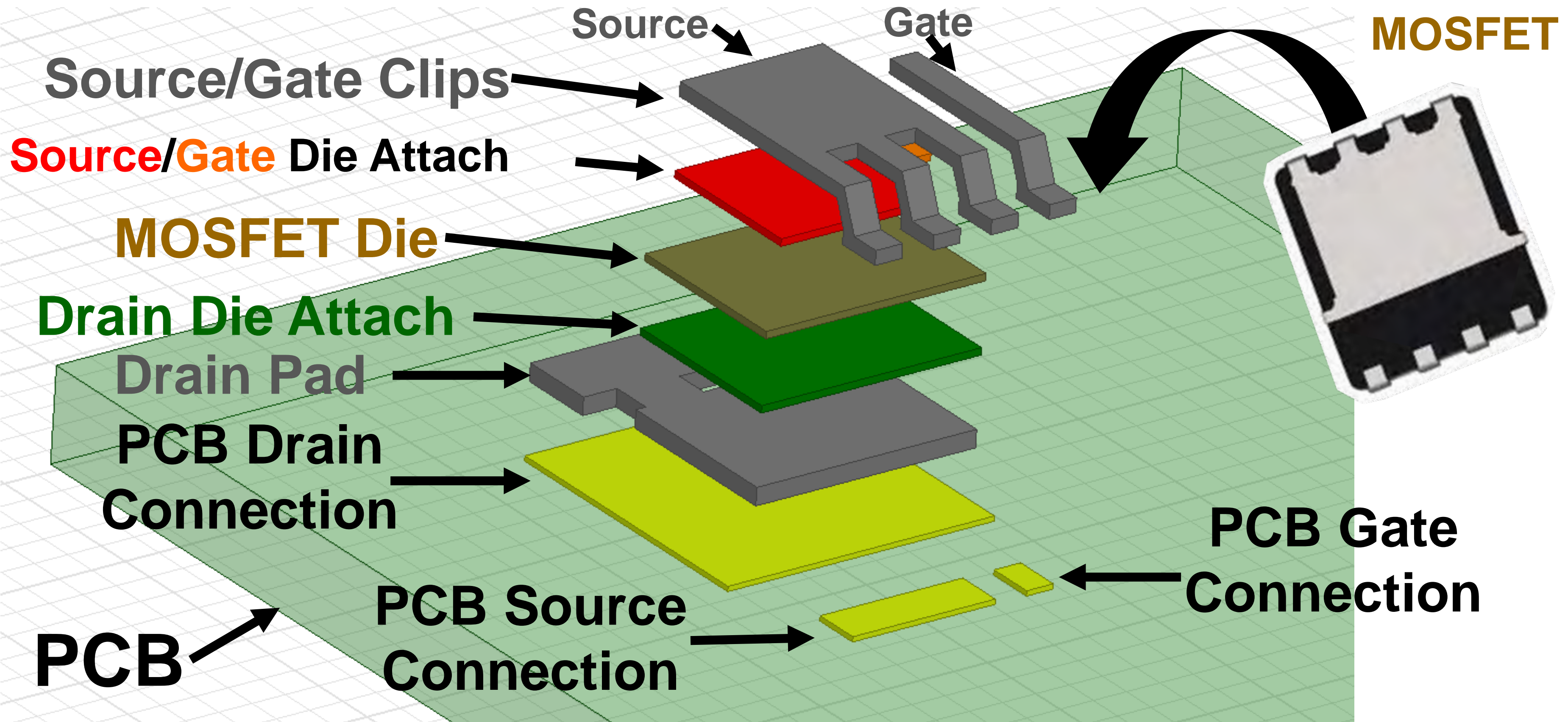
MOSFET vs. eGaN Costs*

Active die <3 mm^2

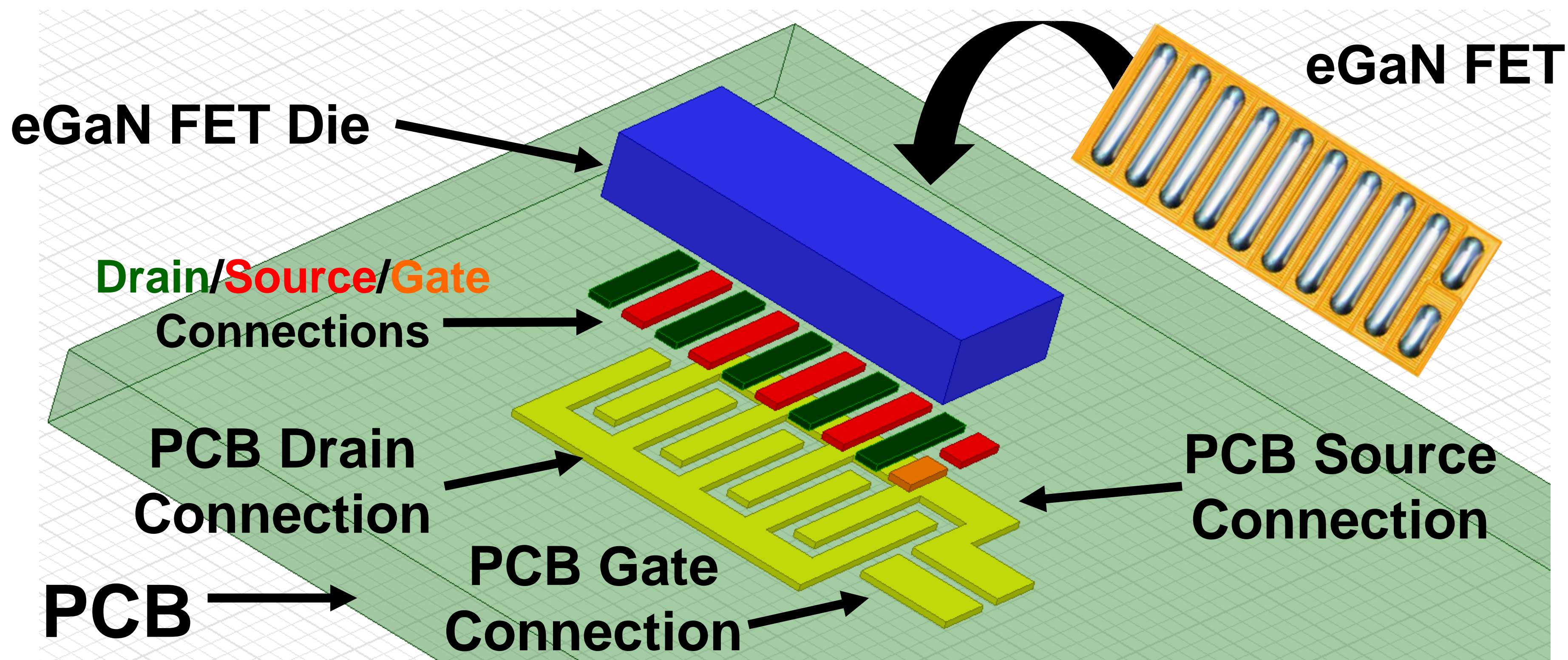
	2014	2016
Starting Material	lower	lower
Epi Growth	***~same***	***~same?***
Wafer Fab	lower	lower
Test	same	same
Assembly	lower	lower
OVERALL	***lower!***	***lower!***

* Product with the same on resistance and voltage rating

Better Power Package

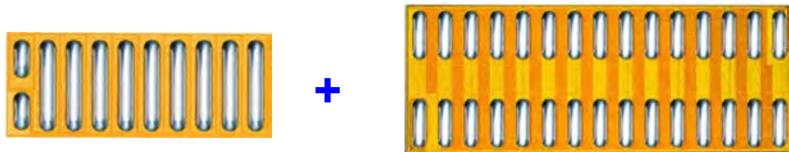


Better Power Package



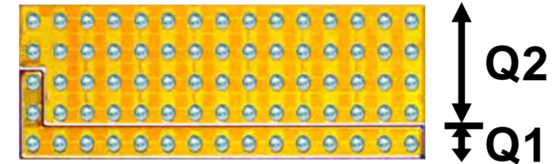
GaN Integration

Generation 2/4 Discrete HB

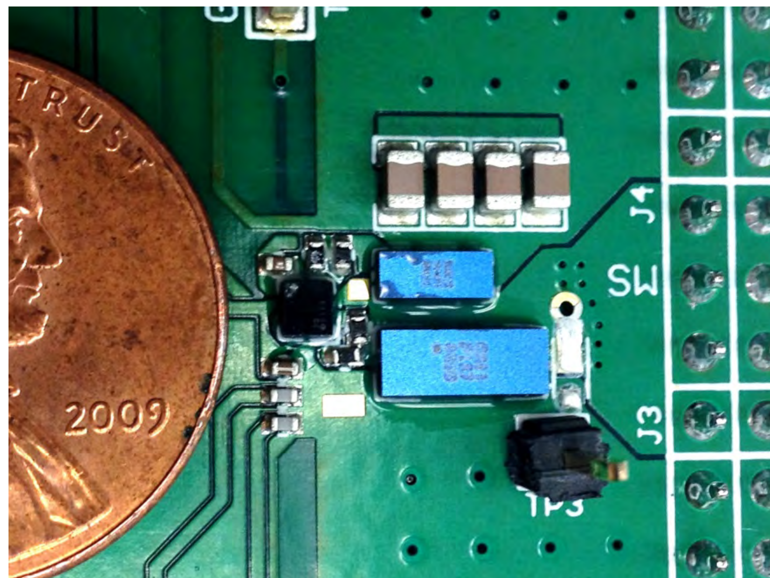


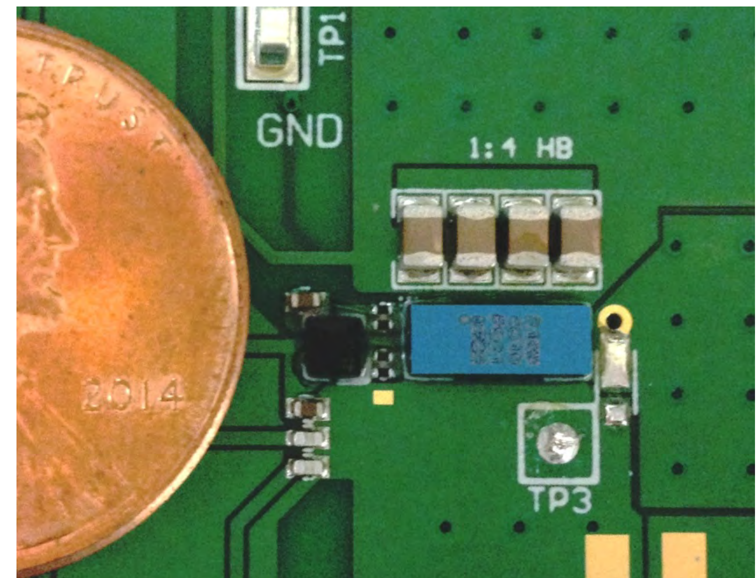
Top Switch (Q1) Bottom Switch (Q2)

Generation 4 Monolithic 1:4 HB

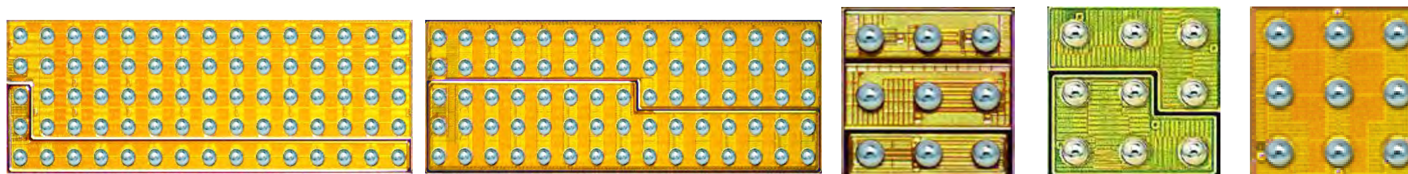


33 % die size reduction





GaN Integration

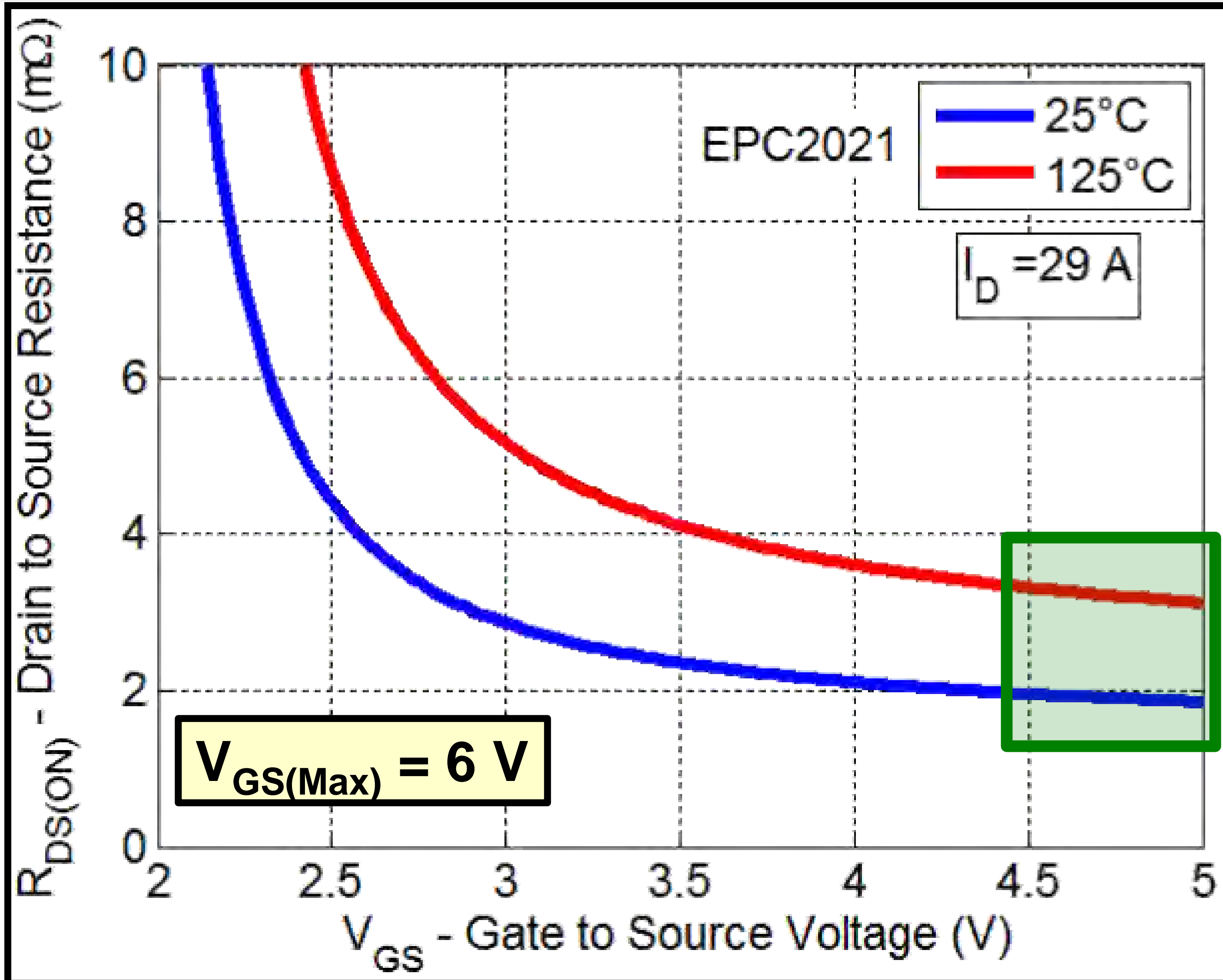


Part Number	Configuration	V_{DS}	Max $R_{DS(ON)}$ (mΩ) @5V_{GS}	Q_G typ (nC)	Q_{GS} typ (nC)	Q_{GD} typ (nC)	Q_{OSS} typ (nC)	Q_{RR} (nC)	Pulsed I_D (A)
EPC2100	Dual Asymmetric	30	8 2	3.5 15	1.4 4.6	0.57 2.6	5.5 28	0	100 400
EPC2101	Dual Asymmetric	60	11.5 2.7	2.7 12	1 3.7	0.50 2.5	9 45	0	80 350
EPC2102	Dual	60	4.4	6.8	2.3	1.4	23 31	0	215
EPC2108	Dual with Bootstrap	60	190	0.22	0.085	0.045	0.65 1	0	5.5
EPC2105	Dual Asymmetric	80	14.5 3.5	2.5 10	1 3.2	0.50 2	11 55	0	75 320
EPC2103	Dual	80	5.5	6.5	2.0	1.3	29 39	0	195
EPC2104	Dual	100	6.3	7	2.0	1.2	35 47	0	165
EPC2106	Dual	100	70	0.73 0.76	0.22 0.24	0.165	3.4 4.4	0	18
EPC2107	Dual with Bootstrap	100	320	0.16	0.065	0.04	0.8 1.4	0	3.8
EPC2110	Dual, Common Source	120	60	0.8	0.25	0.19	4.9	0	20

Design Basics

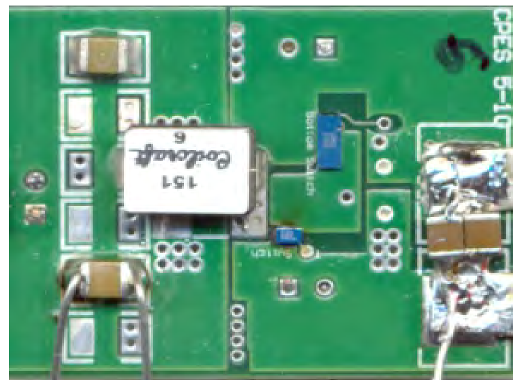
Gate Drive

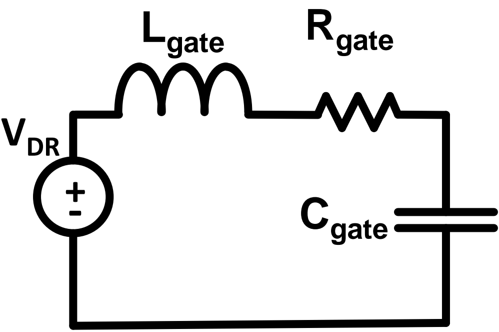
Gate Voltage



Gate Drive Design

2010 GaN Board #1





File Edit Vertical Horiz/Acq Trig Display Cursors Measure Math Utilities Help

Tek Stopped 354 Acqs 06 Oct 10 14:26:57

Buttons

V_{GS} eGaN FET

Circa 2010

Max(C2) 5.44V

Freq(C2) -Hz No period found

+DtyCyc(C2) -% No period found

Min(C2) -3.6V

2 V/ div

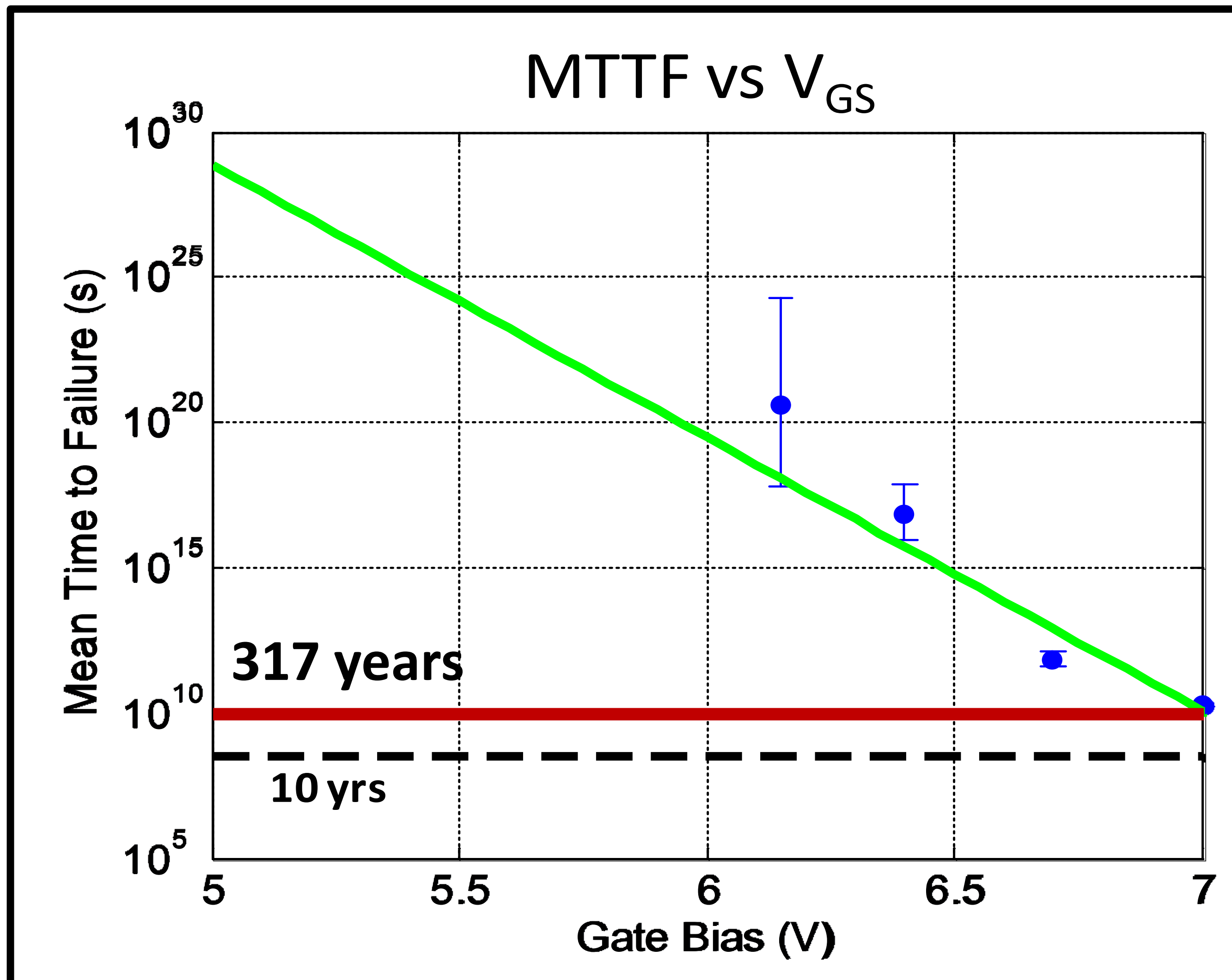
80 ns/ div

Ch2 2.0V

M 80.0ns 5.0GS/s 200ps/pt

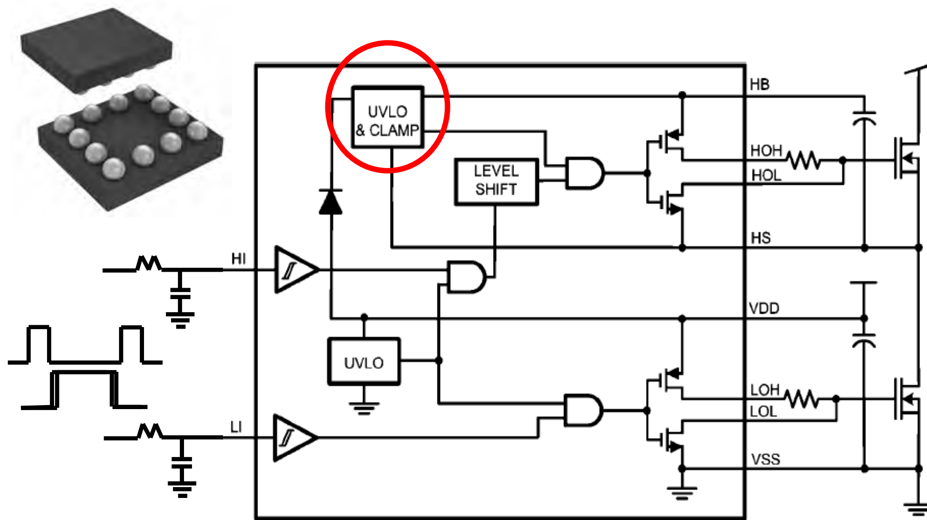
A Ch2 ↘ 2.8 V

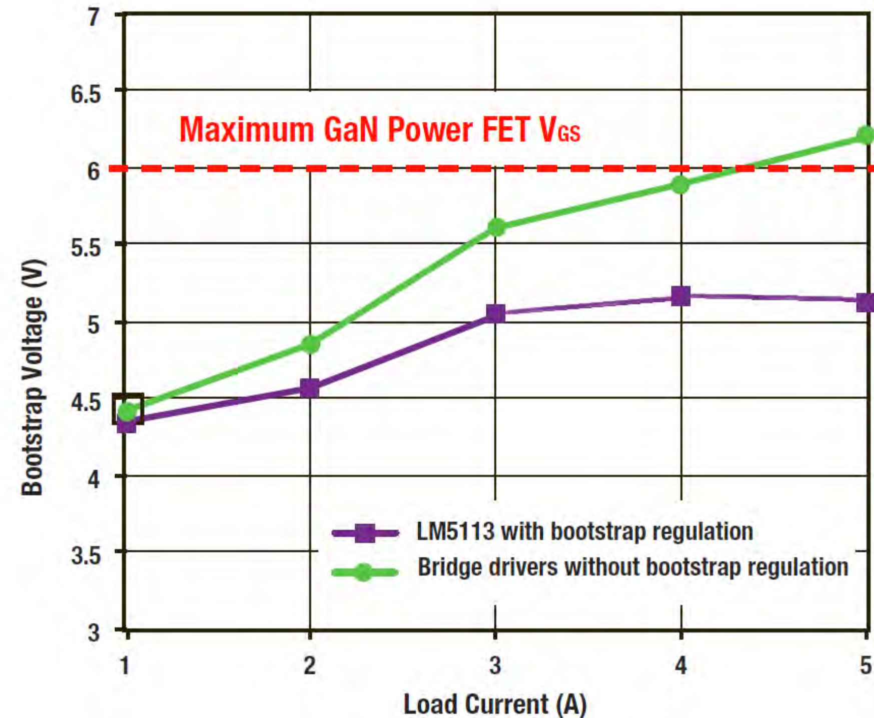
Reliability of eGaN FET



Reference: R. Strittmatter, C. Zhou, A. Lidow, and Y. Ma, "Enhancement Mode Gallium Nitride Transistor Reliability," APEC 2015

eGaN FET Driver IC

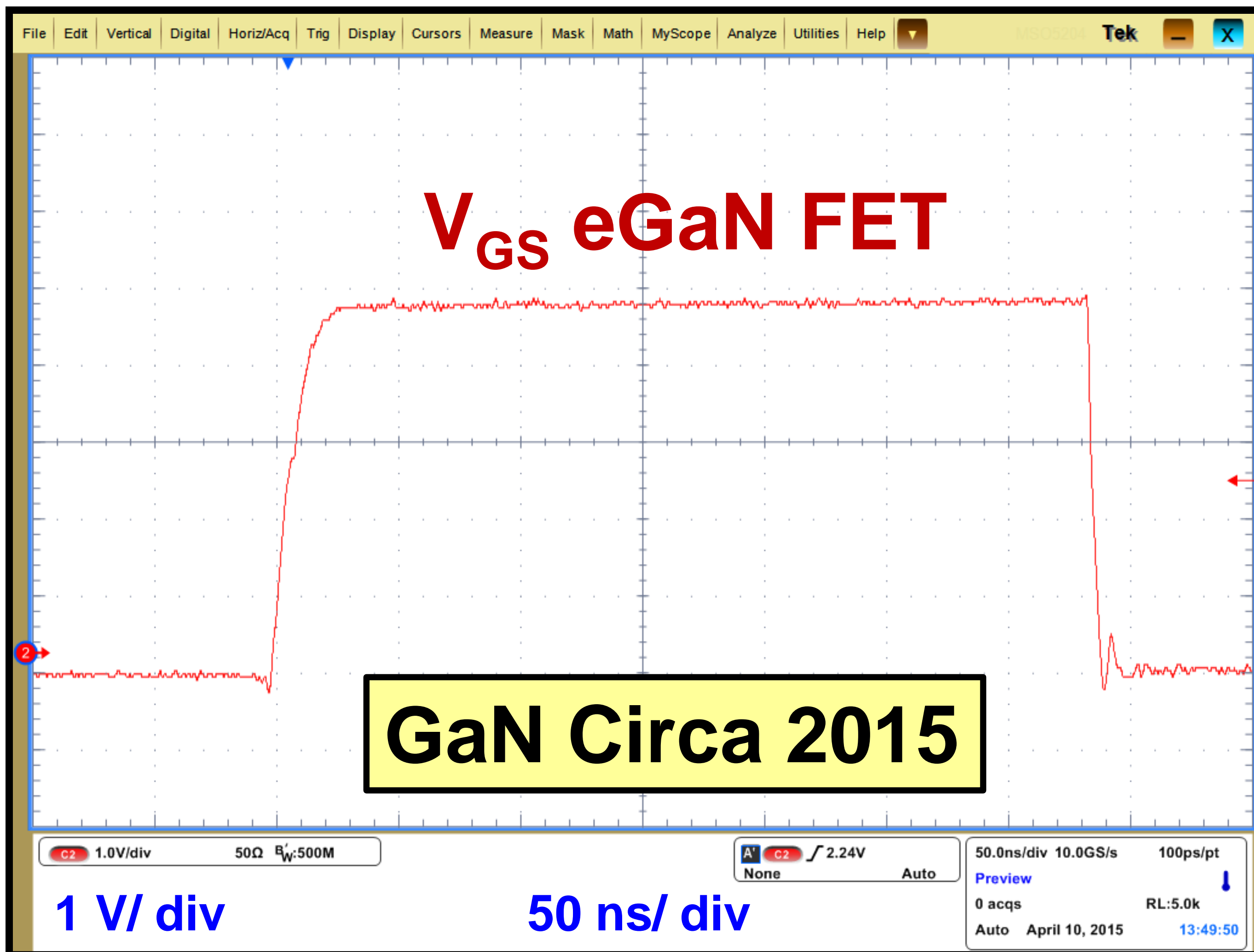




- Bootstrap clamp limits (HS) supply

Reference: Texas Instruments, “Gate Drivers for Enhancement Mode GaN Power FETs 100 V Half-Bridge and Low-Side Drivers Enable Greater Efficiency, Power Density, and Simplicity,” SNVB001

Minimizing Overshoot



Dead-time

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Reverse Conduction Period

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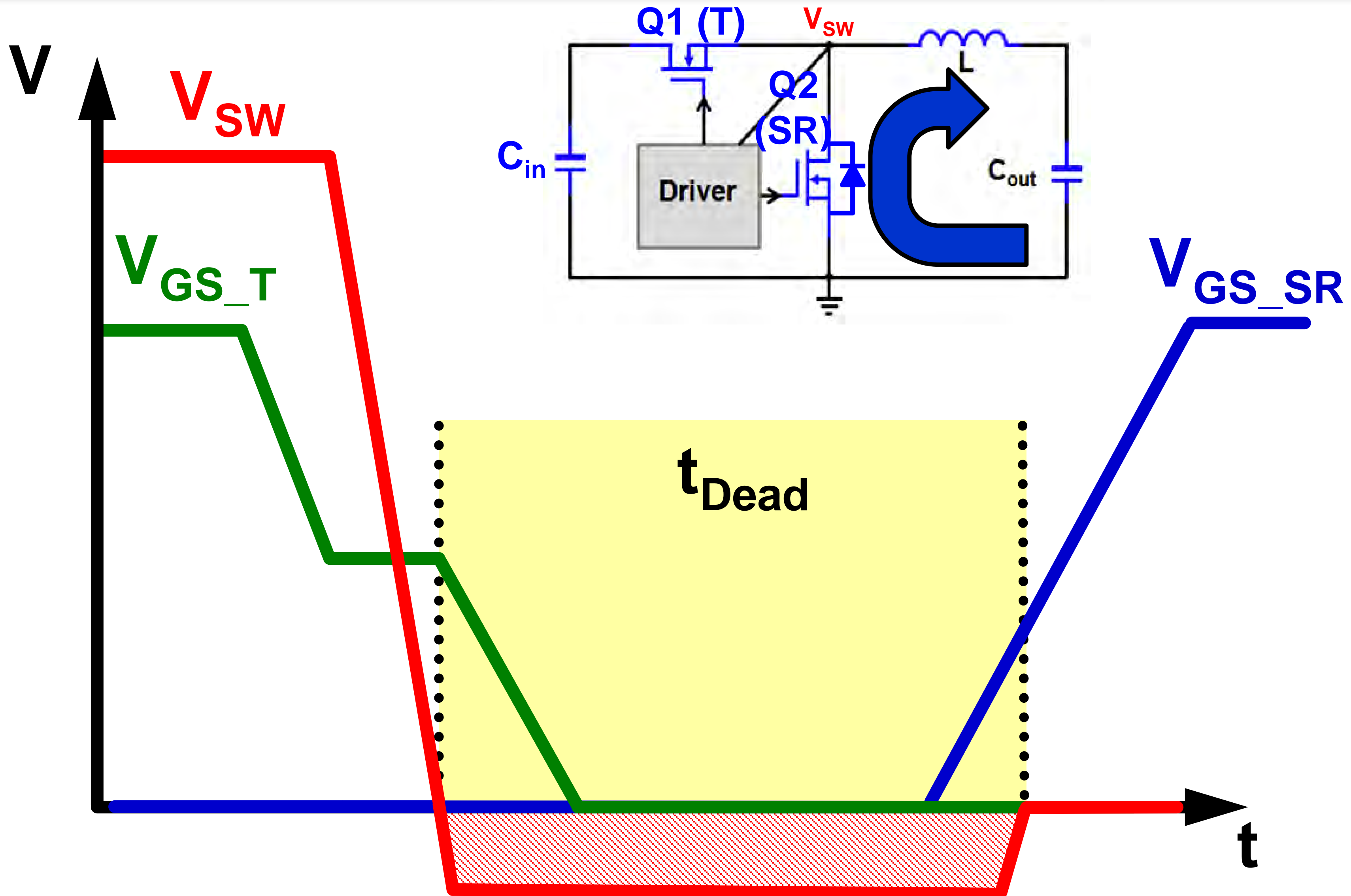
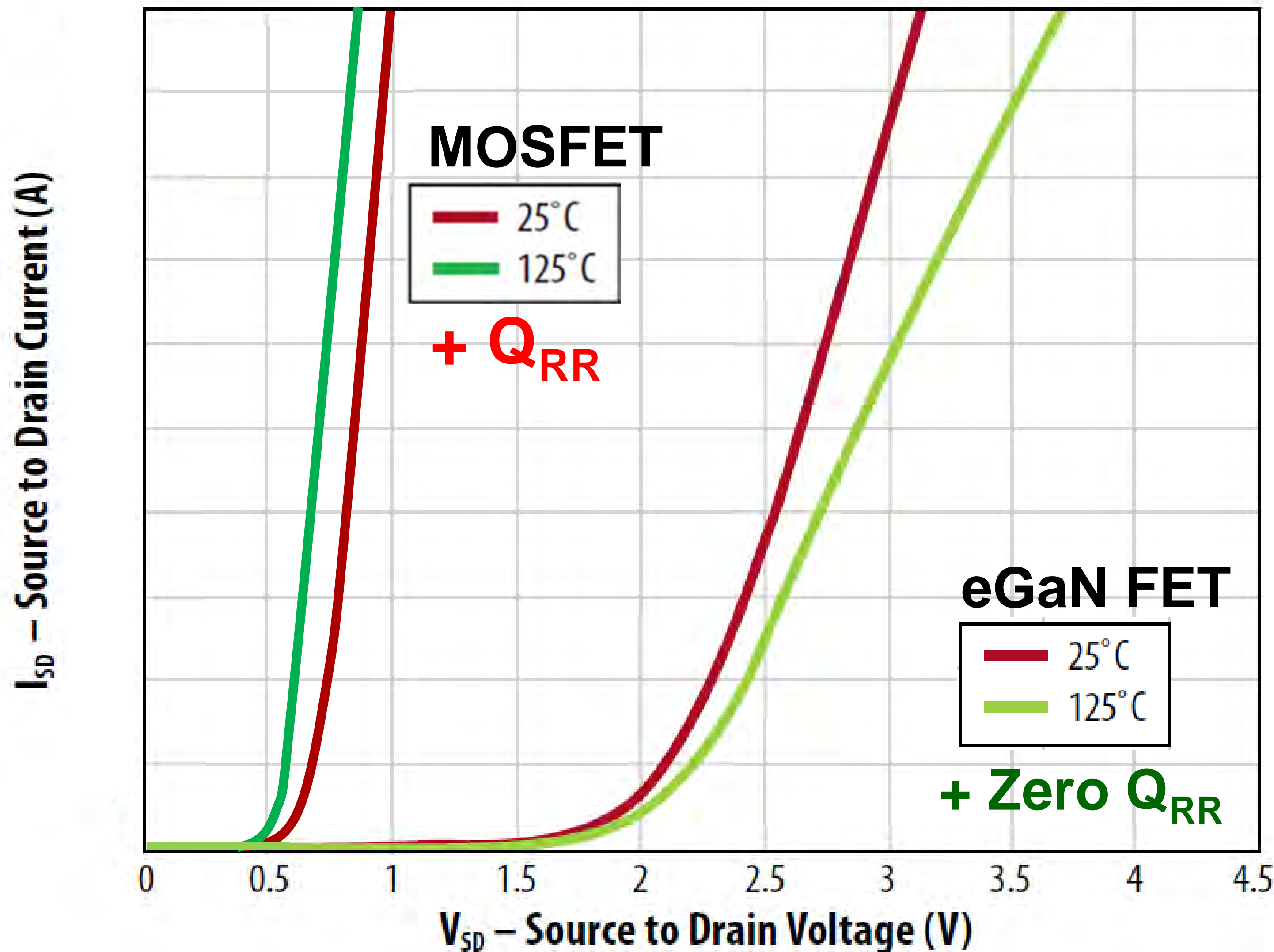
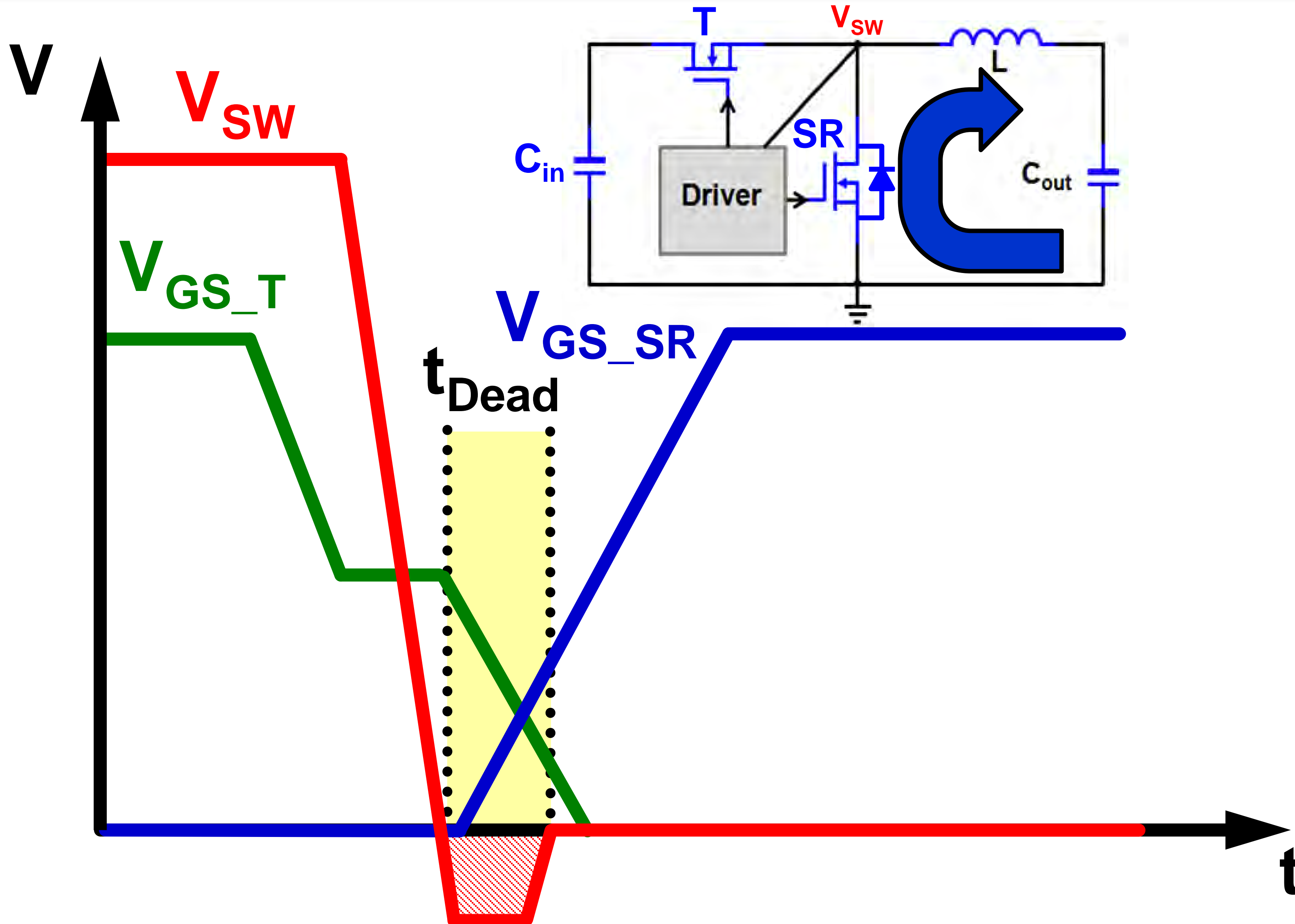


eGaN FET Reverse Conduction

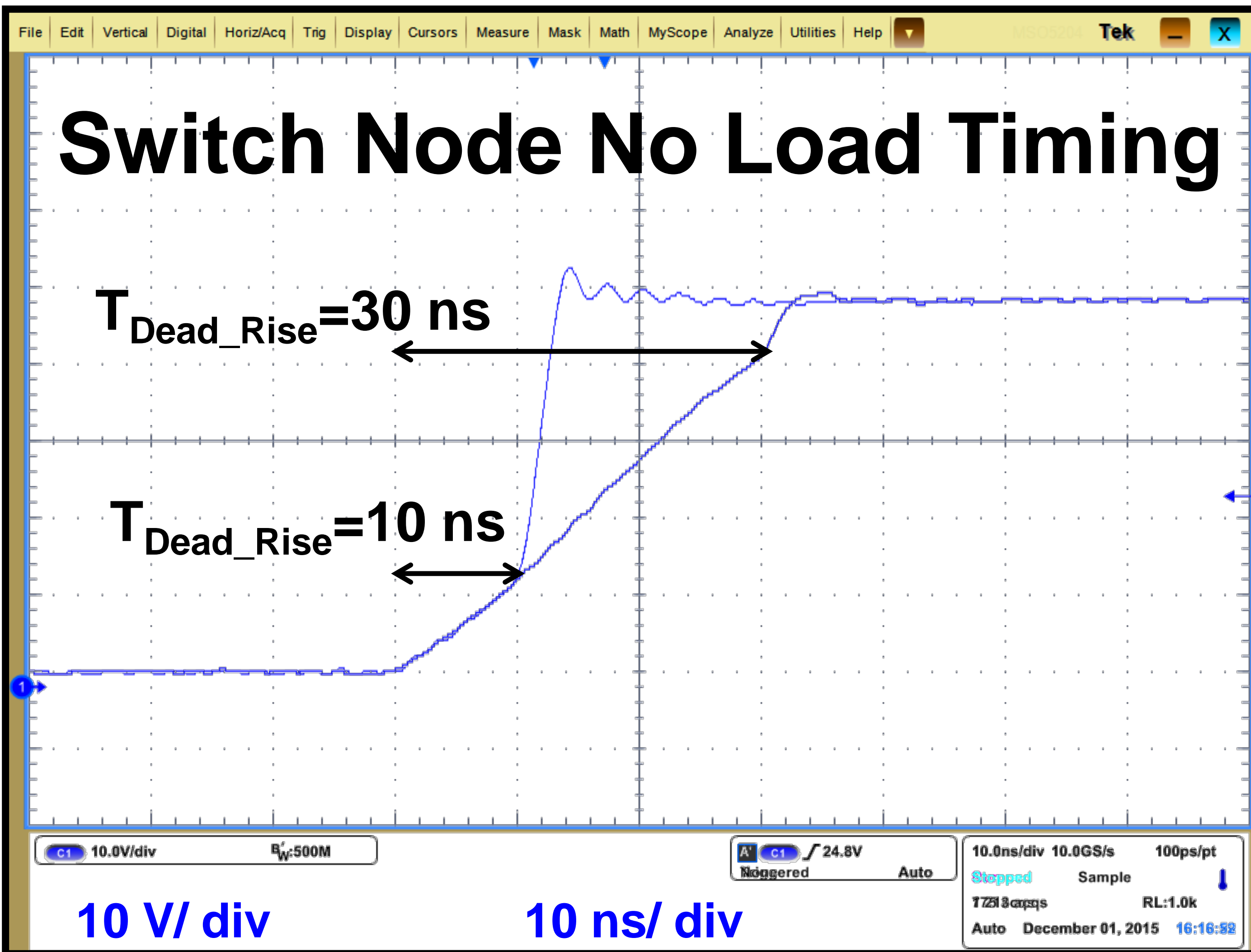
EPC EFFICIENT POWER CONVERSION



Reverse Conduction Period

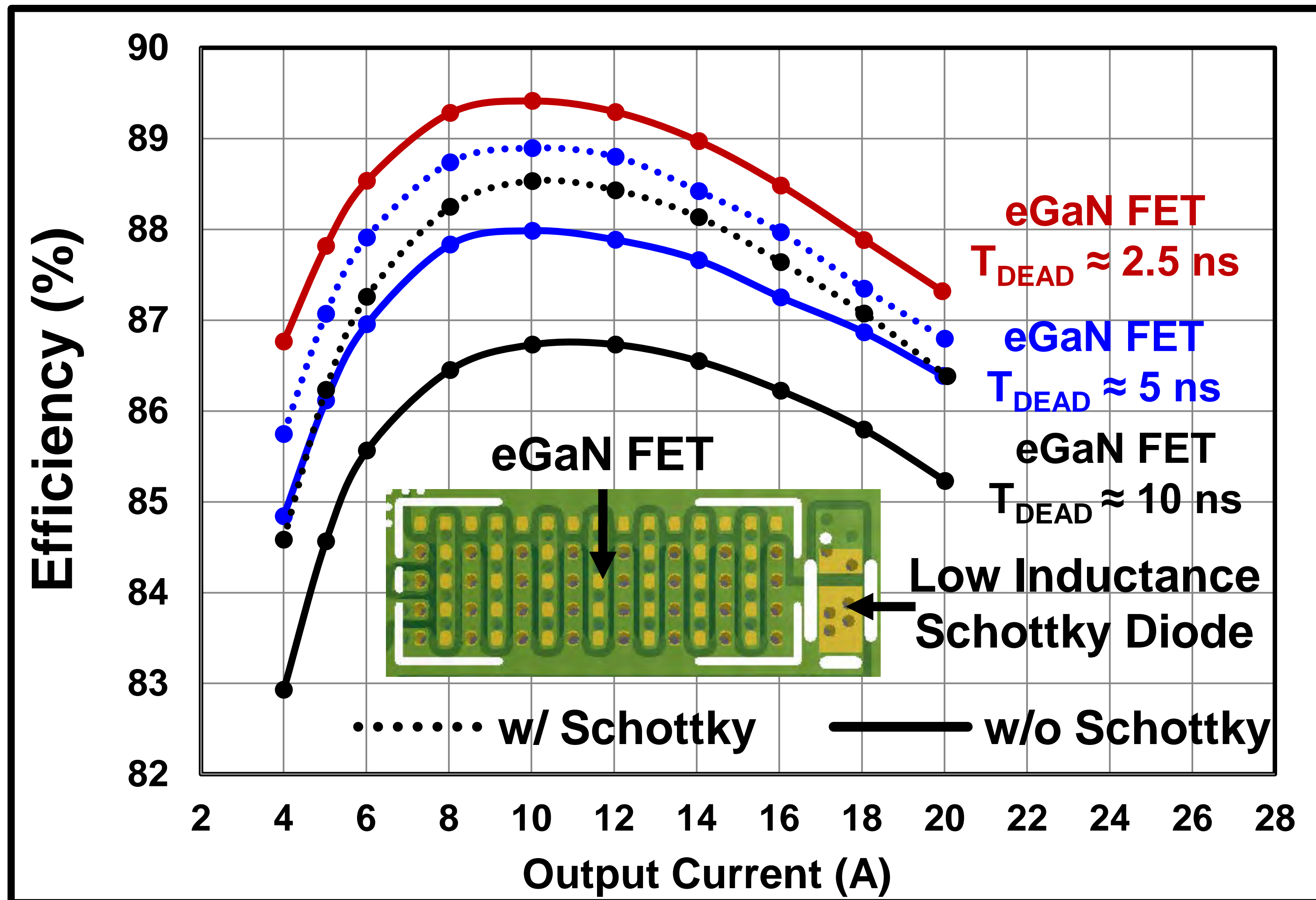


Dead Time Setup



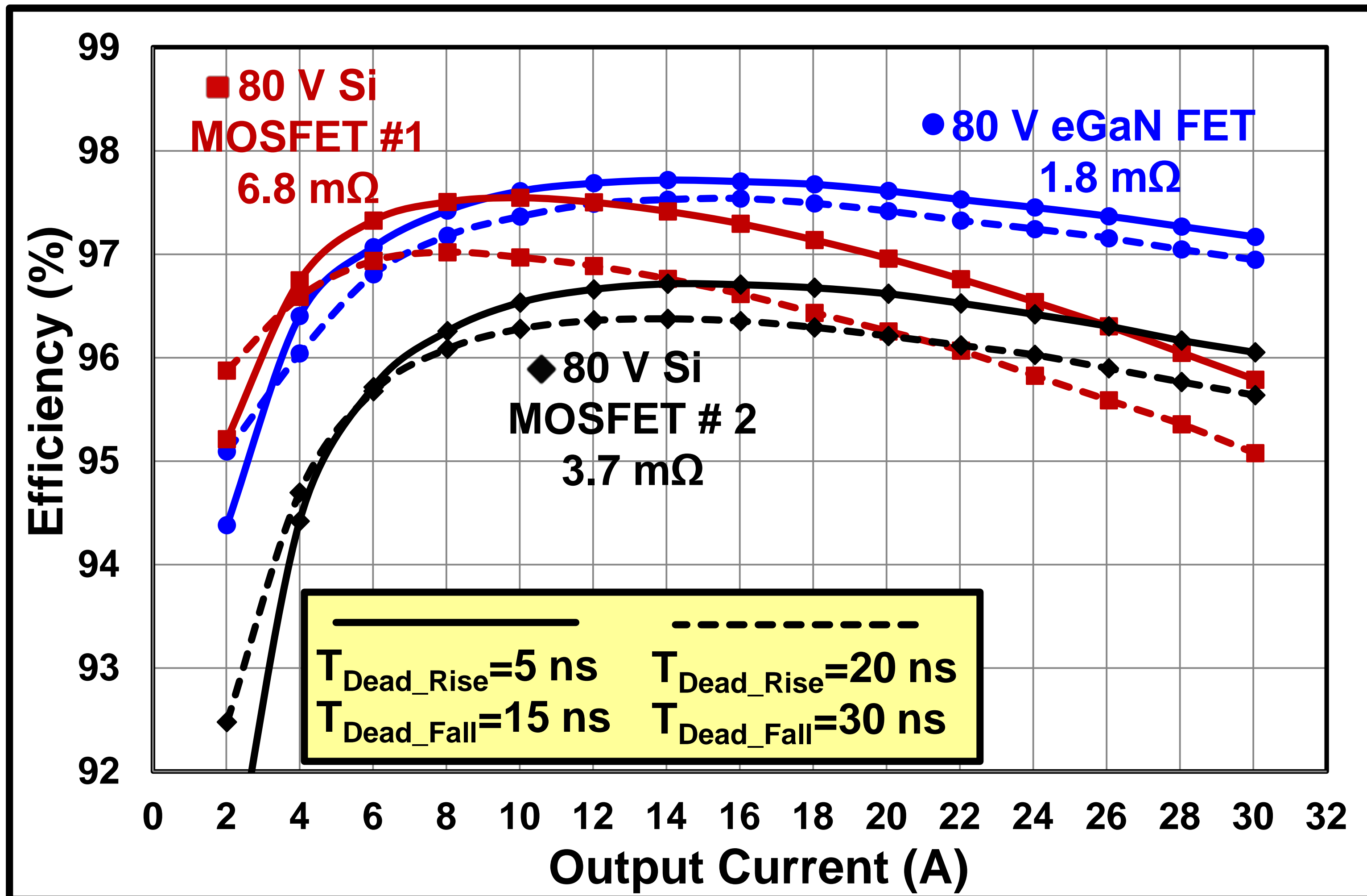
V_{IN}=48 V V_{OUT}≈12 V I_{OUT}=0 A f_{sw}=300 kHz L=4.7uH

Impact of Dead-time on Low Voltage



V_{IN} =12 V, V_{OUT} =1.2 V, and f_{sw} =1 MHz

Impact of Dead-time on High Voltage



V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7uH

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Impact of Rising Edge Dead-time

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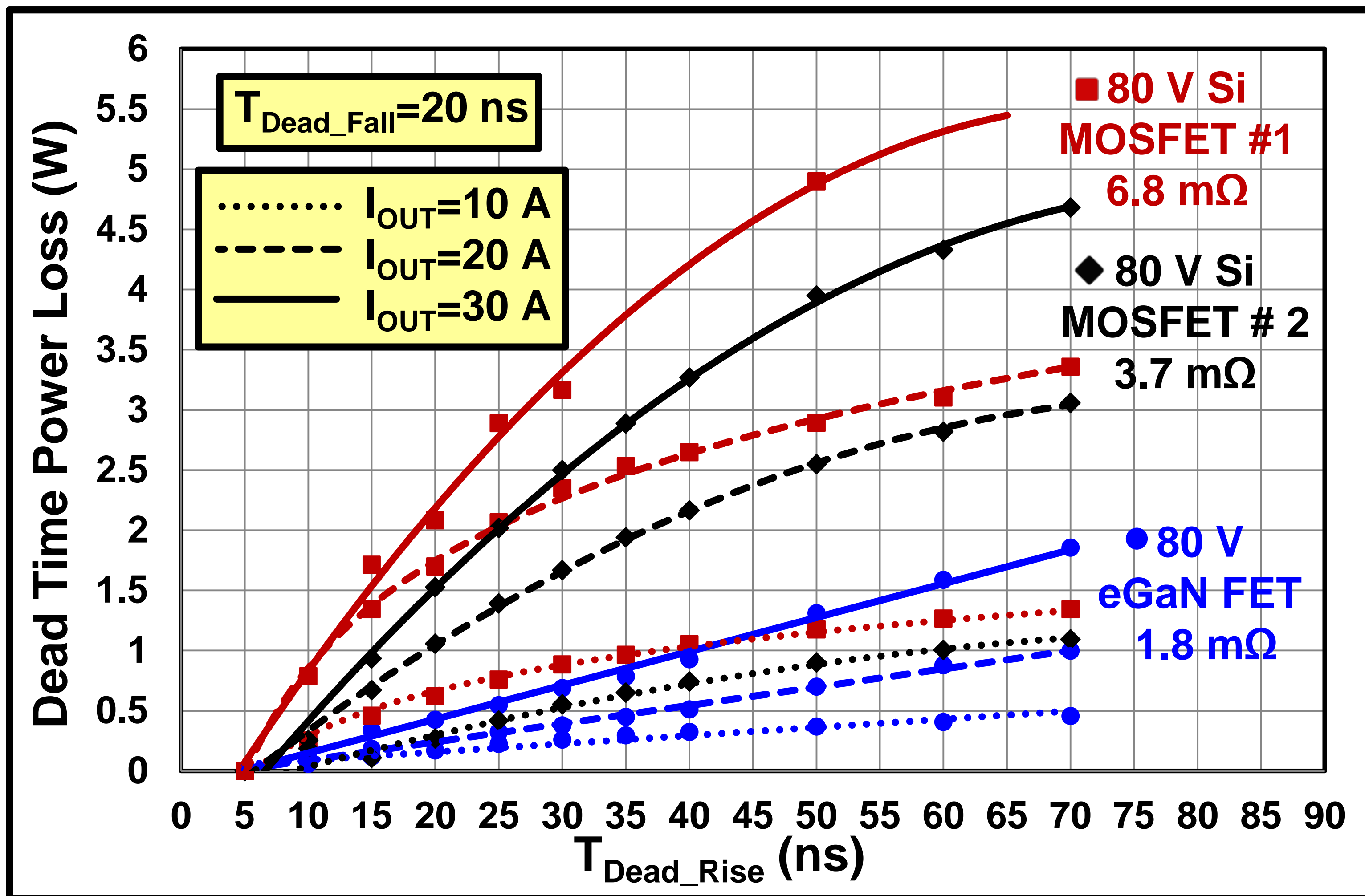
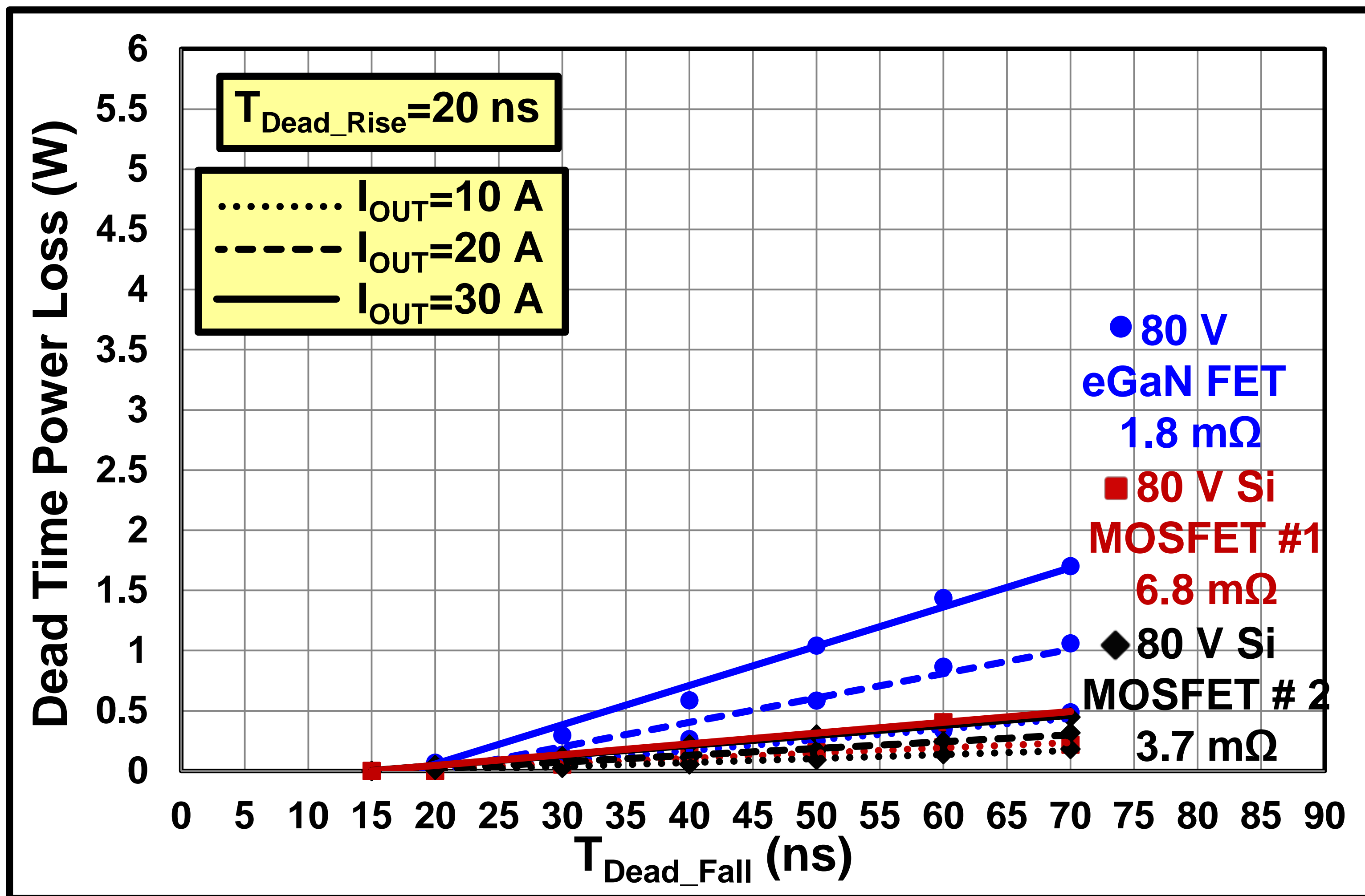


V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7uH

Impact of Falling Edge Dead-time



V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7uH

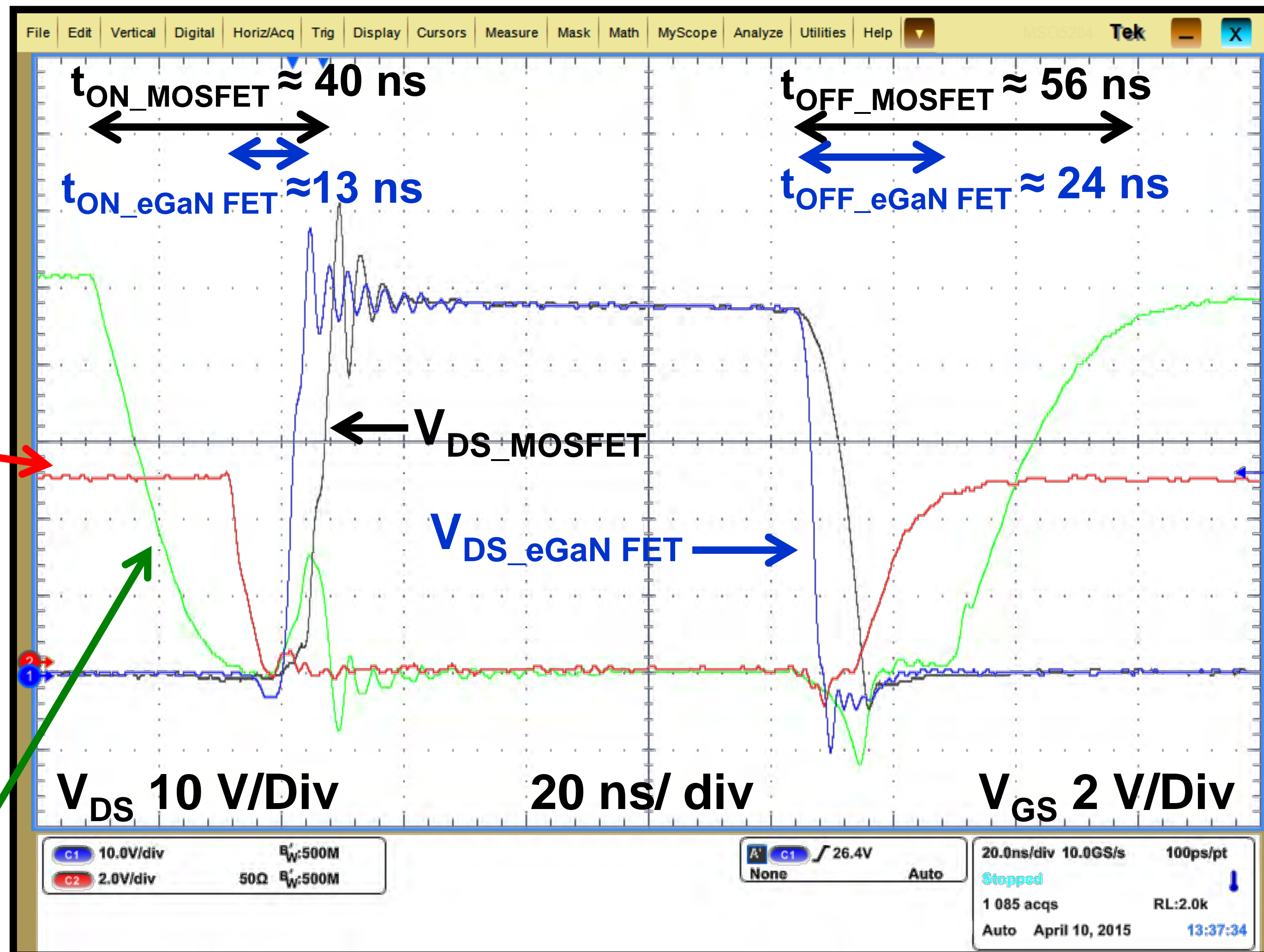
Dead-time Requirements

80 V eGaN FET
1.8 mΩ
13.9 mm²

$V_{DS_eGaN\ FET}$
$V_{GS_eGaN\ FET}$

80 V Si MOSFET
3.7 mΩ
31 mm²

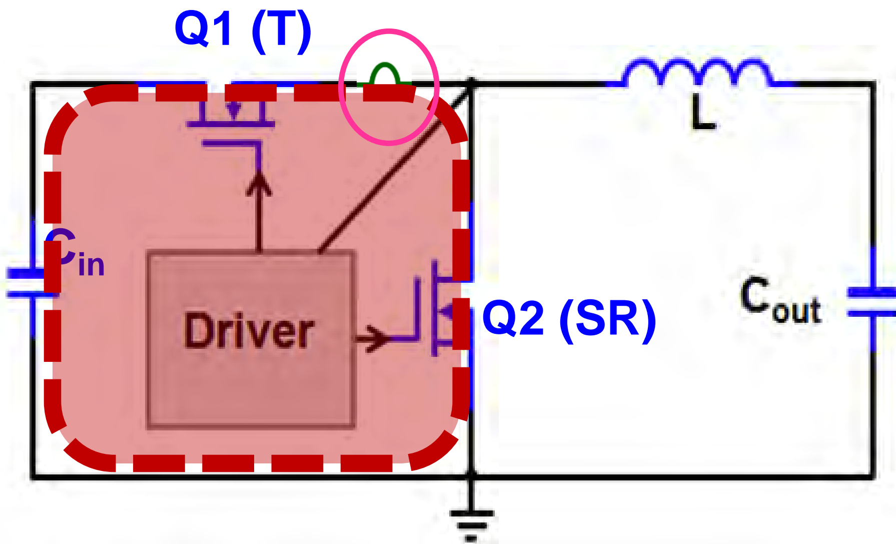
V_{GS_MOSFET}
V_{DS_MOSFET}

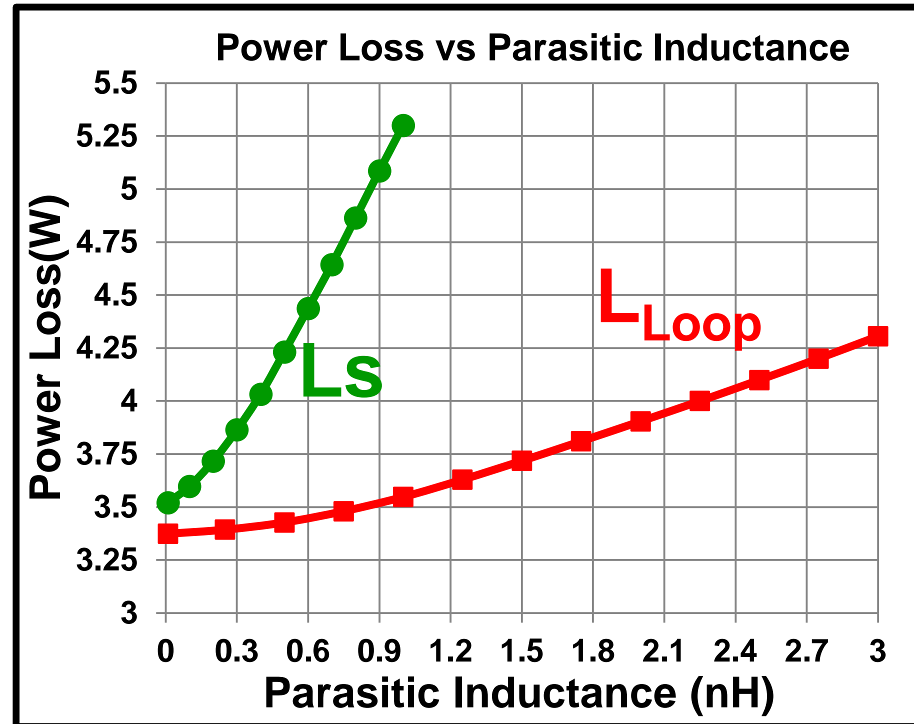


V_{IN}=48 V V_{OUT}=1 V I_{OUT}=30 A

Layout

Converter Parasitics



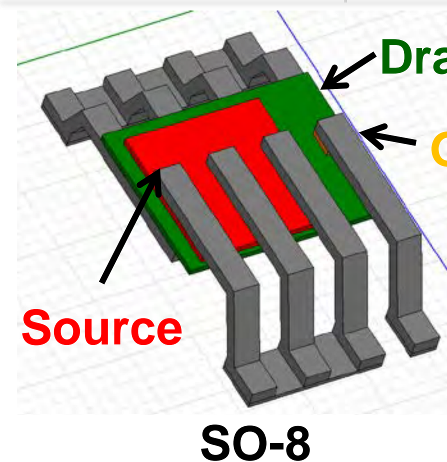


L_S: Common Source Inductance

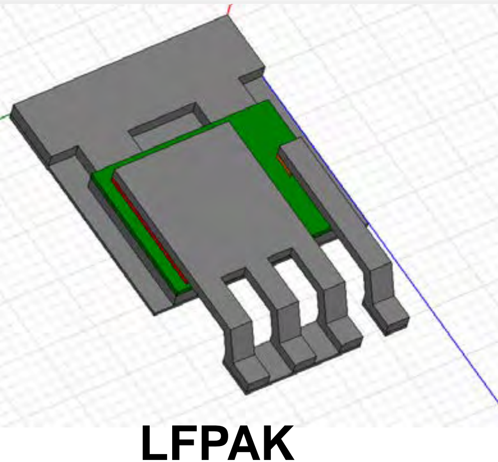
L_{Loop}: High Frequency Power Loop Inductance

V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, I_{OUT}= 20 A

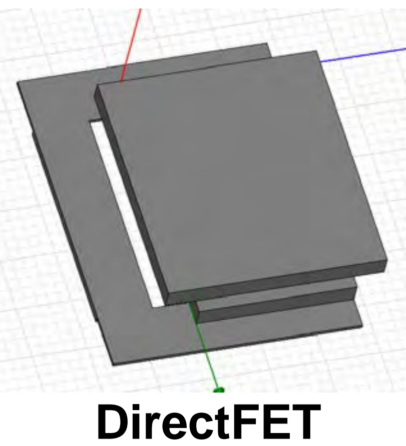
Impact of Package on Power Switch



SO-8

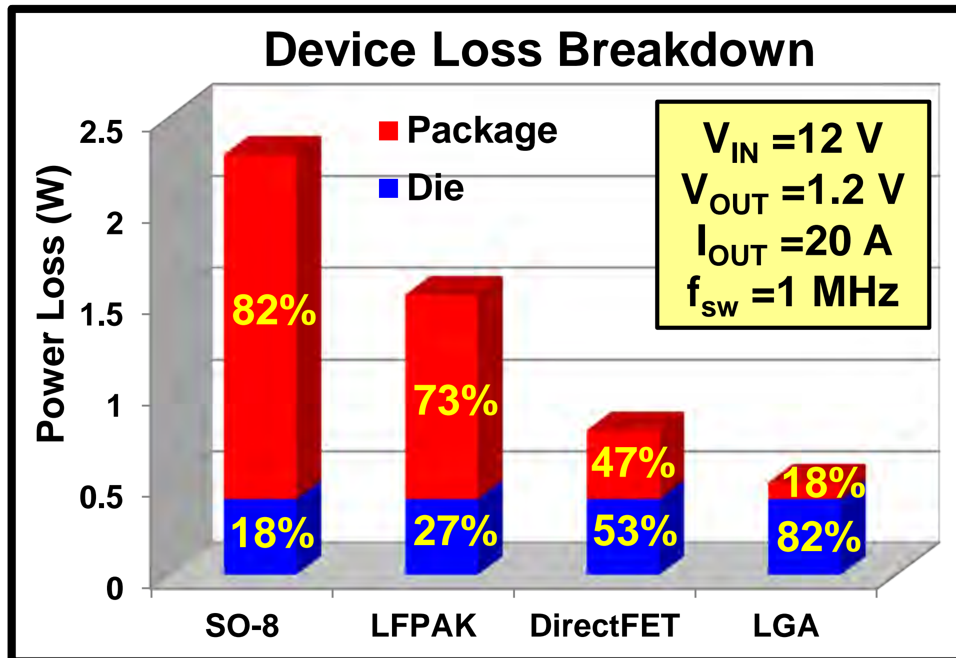


LFPAK



DirectFET

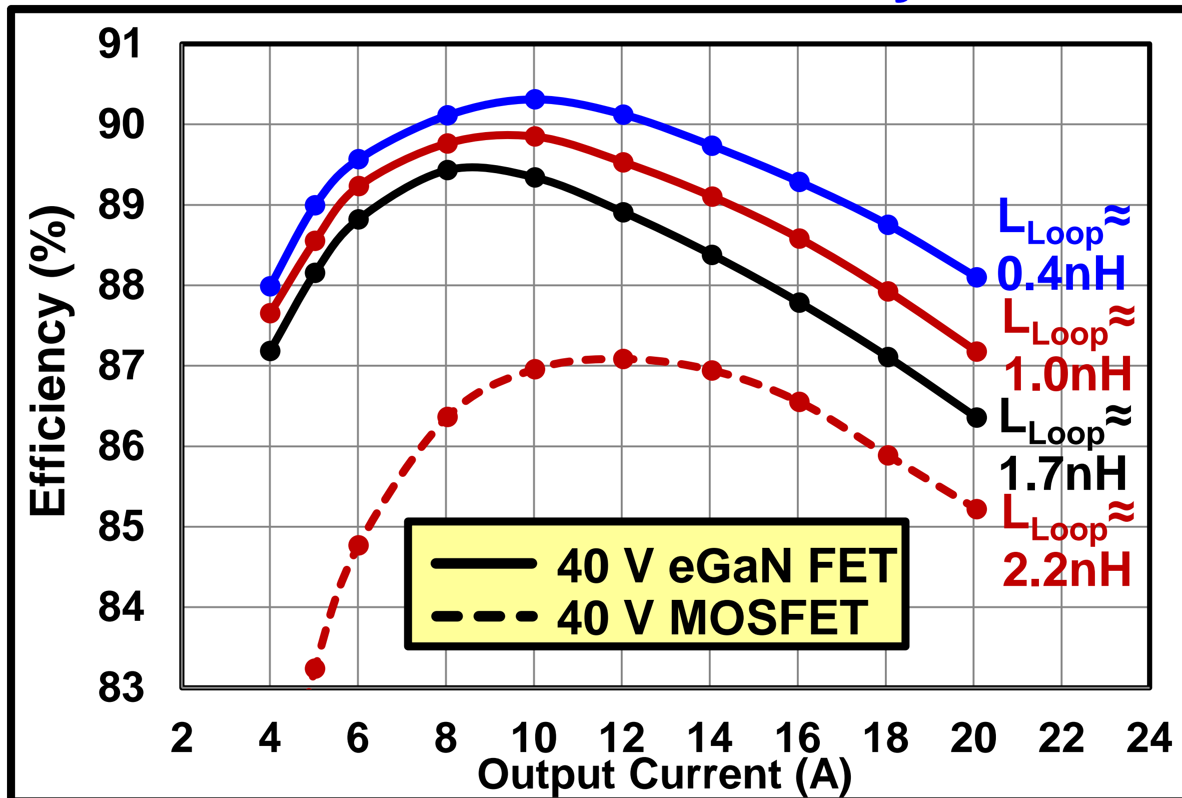
LGA eGaN FET



Reference: D. Reusch, D. Gilham, Y. Su, and F.C. Lee, C, "Gallium Nitride Based 3D Integrated Non-Isolated Point of Load Module," APEC 2012

Layout Impact on Efficiency

Measured Efficiency



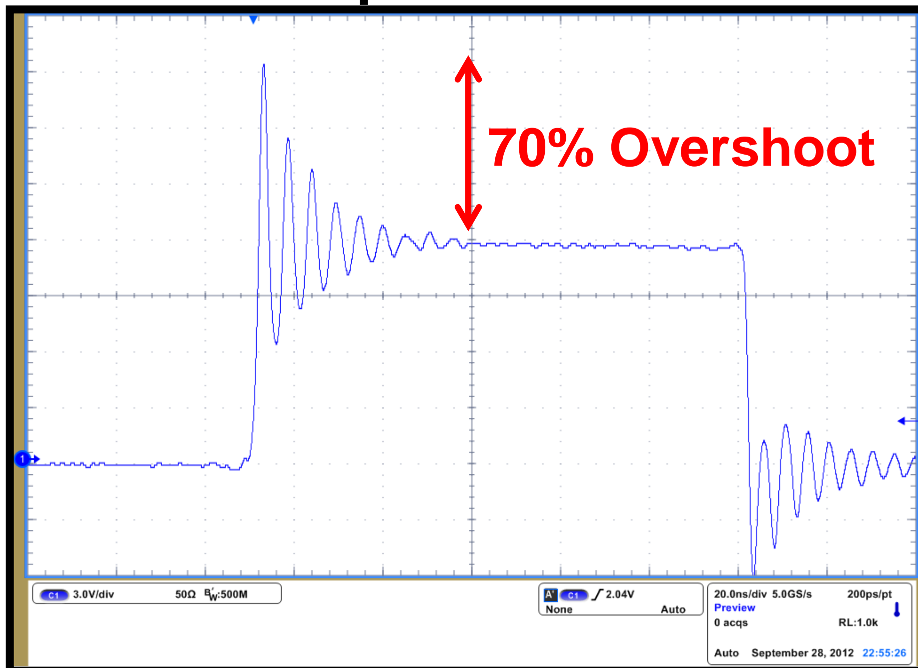
V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, L=300 nH

EPC Optimal Layout

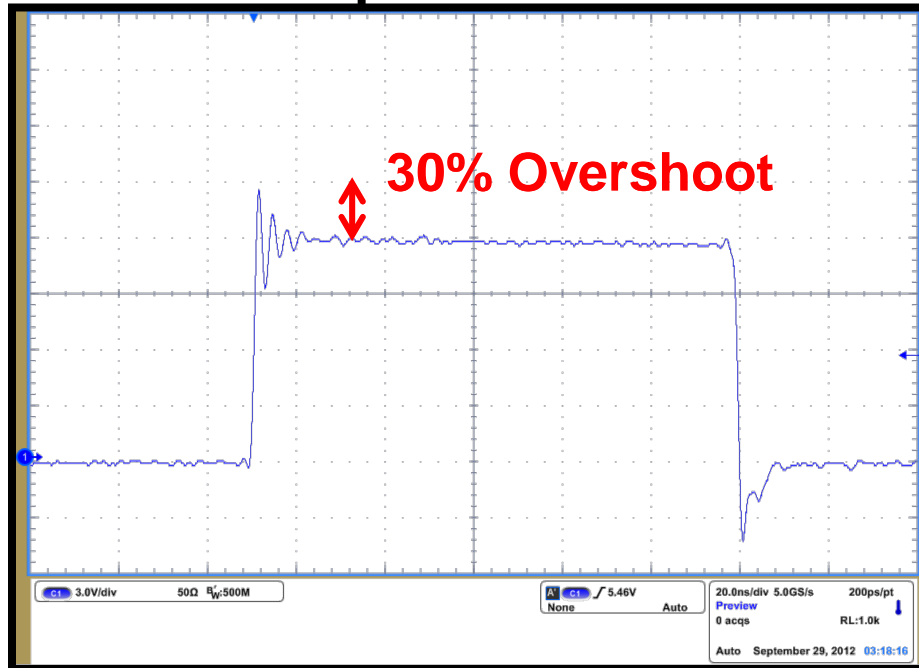
Ref: D. Reusch, J. Strydom, "Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter," APEC 2013, IEEE Transactions on Power Electronics 2014

Layout Impact on Peak Voltage

L_{Loop}≈1.0 nH



L_{Loop} ≈ 0.4 nH

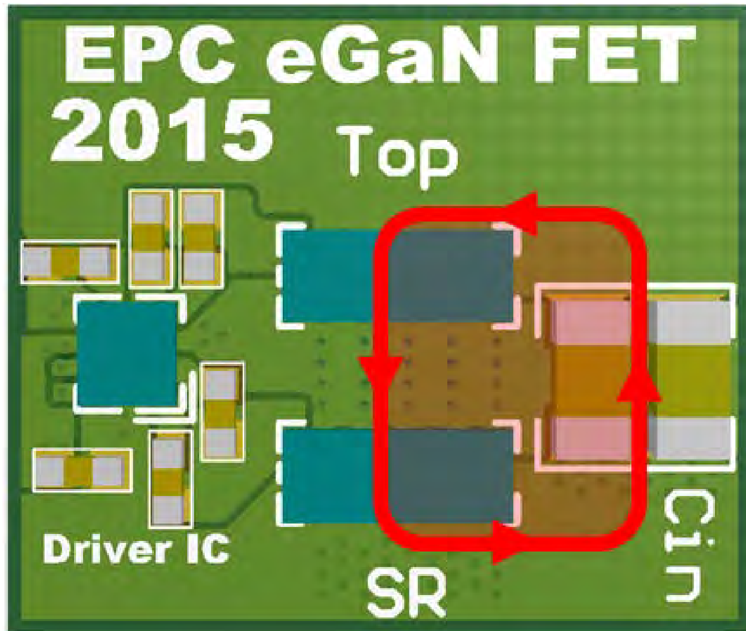


Switching Node Voltage

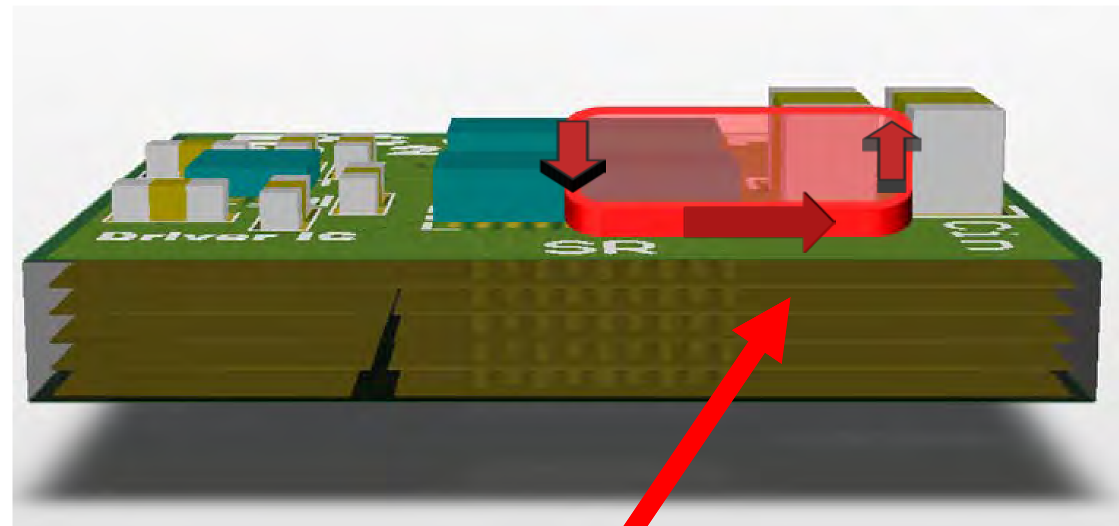
V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A
f_{sw}=1 MHz L=150 nH

Conventional Lateral Layout

Top View

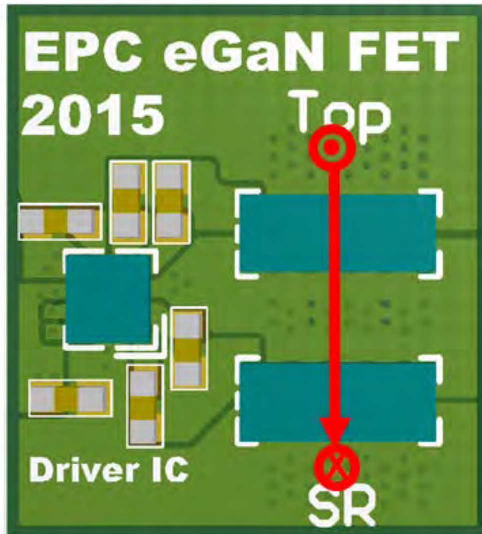


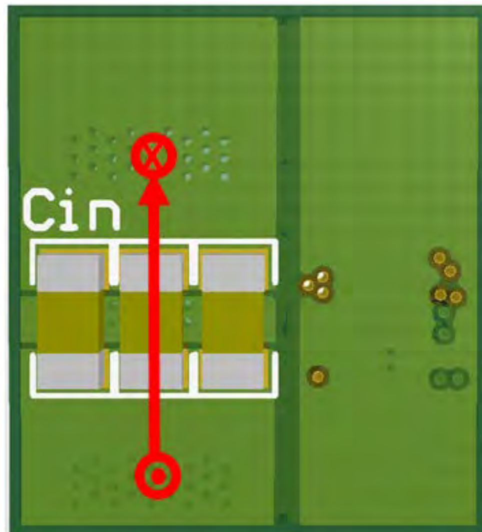
Side View

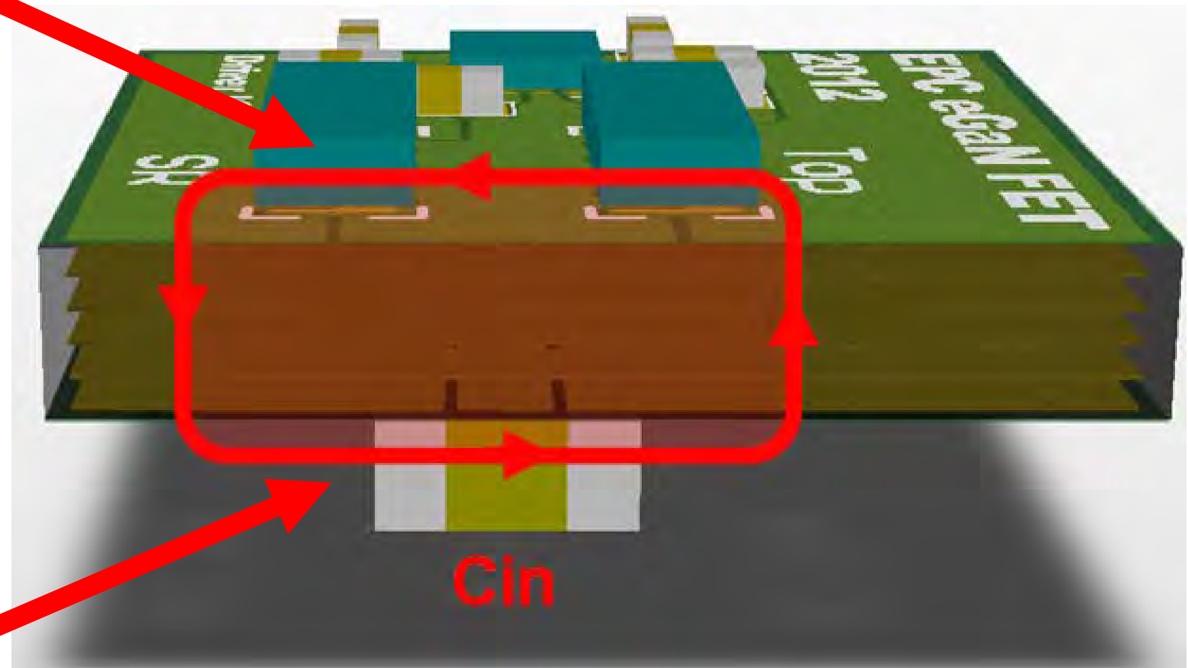


Shield Layer

Conventional Vertical Layout

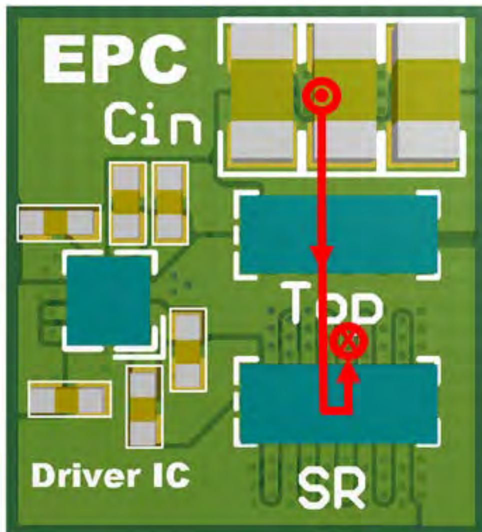




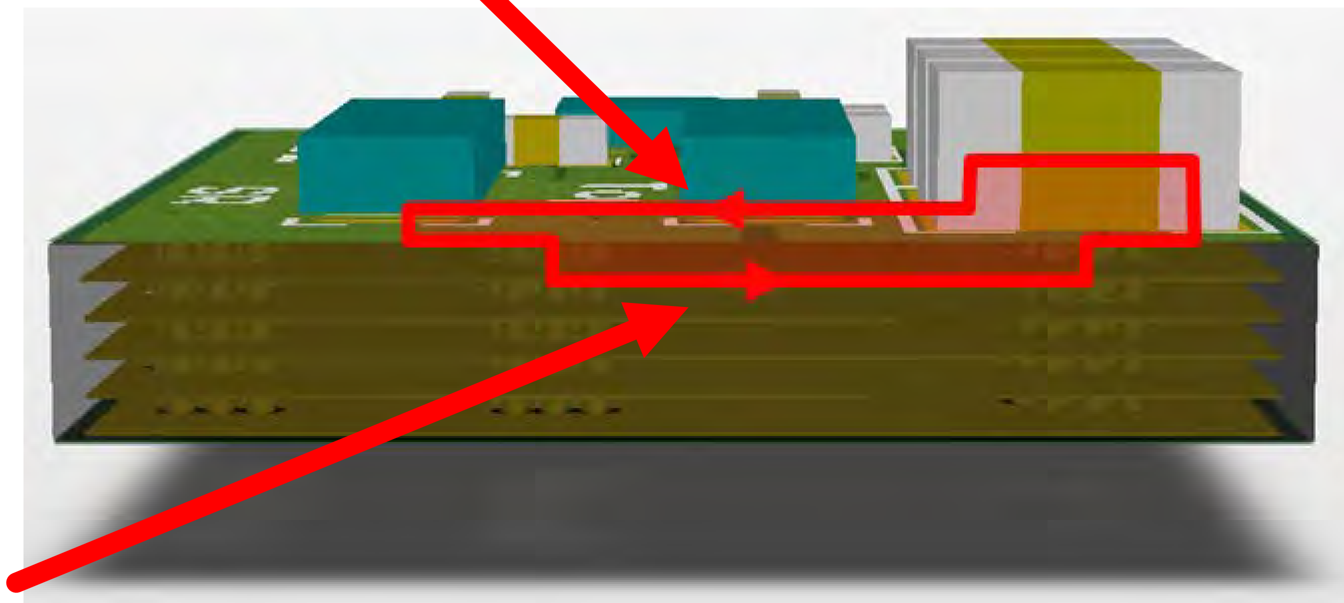


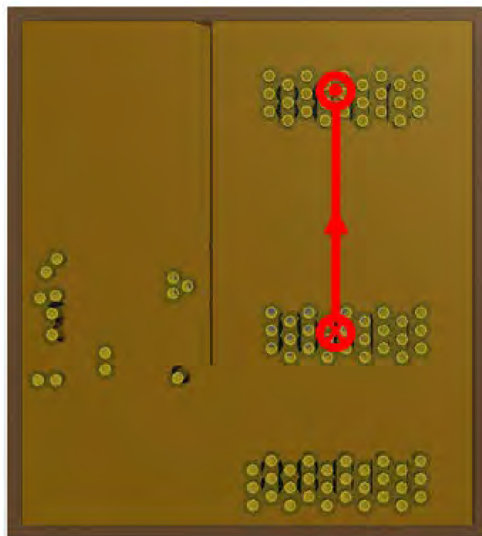
EPC Optimal Layout

Top View



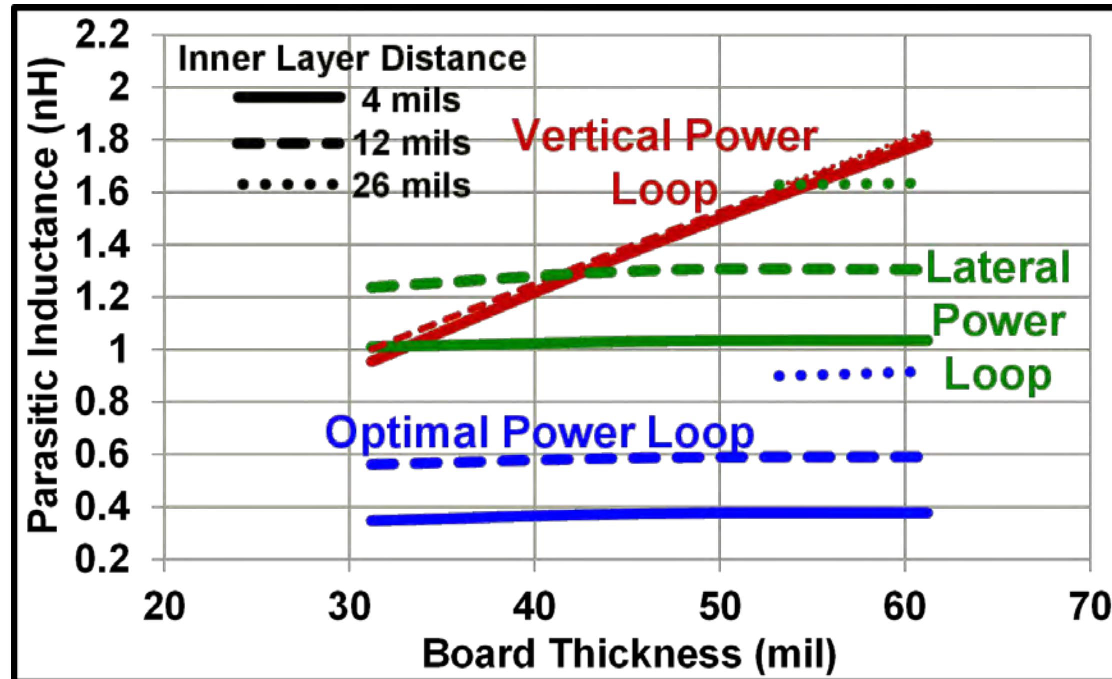
Side View

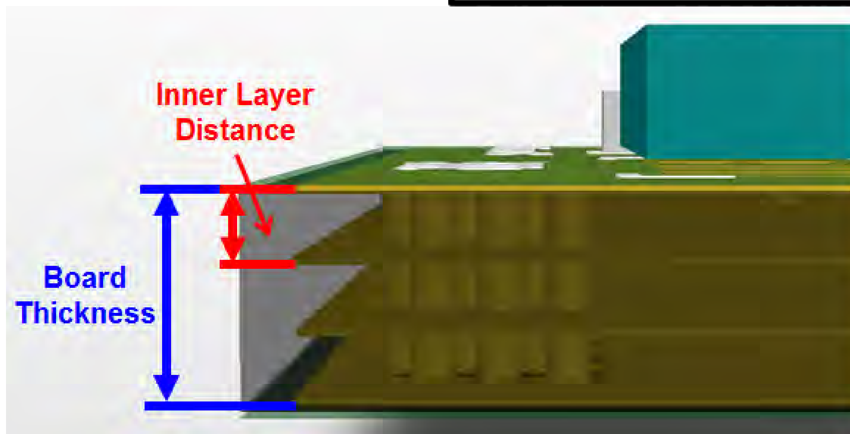




Top View
Inner Layer 1

Layout Inductance Comparison

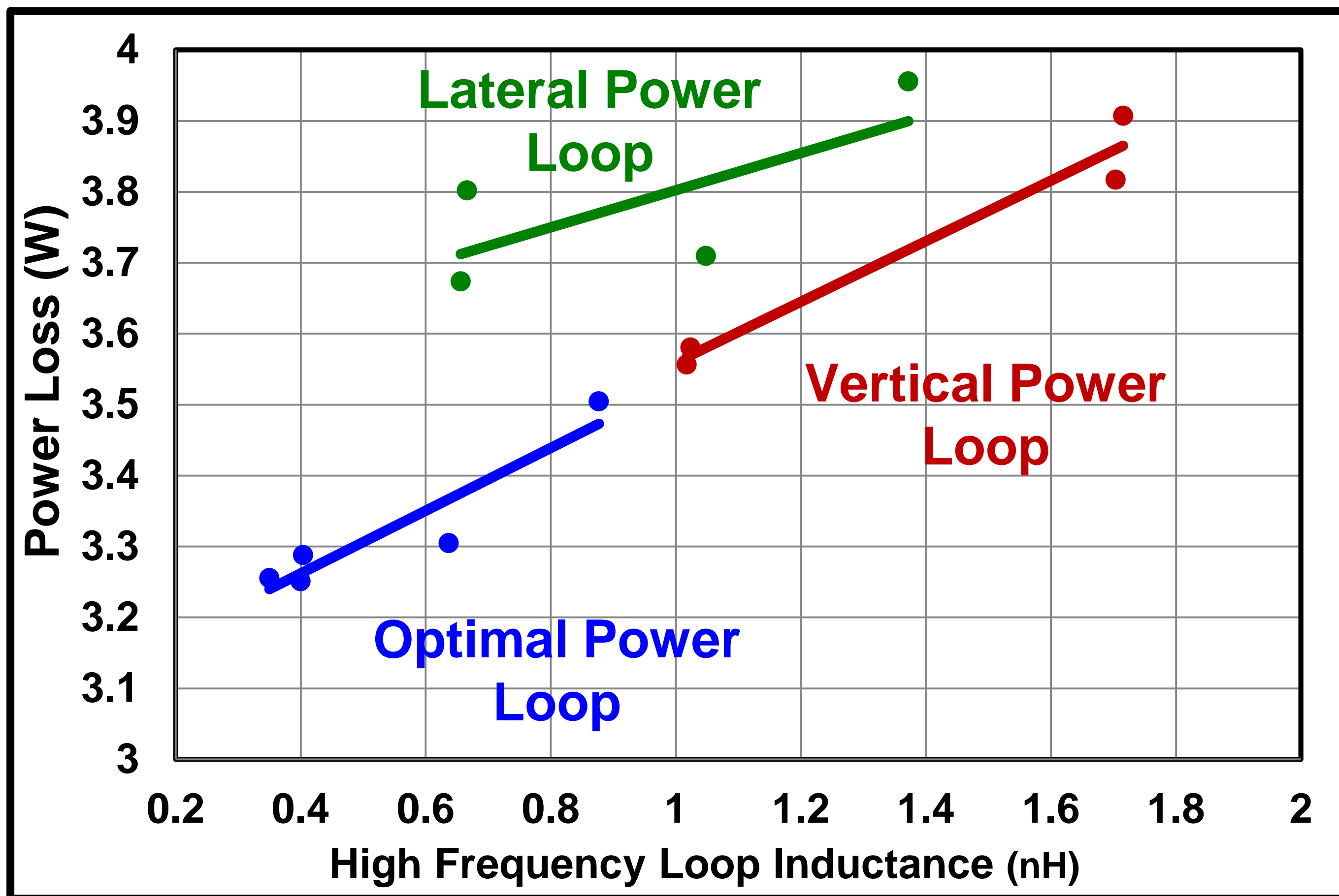




Test Cases

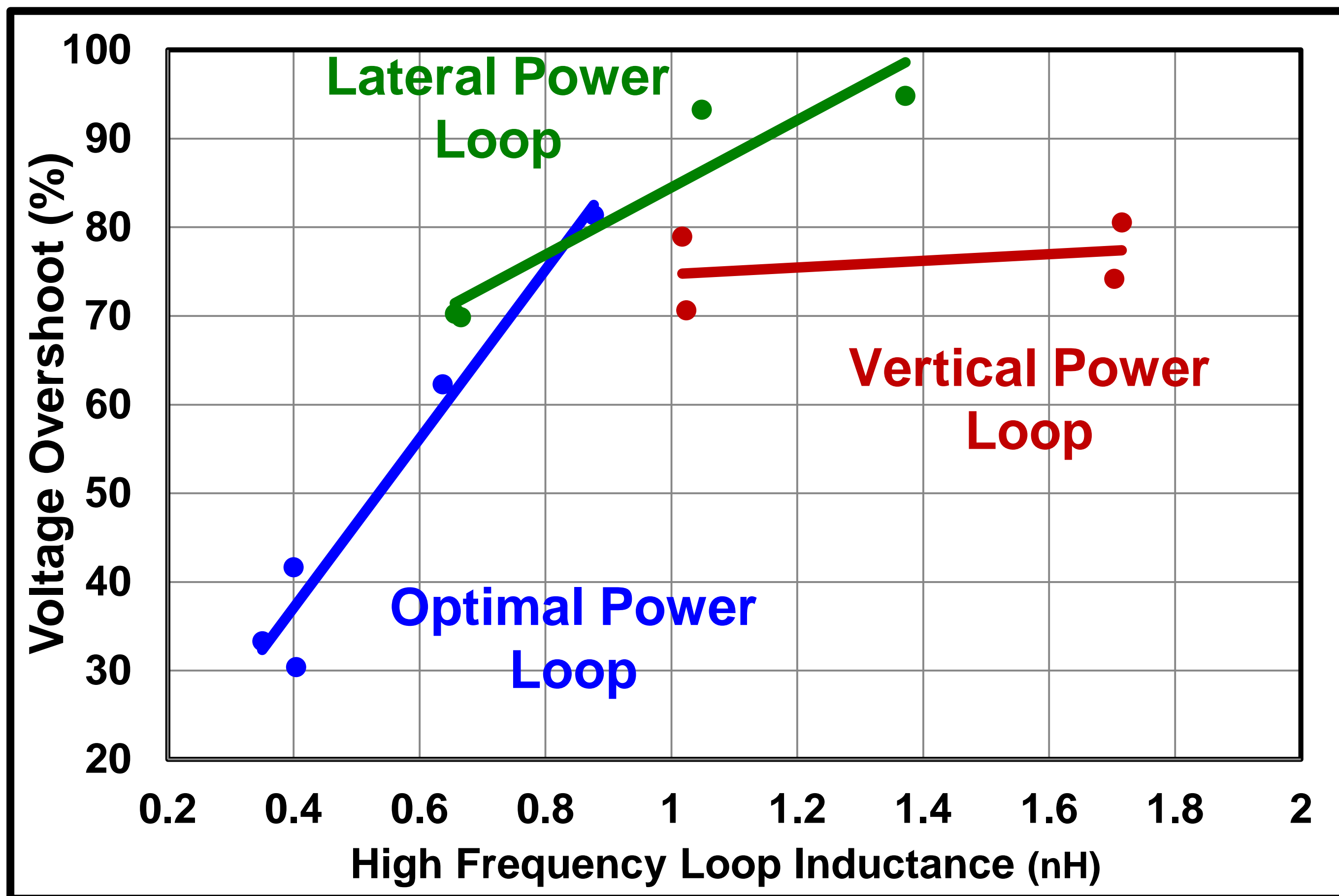
	Board Thickness (mils)	Inner Layer Distance (mils)
Design 1	31	4
Design 2	31	12
Design 3	62	4
Design 4	62	26

Power Loss Comparison



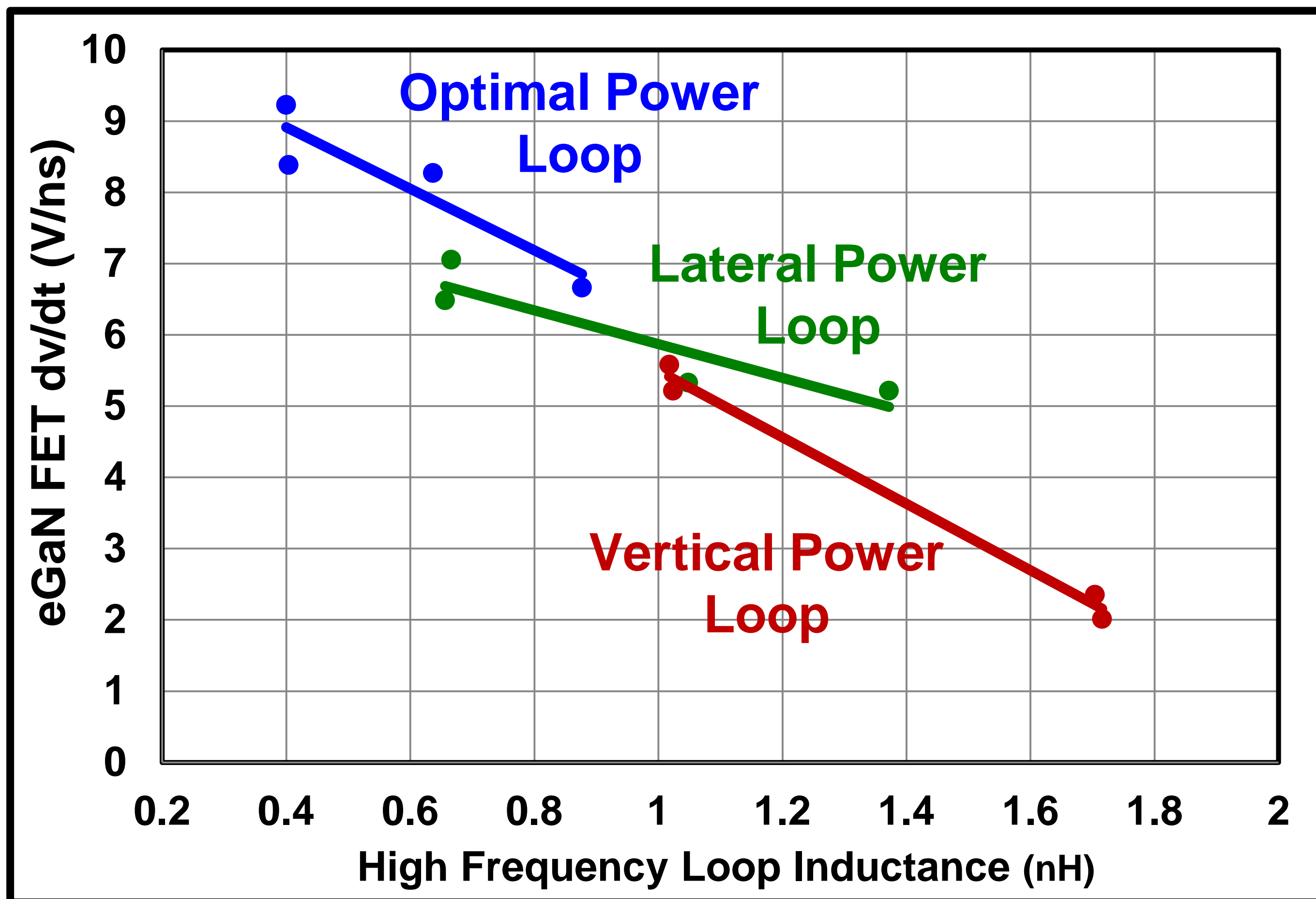
V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A f_{sw}=1 MHz L=300 nH
T/SR: EPC2015 Driver LM5113

Voltage Overshoot Comparison



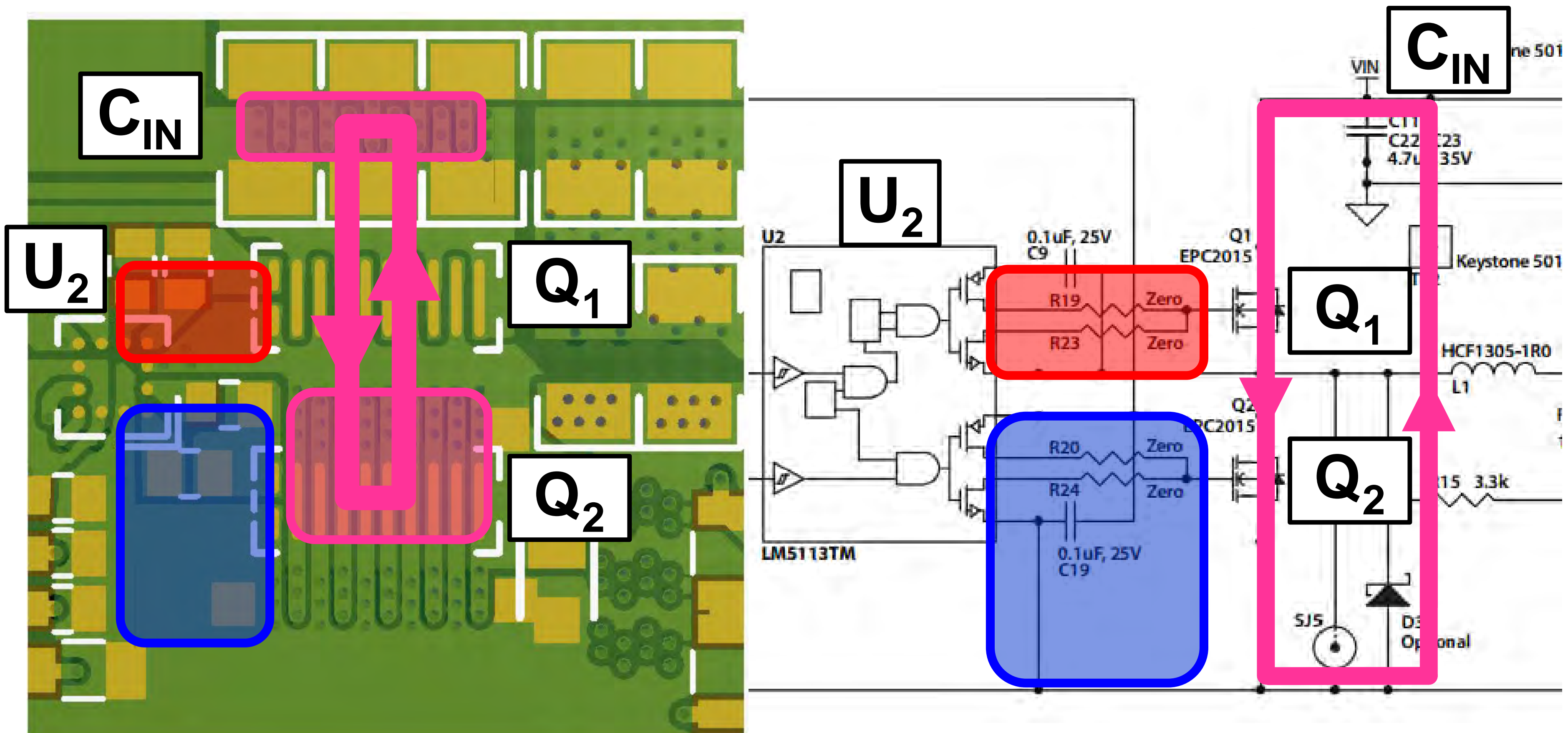
V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A f_{sw}=1 MHz L=300 nH
T/SR: EPC2015 Driver LM5113

Switching Speed Comparison



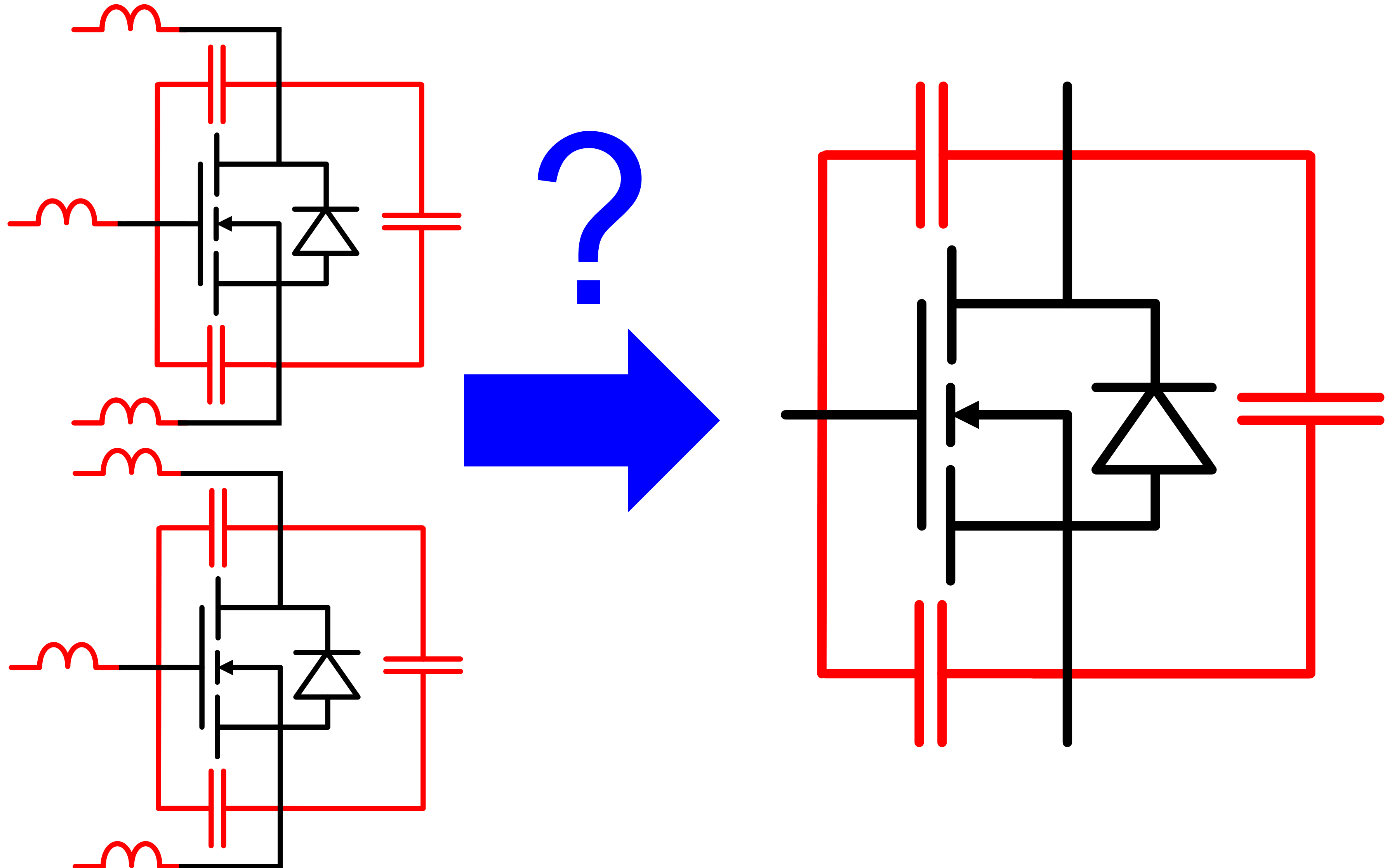
V_{IN}=12 V V_{OUT}=1.2 V I_{OUT}=20 A f_{sw}=1 MHz L=300 nH
T/SR: EPC2015 Driver LM5113

Optimal Layout Implementation

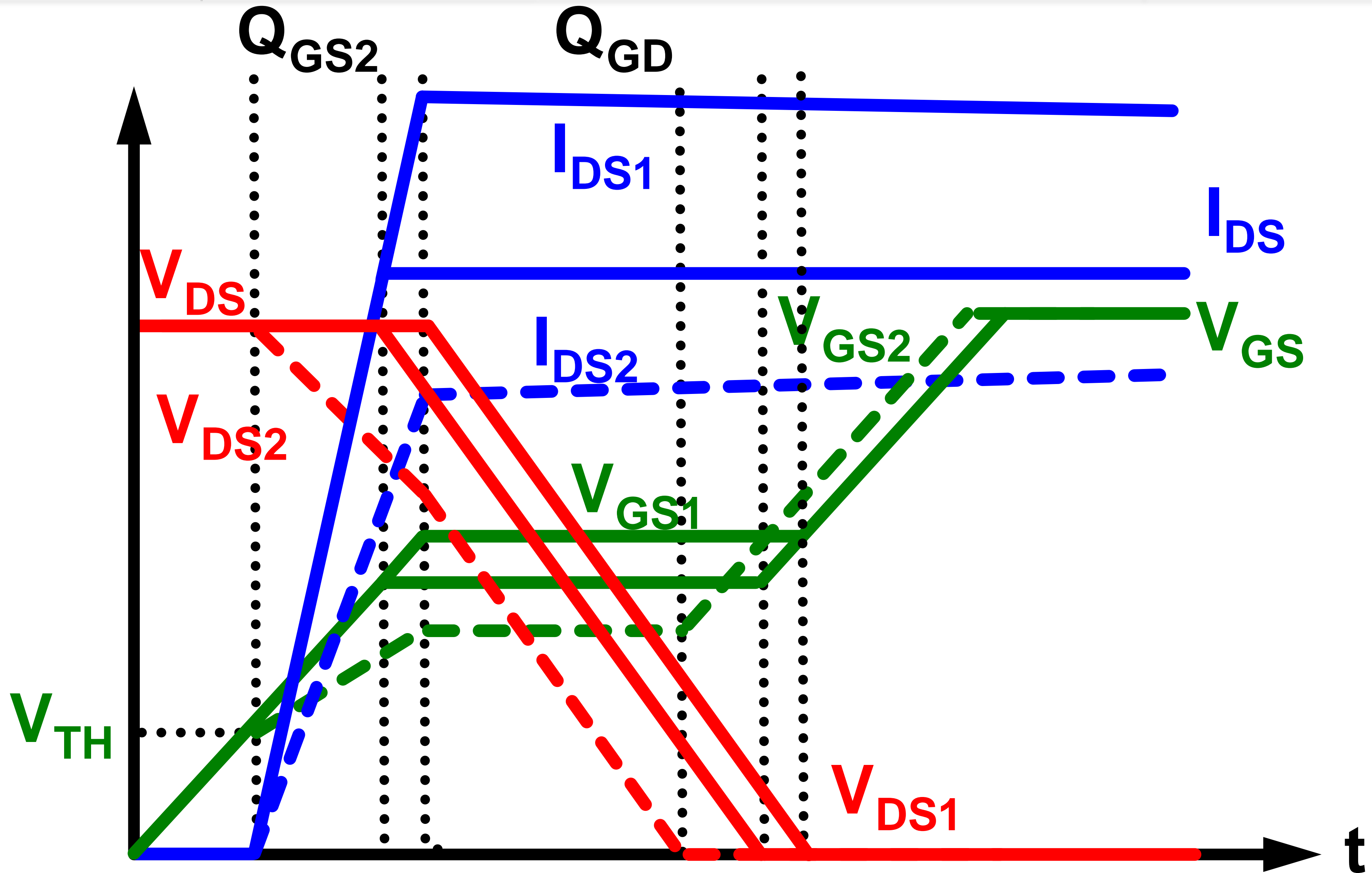


Paralleling

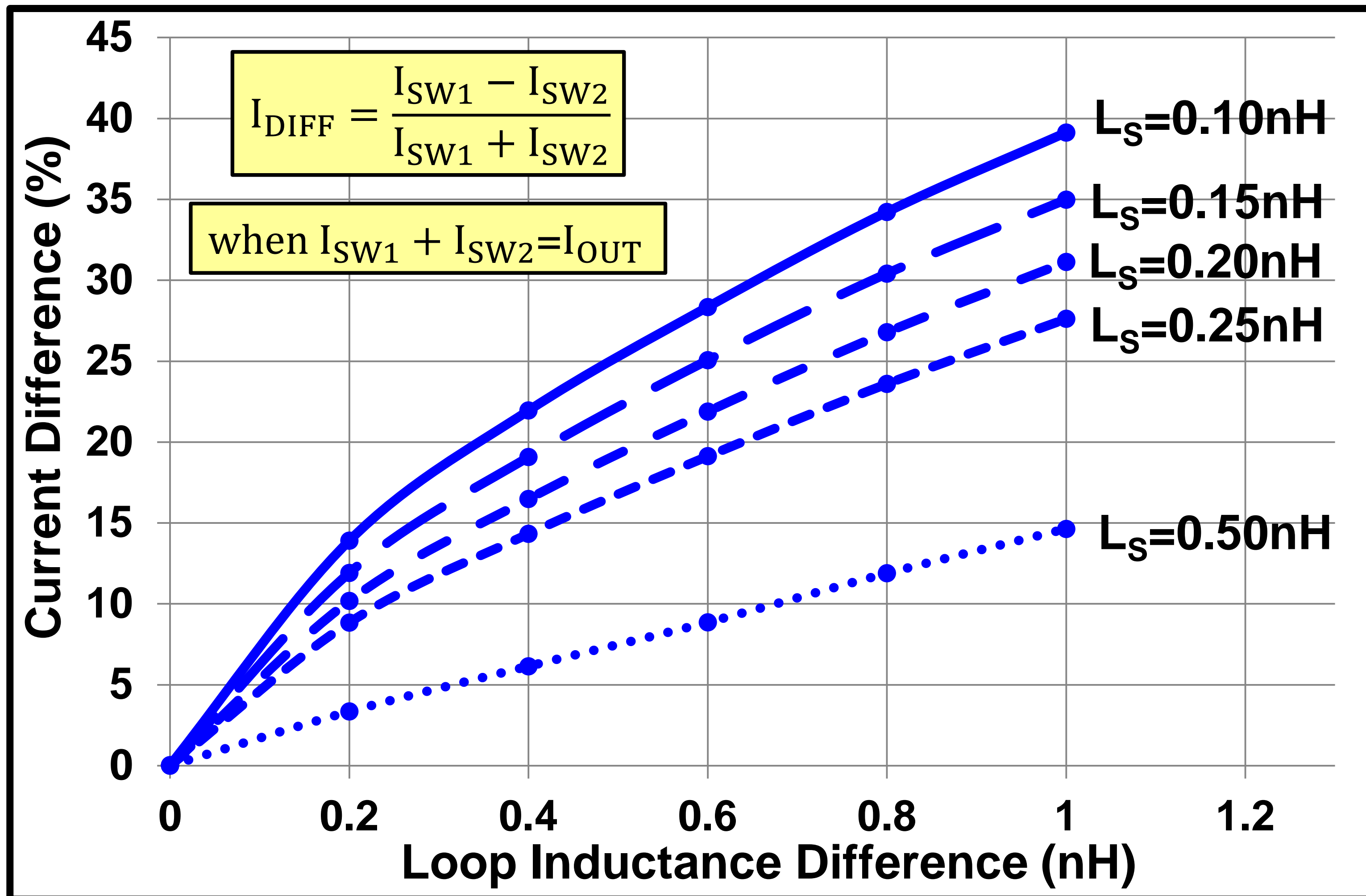
Parallel Power Devices



Parasitic Imbalance

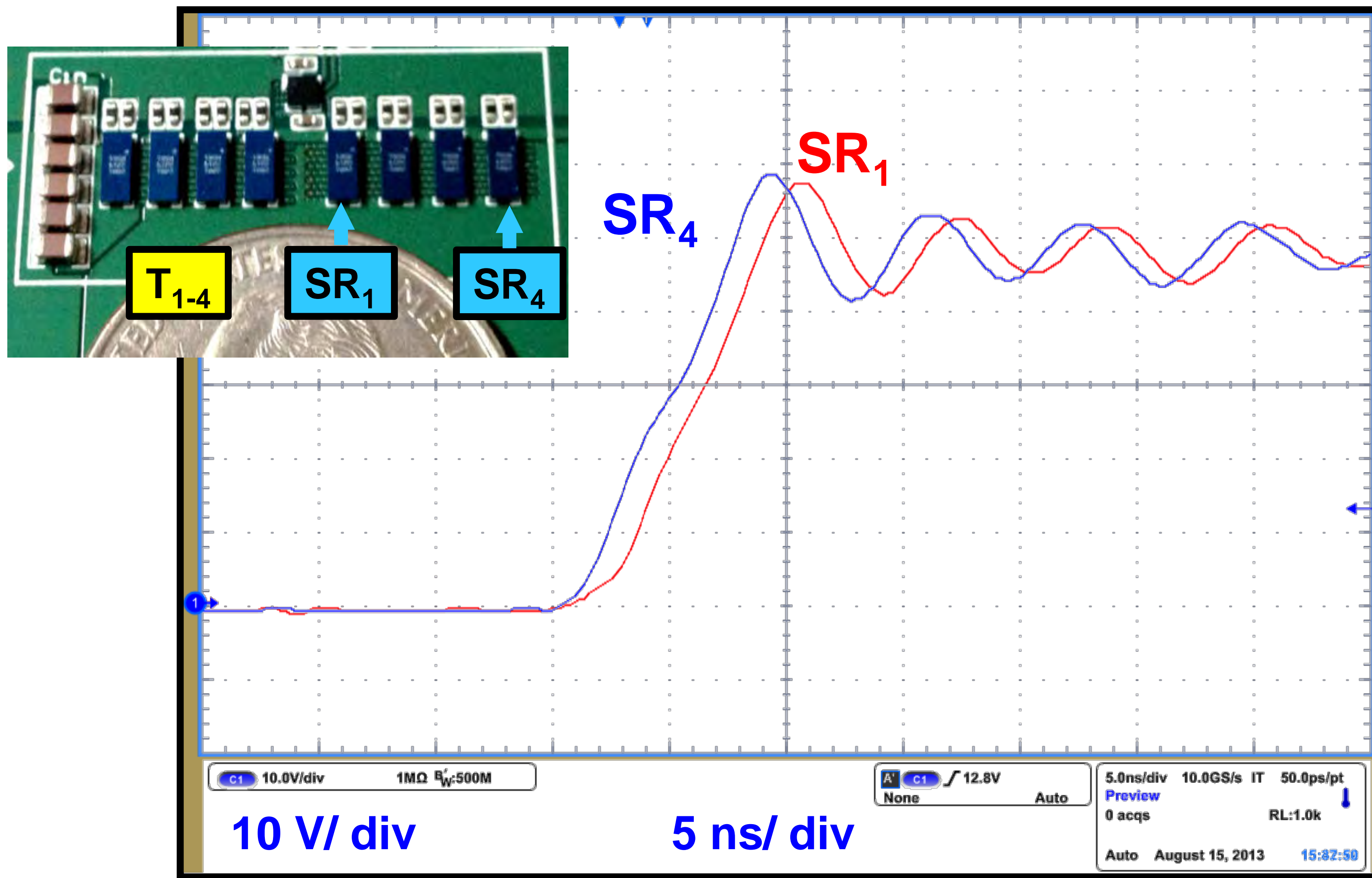


Loop Inductance Impact



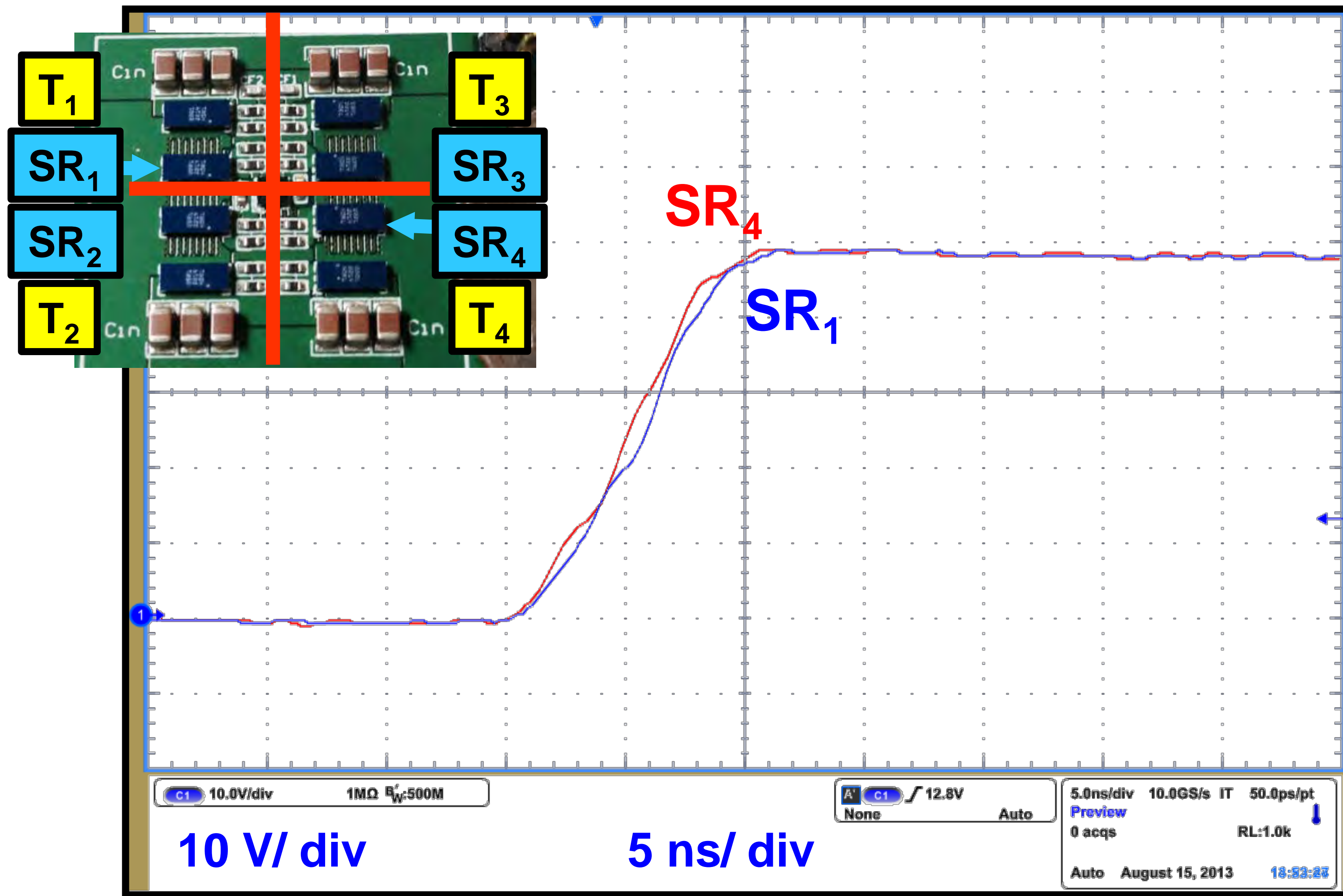
V_{IN}=48 V I_{OUT}=25 A eGaN FET T/SR: 100 V EPC2001
Nominal Drain Inductance $L_D = L_{LOOP} - L_S$=0.3 nH

Conventional Parallel Layout



V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 μH GaN FET T/SR: 100 V EPC2001

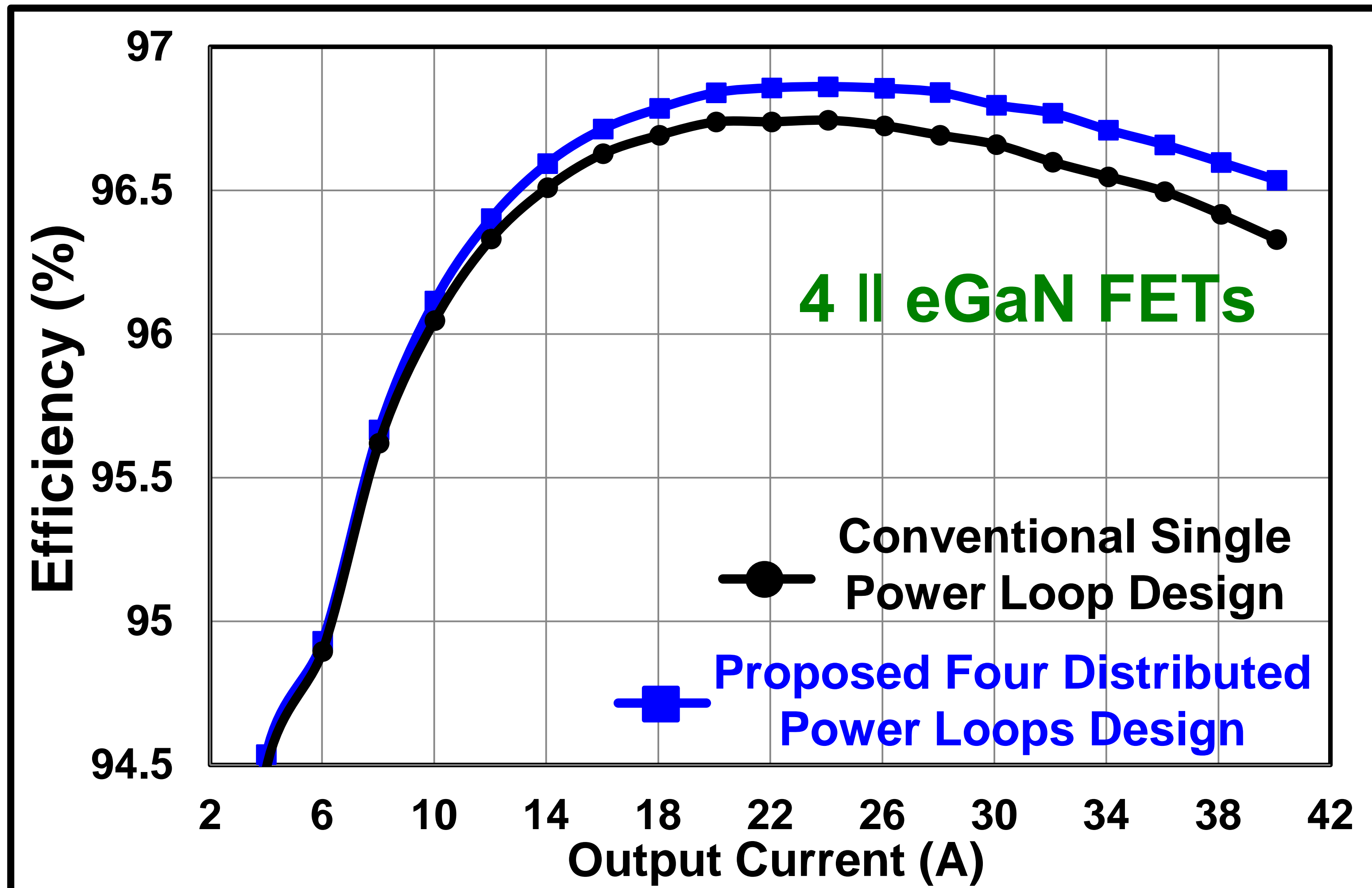
Optimal Parallel Layout



V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001

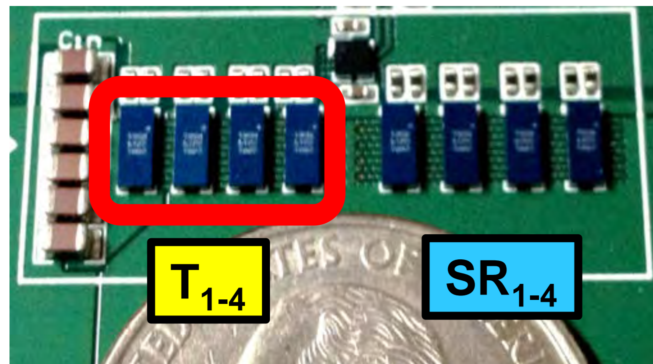
Reference: D. Reusch, J. Strydom, “Effectively Paralleling Gallium Nitride Transistors for High Current and High Frequency Applications,” APEC 2015

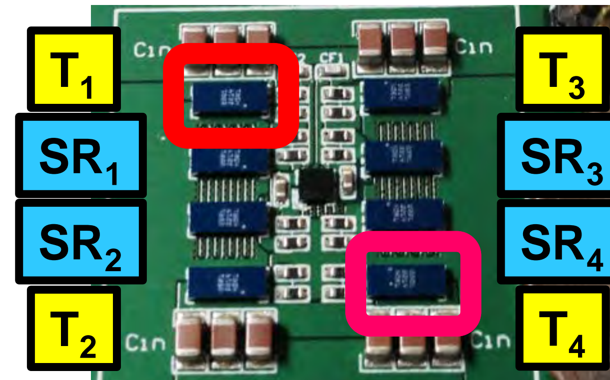
Parallel Layout Performance

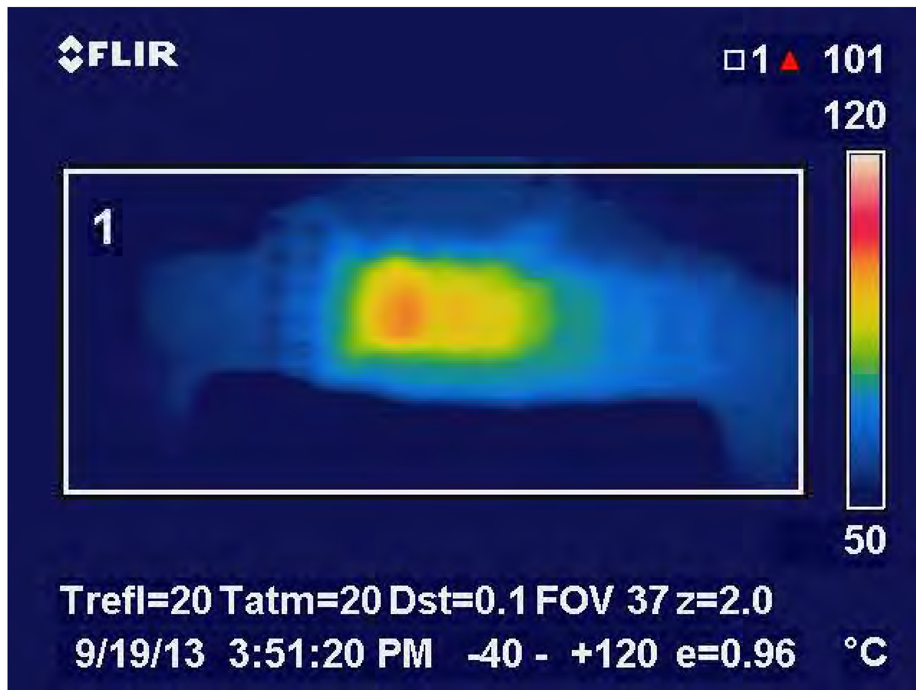


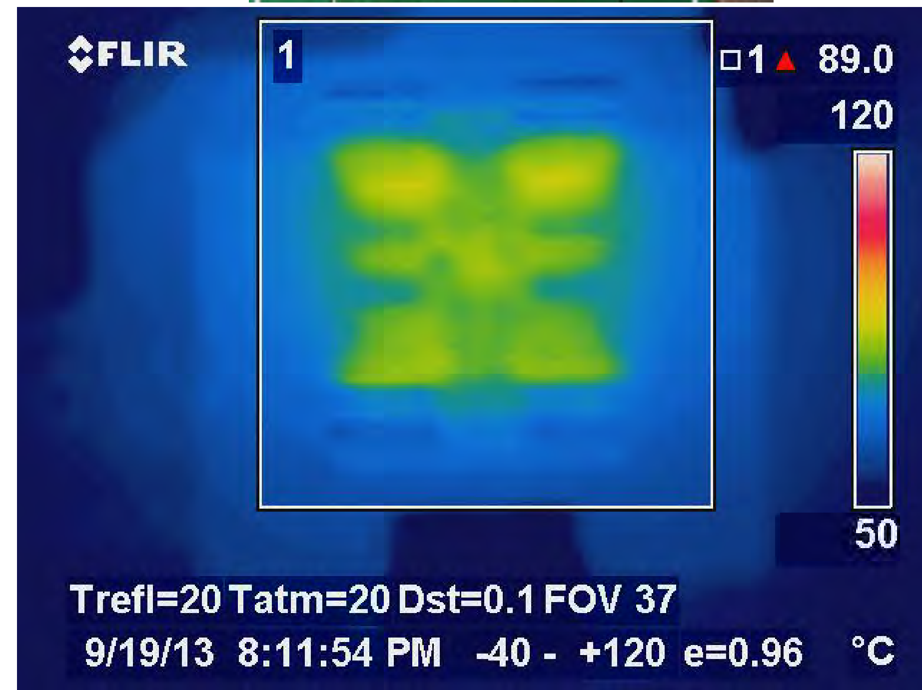
V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 4x100 V EPC2001
4 Layer 2 oz PCB

Parallel Layout Implementation



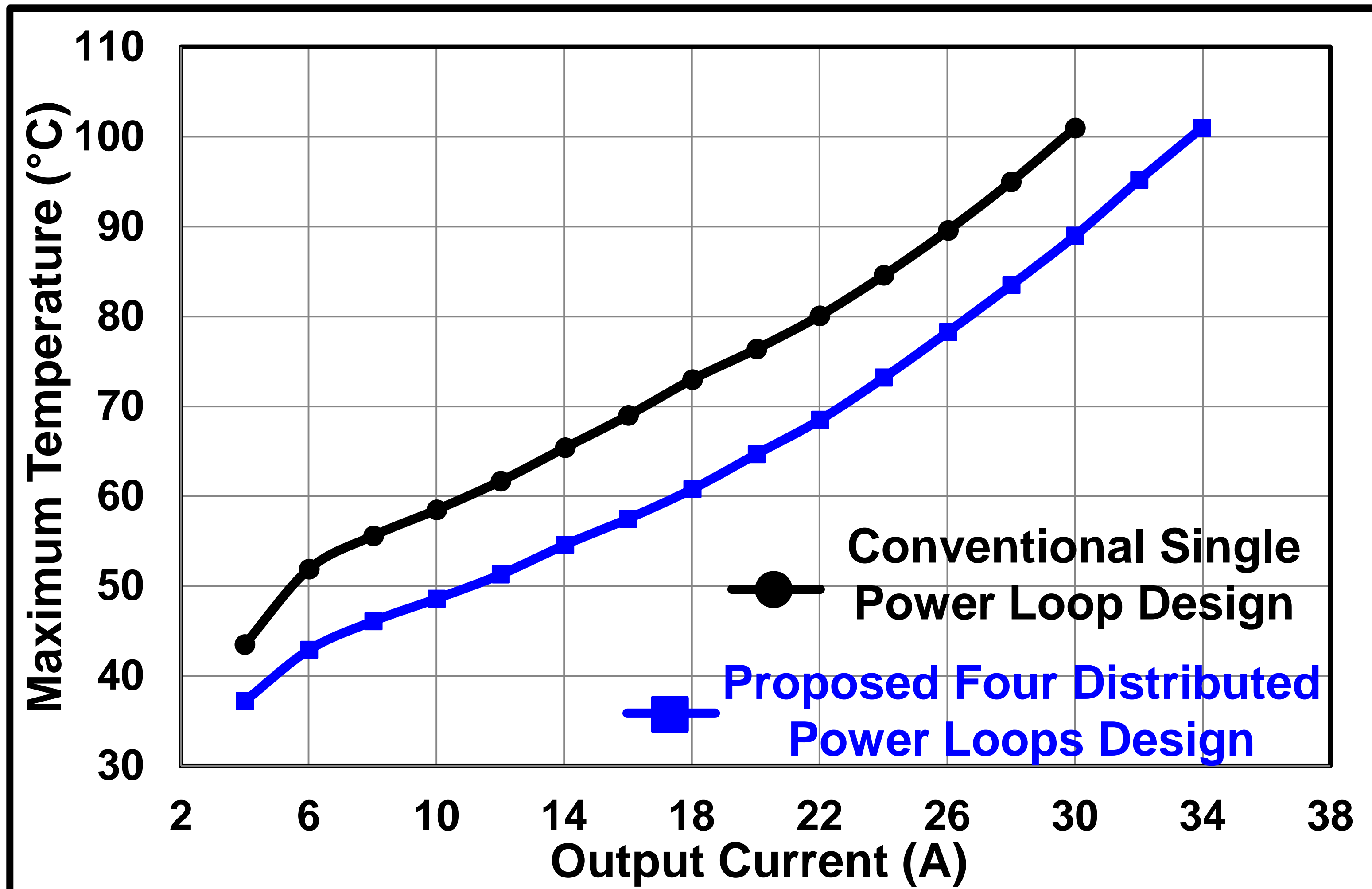






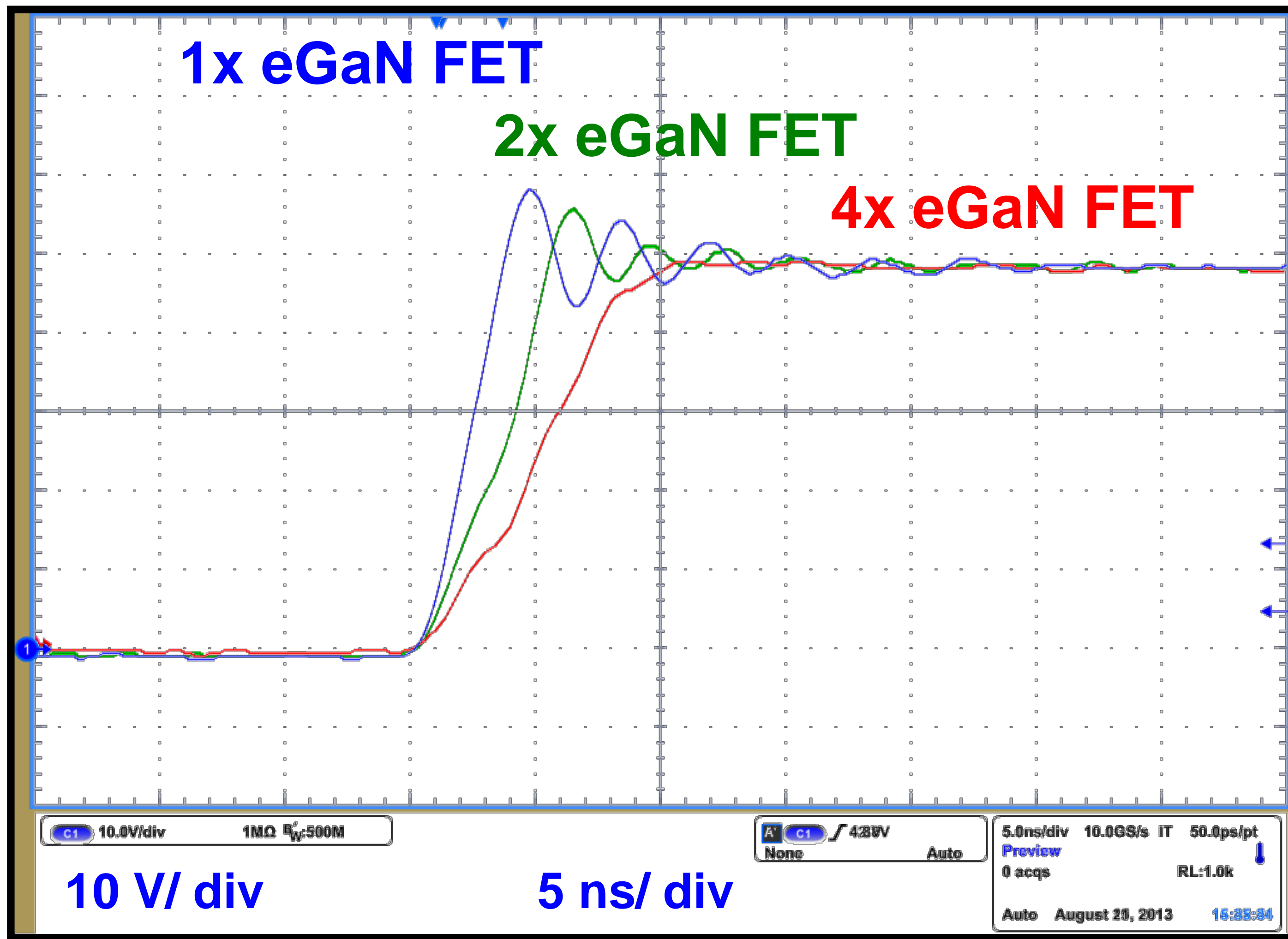
V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A f_{sw}=300 kHz L=3.3 μH GaN FET T/SR: 100 V EPC2001

Parallel Layout Performance



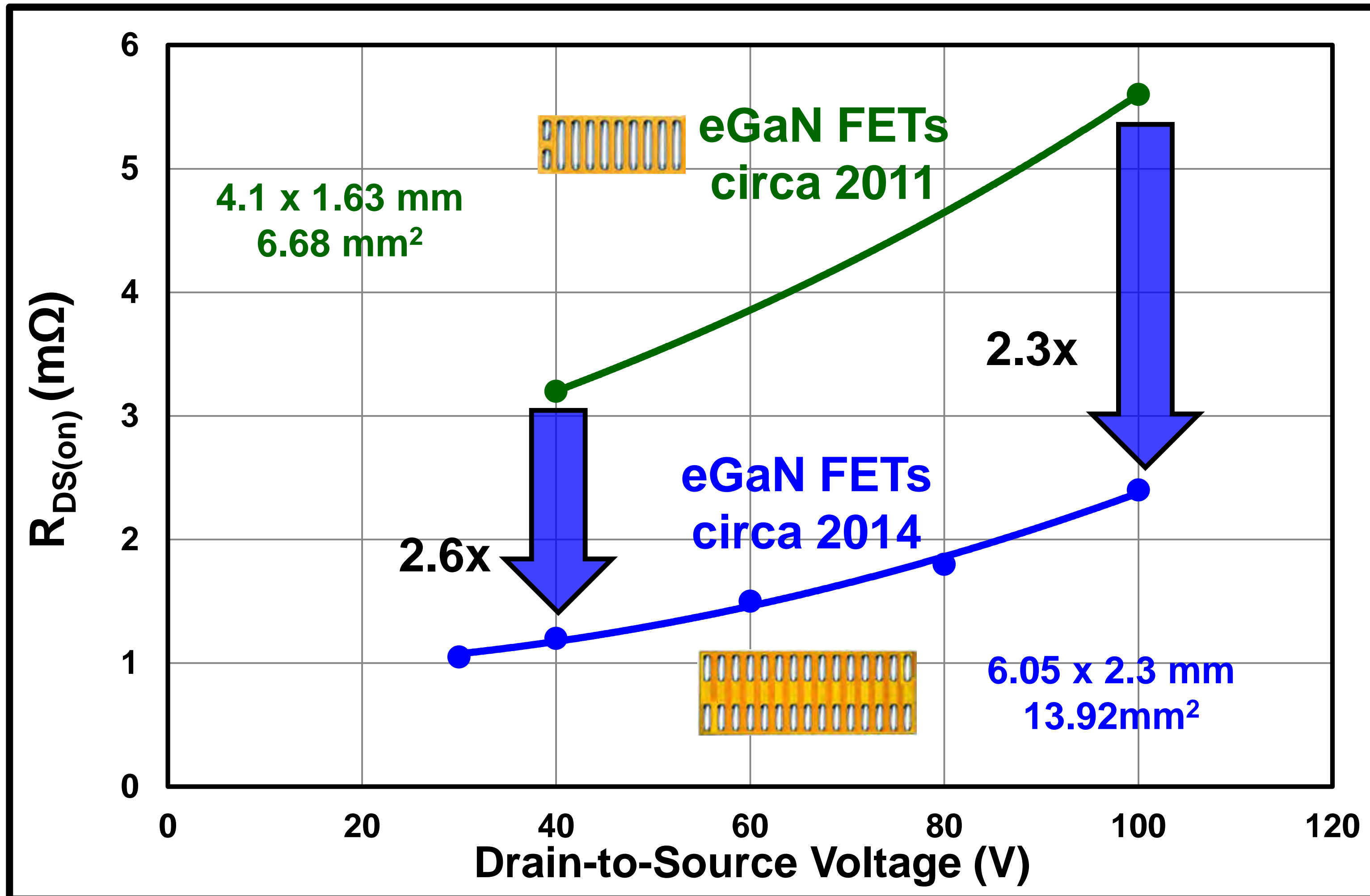
V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=3.3 µH GaN FET T/SR: 100 V EPC2001
Fan Speed 200 LFM 4 Layer 2 oz PCB

Parallel eGaN FET Swithcing

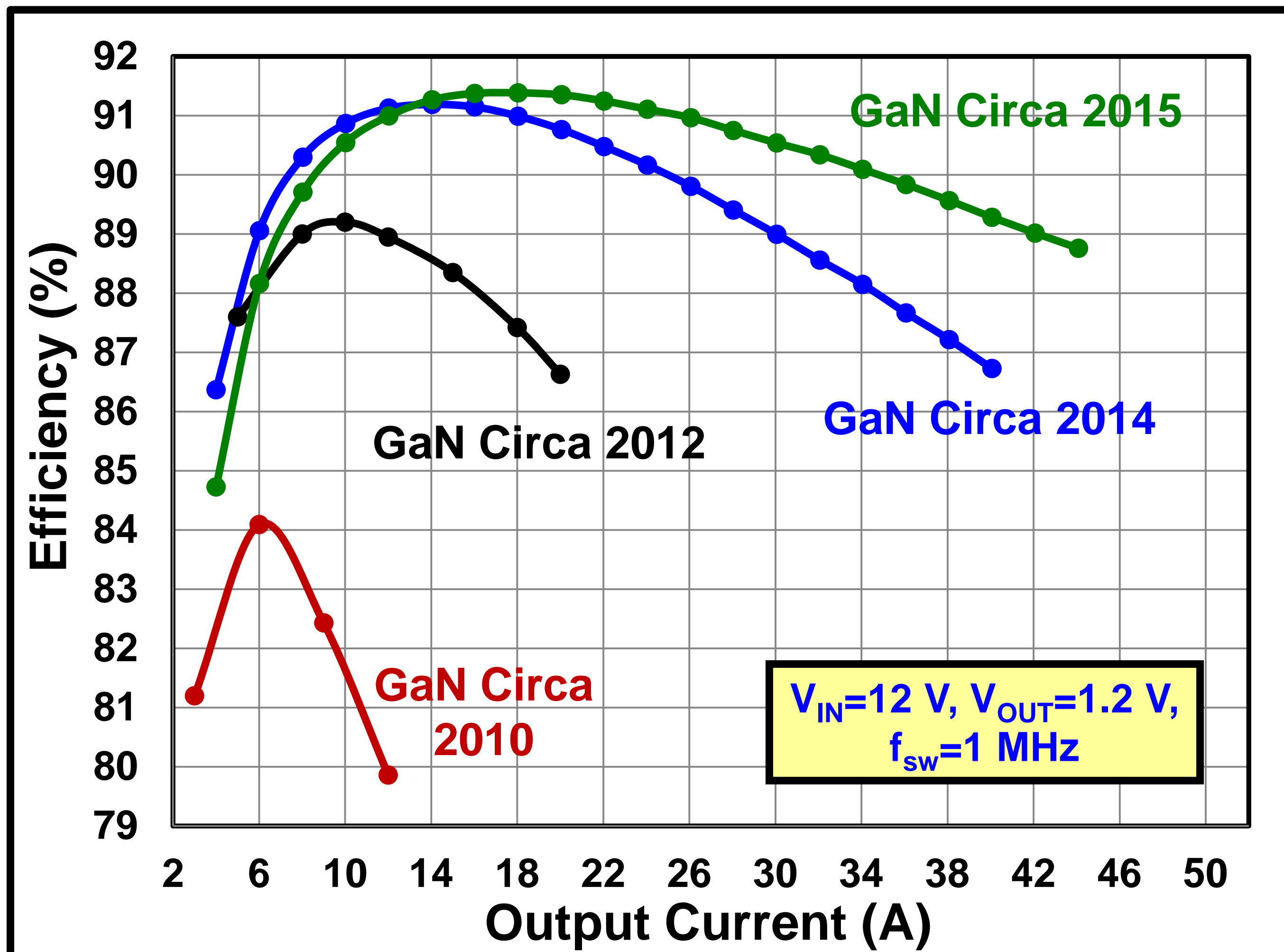


V_{IN}=48 V V_{OUT}=12 V I_{OUT}=30 A/ number of devices f_{sw}=300 kHz GaN FET T/SR: 100 V EPC2001

Further Increasing Current



V_{GS}=5 V


Efficiency (%)
92
91
90
89
88
87
86
85
84
83
82
81
80
79
2
6
10
14
18
22
26
30
34
38
42
46
50
Output Current (A)
GaN Circa 2015
GaN Circa 2014
GaN Circa 2012
GaN Circa 2010
V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz

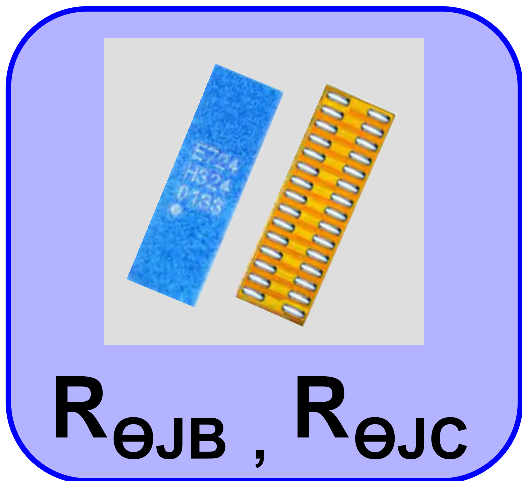
Thermal

Thermal Modeling

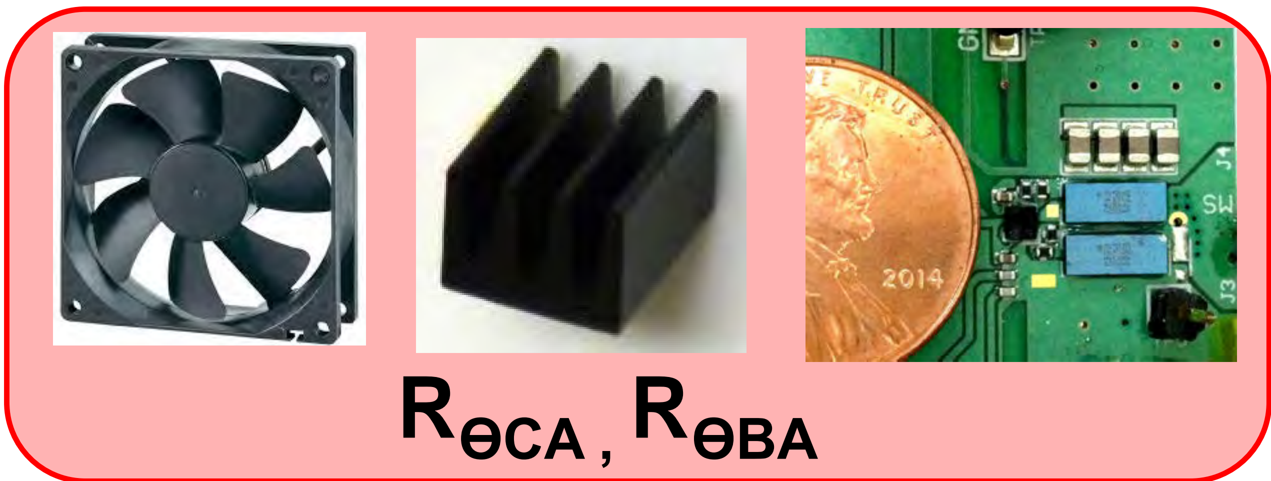
$R_{\theta JC}$ $R_{\theta CA}$ T_J T_A $R_{\theta JB}$ $R_{\theta BA}$ P_{LOSS} T_A

$R_{\theta JA}$ T_J T_A P_{LOSS} T_A

$$P_{MAX} = \frac{T_{JMAX} - T_A}{R_{JA}}$$

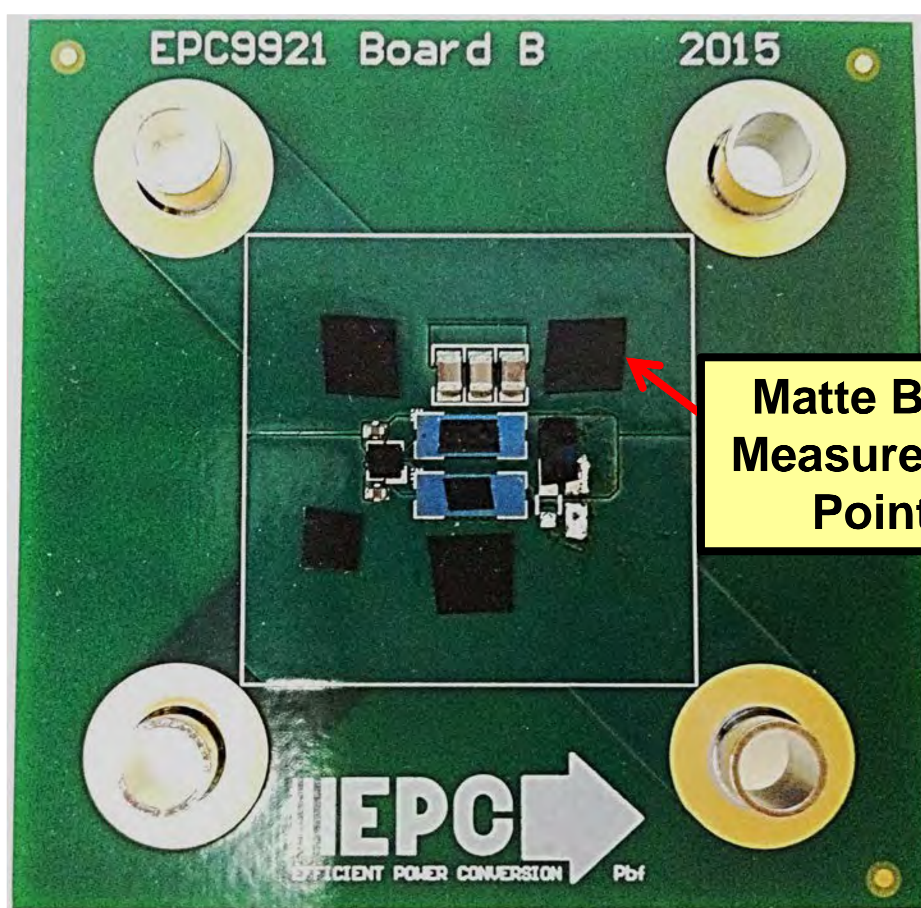


$R_{\theta JB}$, $R_{\theta JC}$

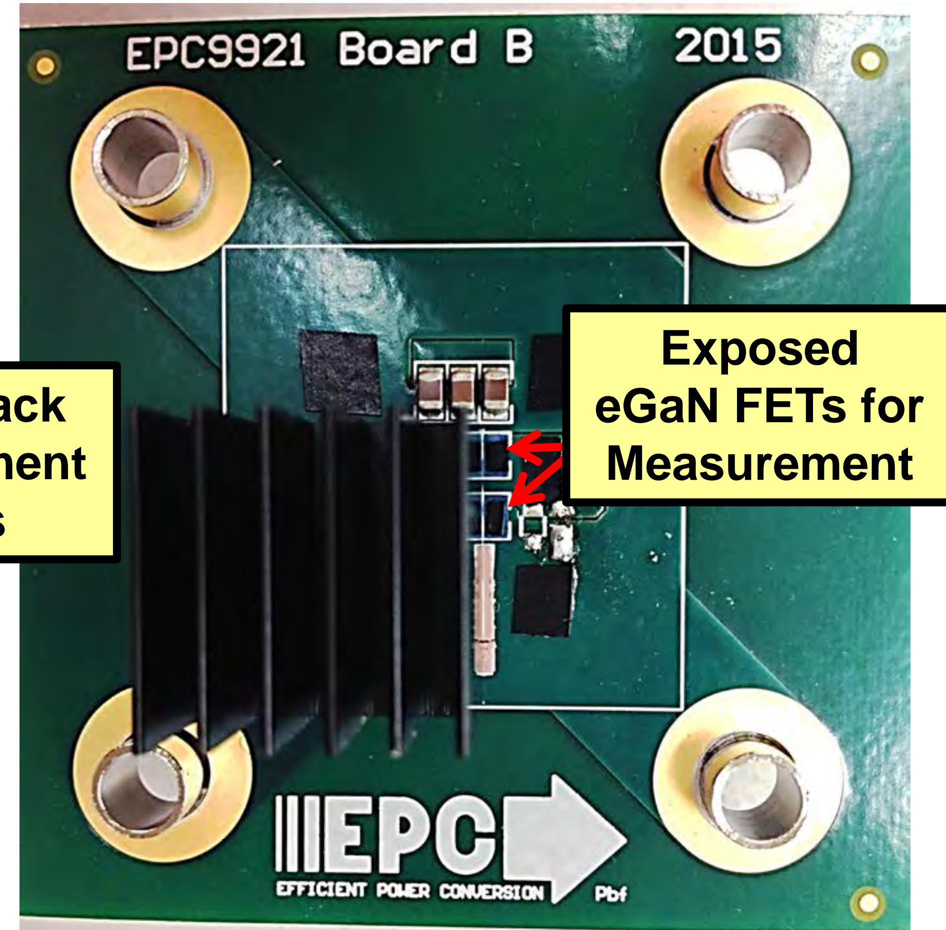


$R_{\theta CA}$, $R_{\theta BA}$

Thermal Evaluation Boards

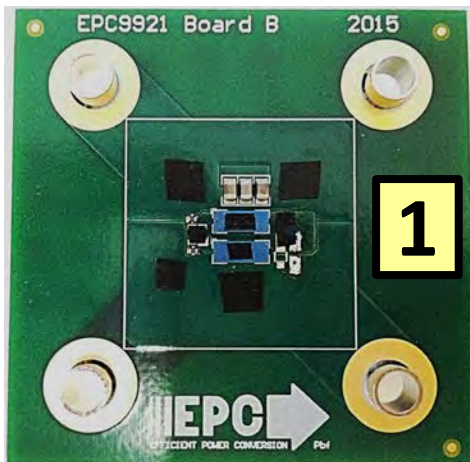


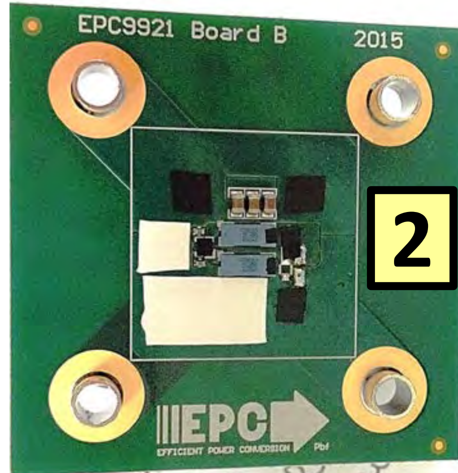
1x1 inch Buck Converter
4 Layers 2oz Copper



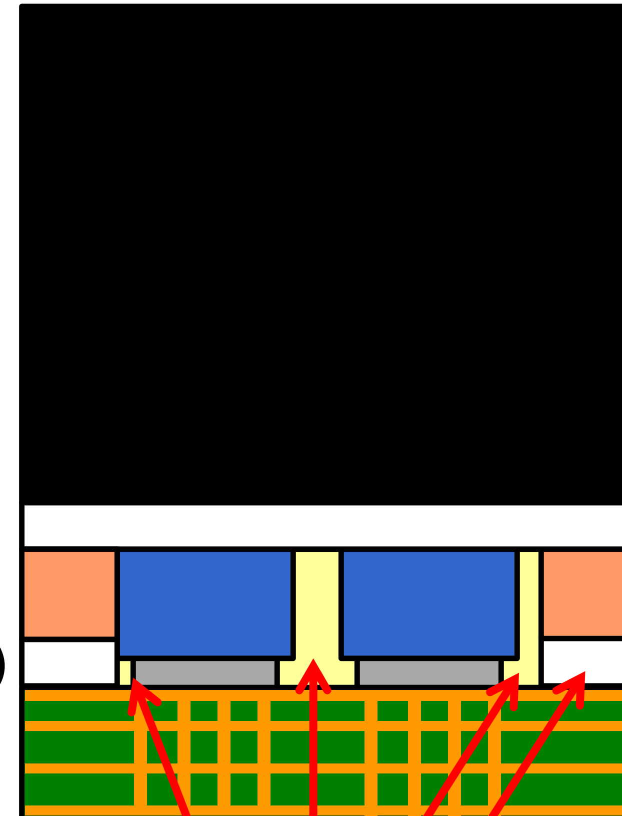
15x15x14.5 mm
Heat Sink

Heat Sink Attachment





Heat Sink (4)

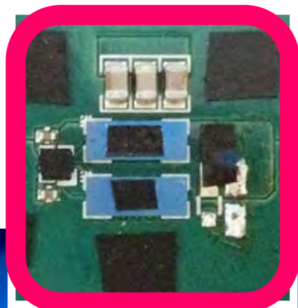


Thermal Tape (4)
Gap Pad (3)
Thermal Tape (2)
PCB (1)
TIM (Optional)

APEC

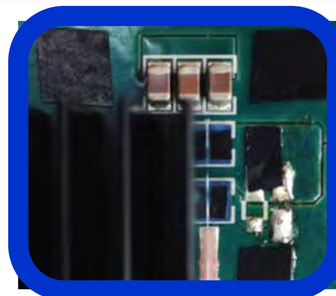
Thermal Comparison

EPC EFFICIENT POWER CONVERSION



Q1 ≈ 98°C

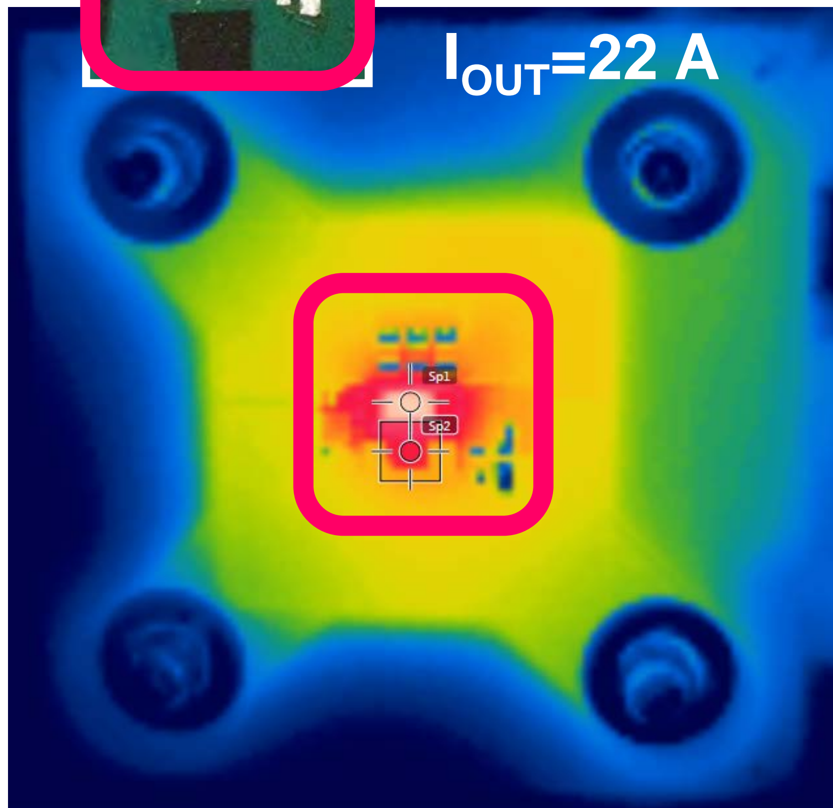
Q2 ≈ 84°C

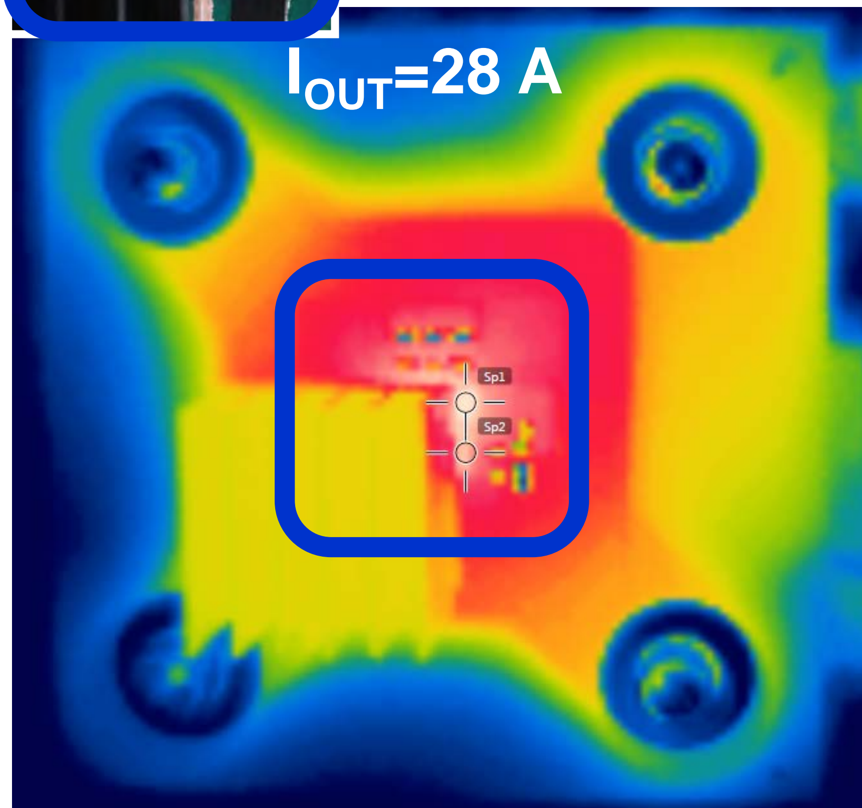


Q1 ≈ 102°C

Q2 ≈ 92°C

100°C

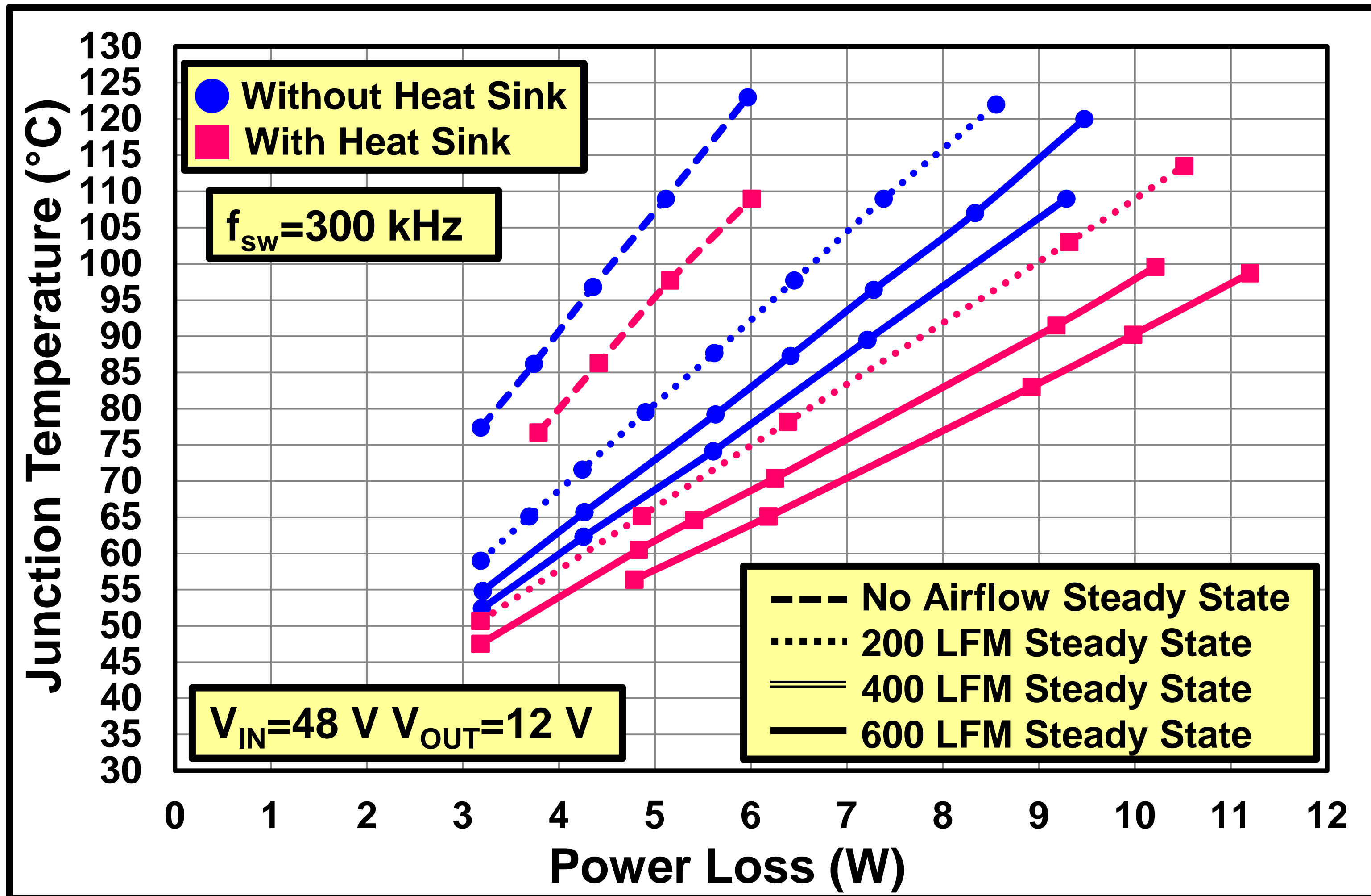




25°C

Devices 80 V EPC2021 Fan Speed=200 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

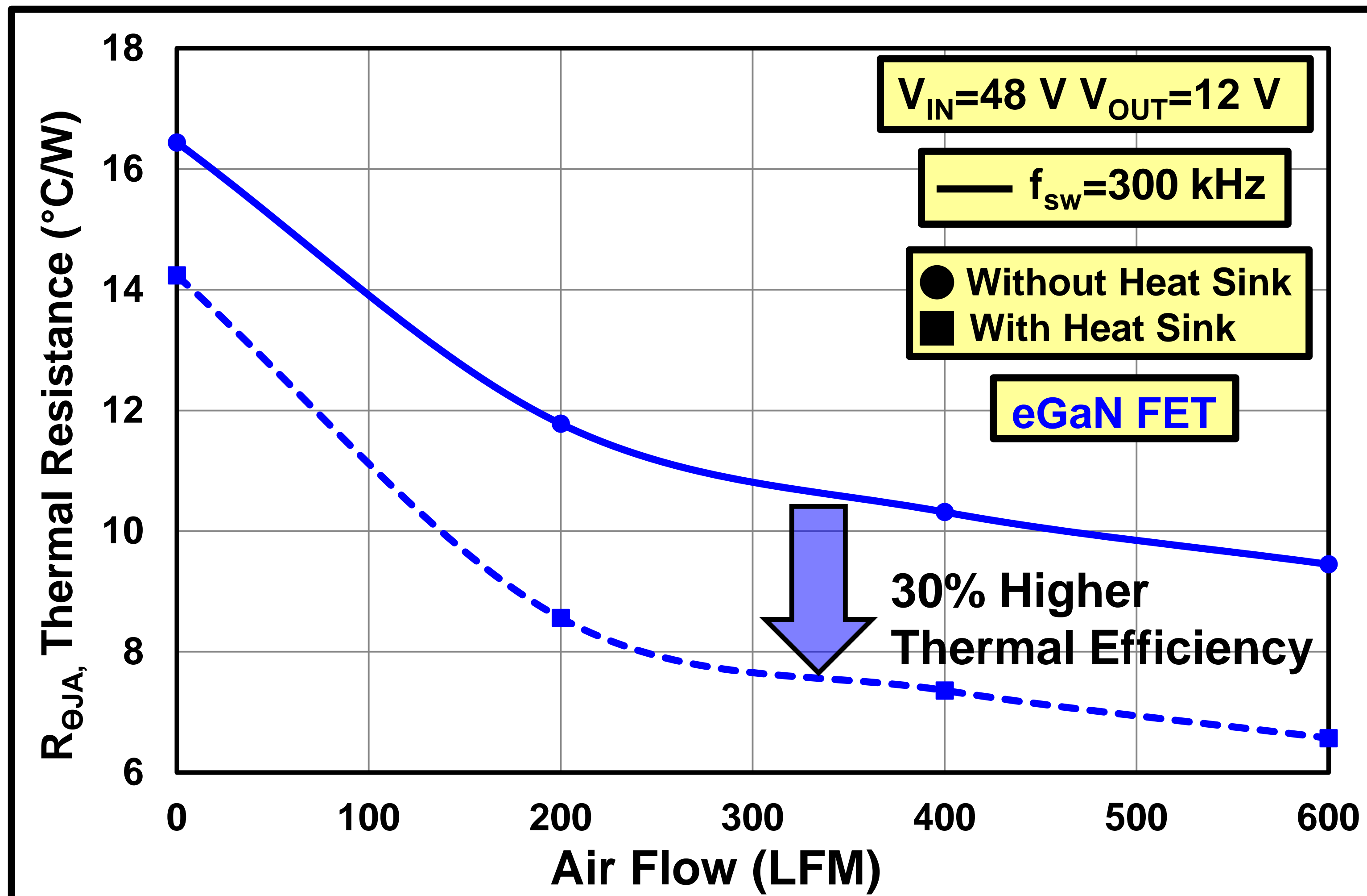
Improved Thermal Management



APEC

Impact of Heat Sink

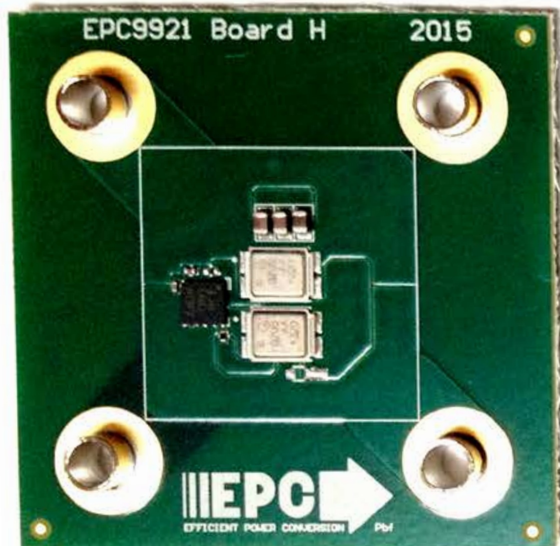
EPC EFFICIENT POWER CONVERSION



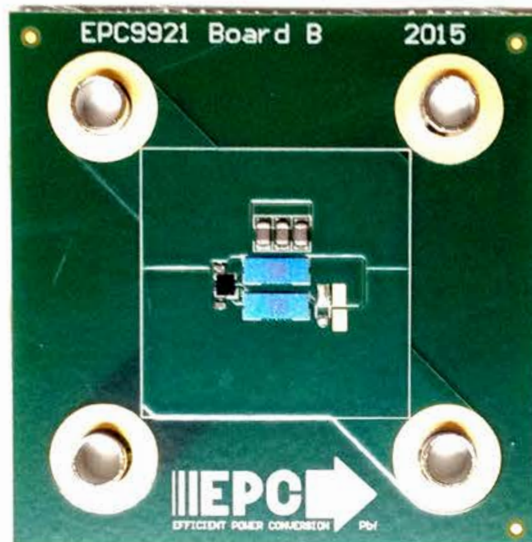
48 V Non-Isolated Buck Converter

48 V Evaluation Boards

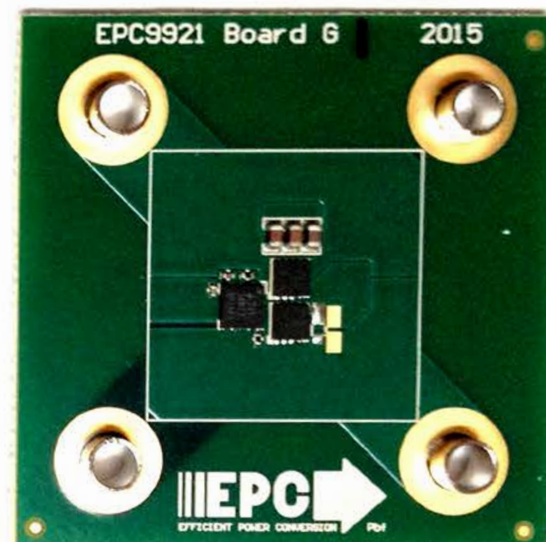
80 V 3.7 mΩ CanPAK MOSFET	80 V 1.8 mΩ LGA eGaN FET	80 V 6.8 mΩ S308 MOSFET



Active Area ≈150 mm²

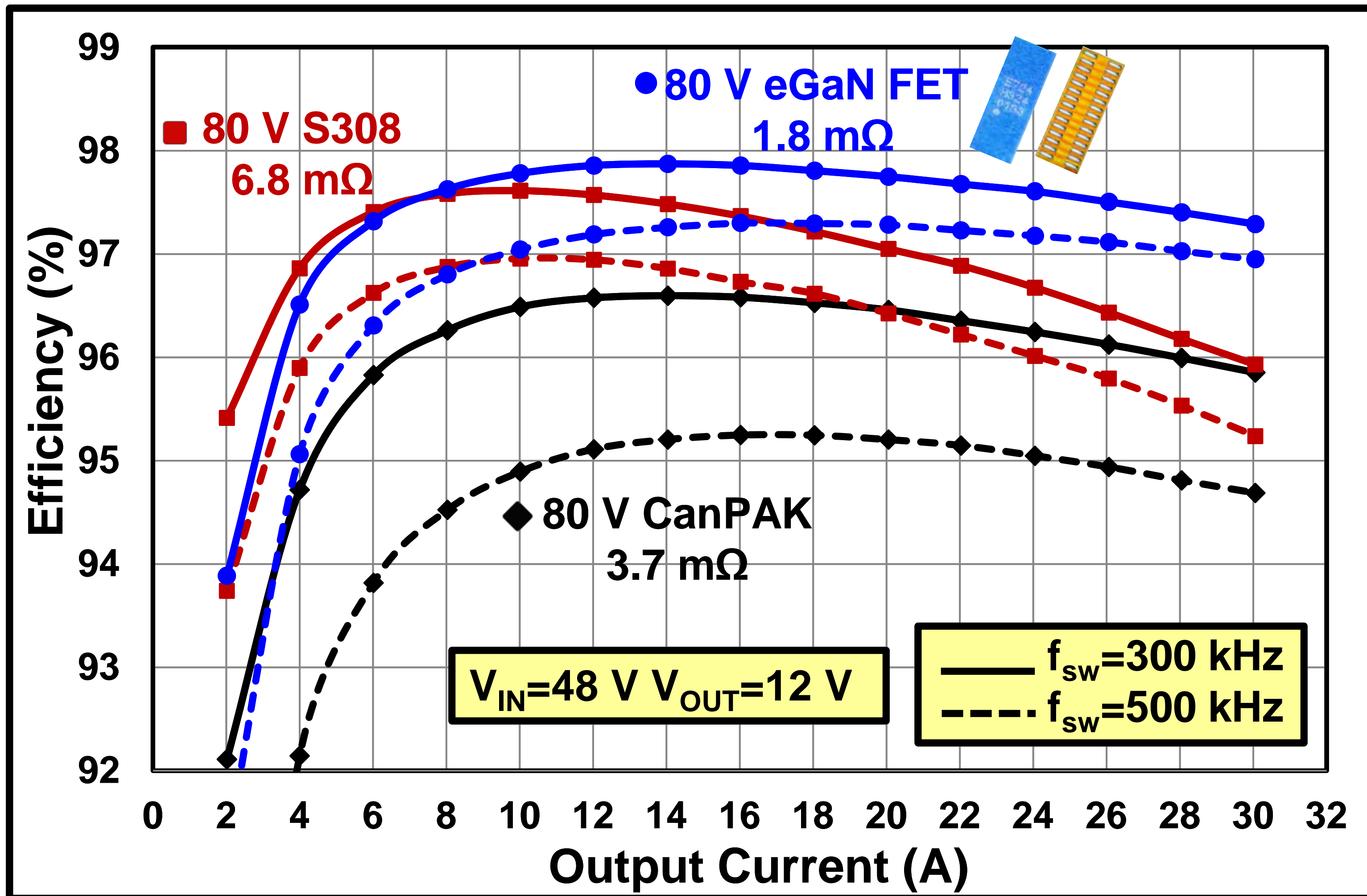


Active Area ≈60 mm²

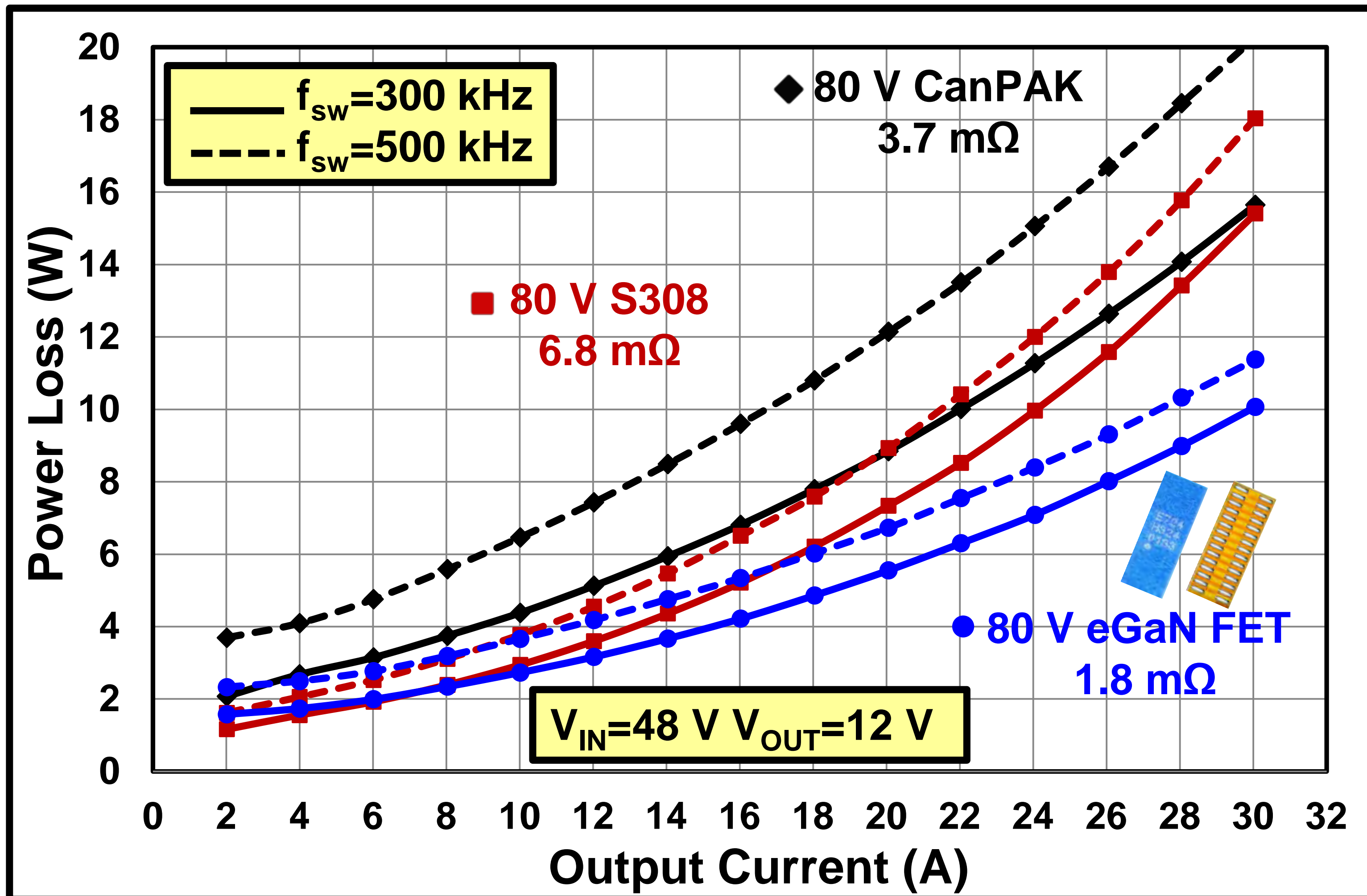


Active Area ≈132 mm²

Efficiency Comparisons



Power Loss Comparison



eGaN FET and S308 MOSFET

Q1 ≈ 72°C

Q2 ≈ 61°C

100°C

100.0°C

I_{OUT}=16 A

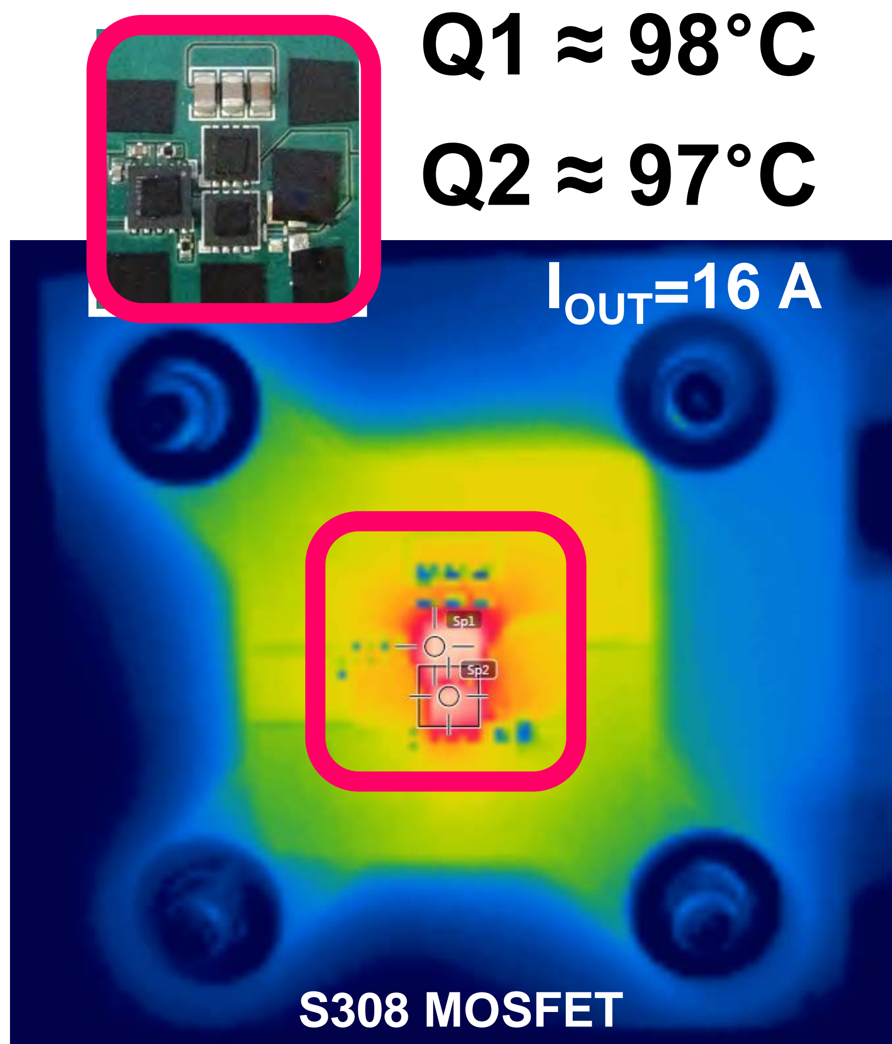
Sp1

Sp2

25.0°C

eGaN FET

25°C



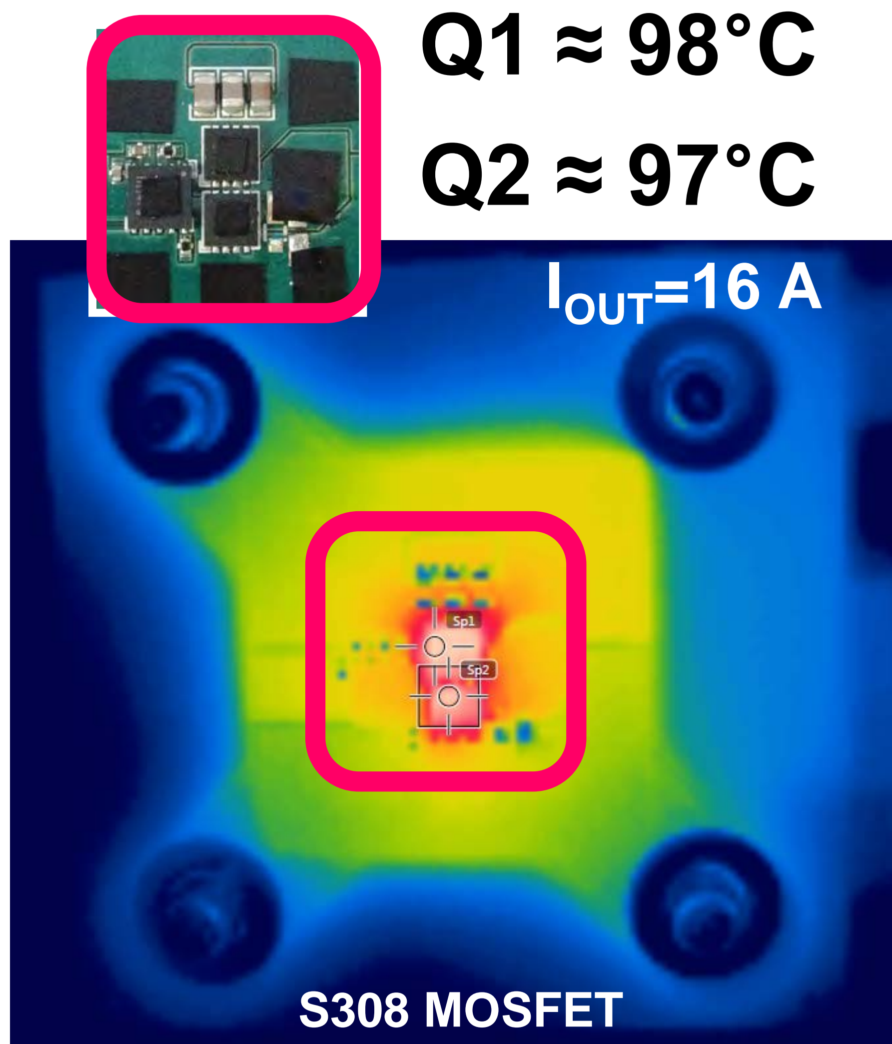
Fan Speed=200 LFM I_{OUT}=16 A V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

eGaN FET and S308 MOSFET

100°C

25°C

eGaN FET: Q1 ≈ 98°C, Q2 ≈ 84°C, I_{OUT}=22 A

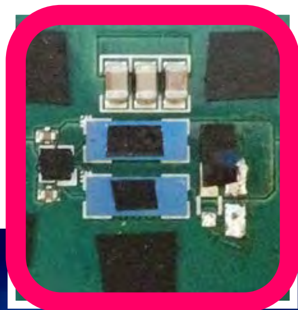


Fan Speed=200 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

eGaN FET and CanPAK MOSFET

100°C

25°C

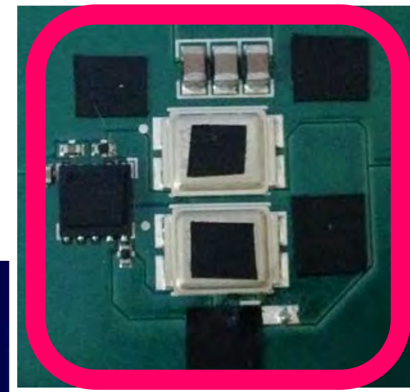


Q1 ≈ 65°C

Q2 ≈ 55°C

I_{OUT}=14 A

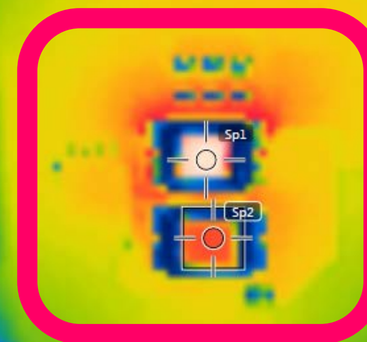
eGaN FET



Q1 ≈ 100°C

Q2 ≈ 80°C

I_{OUT}=14 A



Can PAK MOSFET

Fan Speed=200 LFM I_{OUT}=14 A V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 µH

eGaN FET and CanPAK MOSFET

Q1 ≈ 98°C

Q2 ≈ 84°C

I_{OUT}=22 A

eGaN FET

Q1 ≈ 100°C

Q2 ≈ 80°C

I_{OUT}=14 A

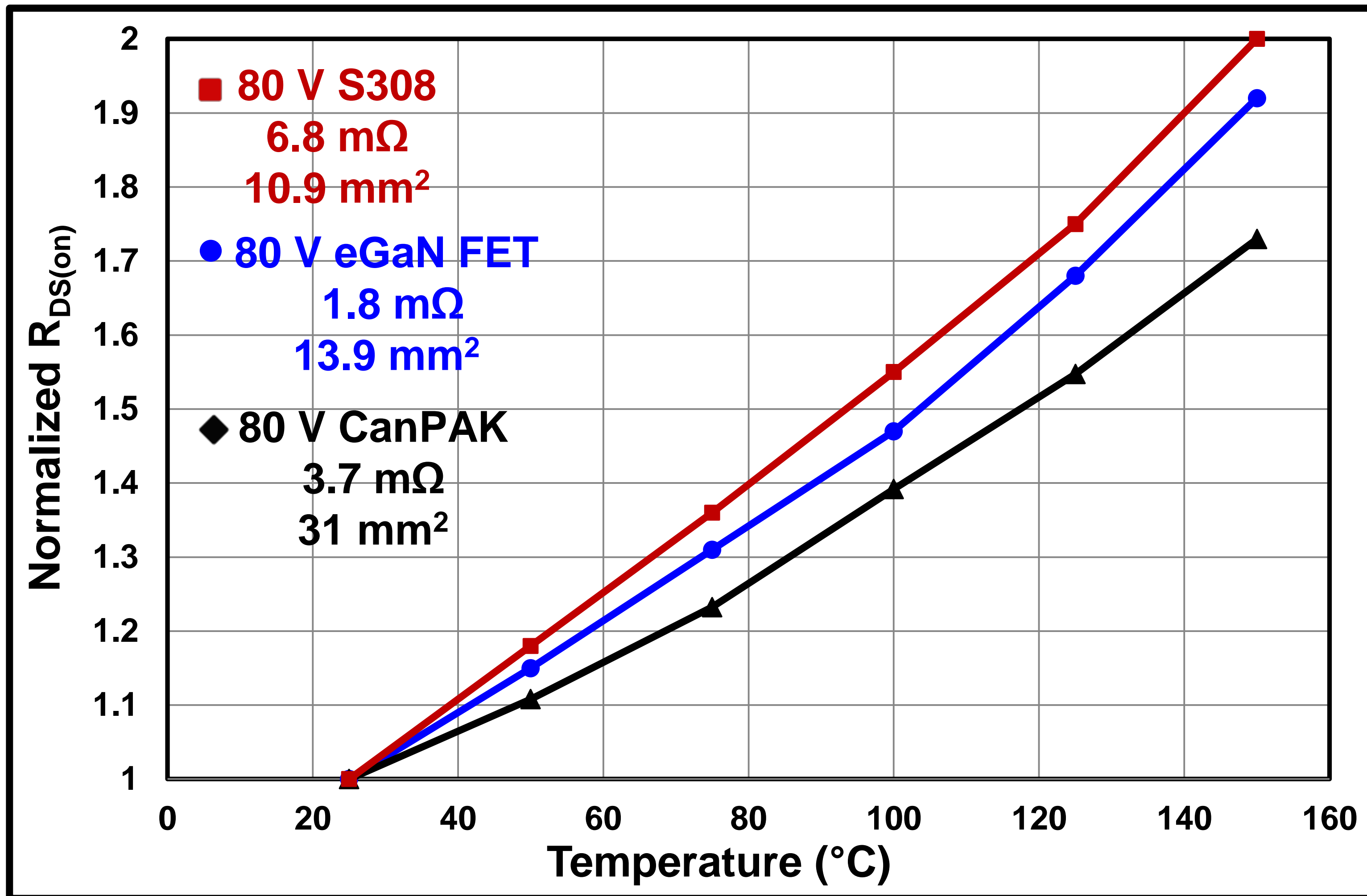
Can PAK MOSFET

100°C

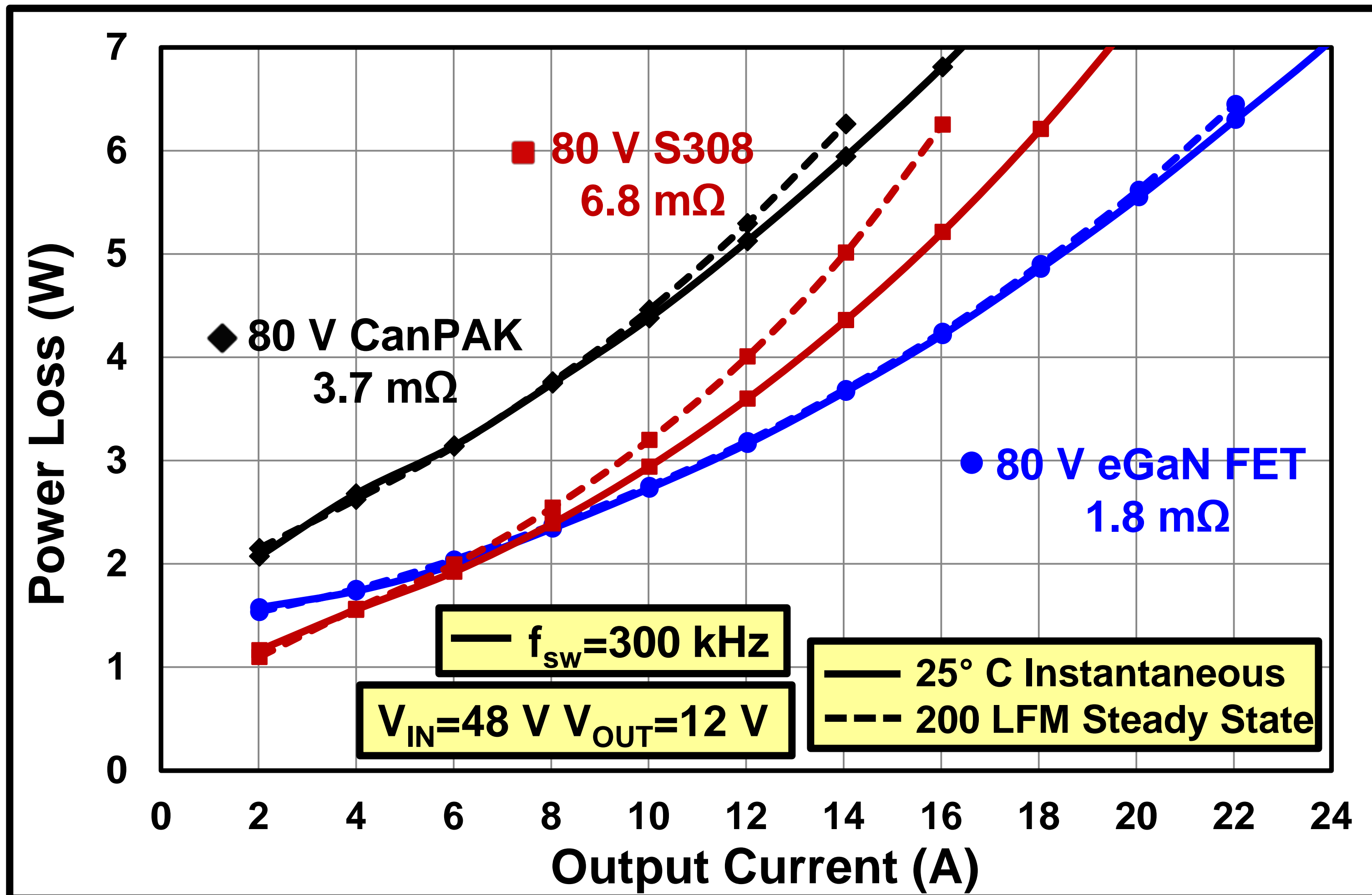
25°C

Fan Speed=200 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

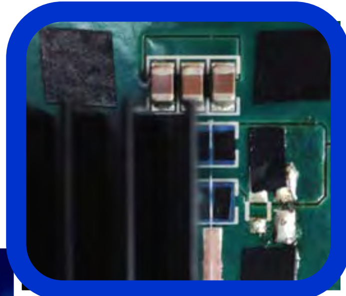
Thermal Impact on Electrical Performance



Thermal Impact on Electrical Performance

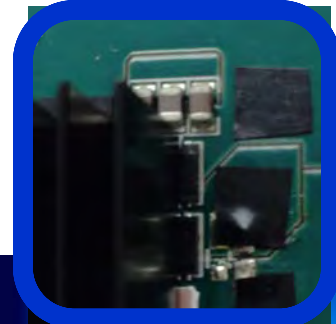


eGaN FET and S308 MOSFET



Q1 ≈ 65°C

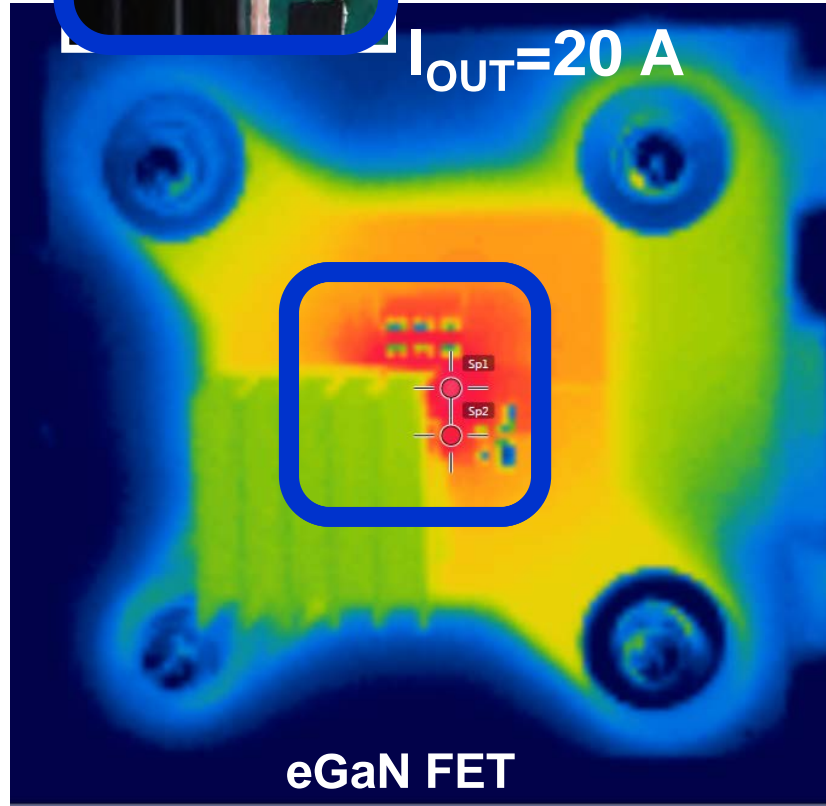
Q2 ≈ 54°C

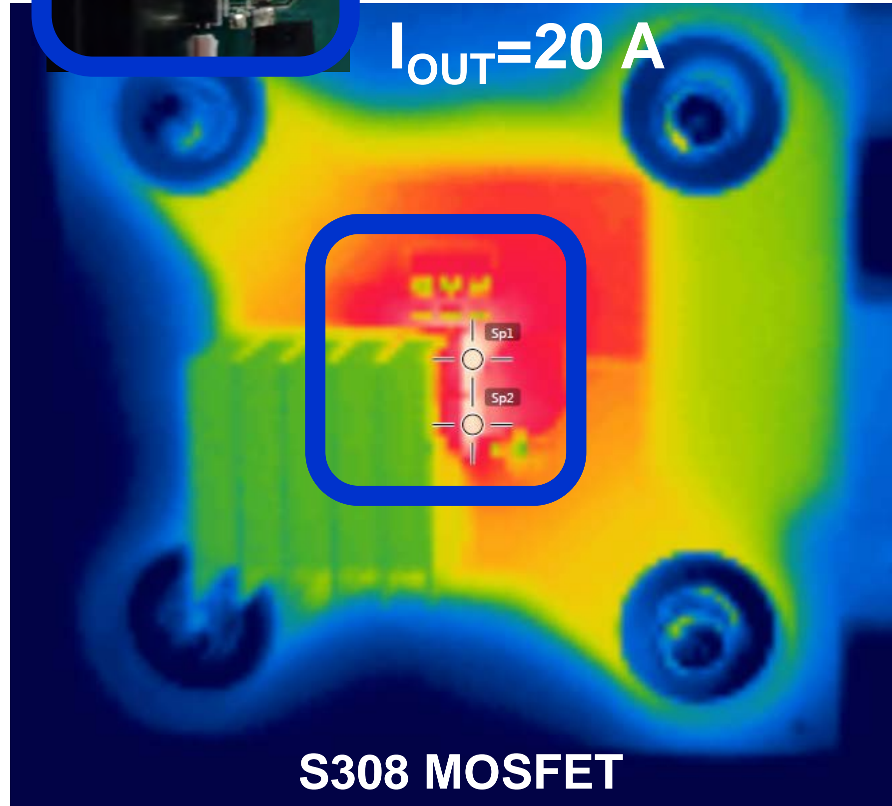


Q1 ≈ 102°C

Q2 ≈ 100°C

100°C

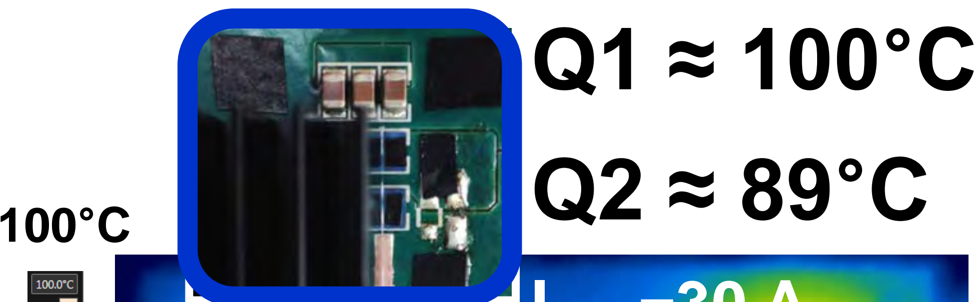


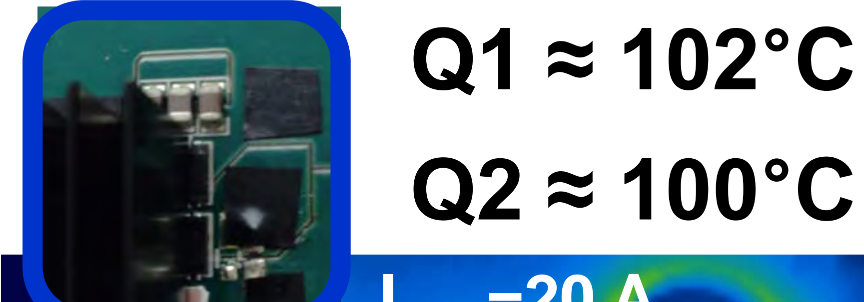


25°C

Fan Speed=400 LFM I_{OUT}=20 A V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

eGaN FET and S308 MOSFET





Q1 ≈ 100°C

Q2 ≈ 89°C

Q1 ≈ 102°C

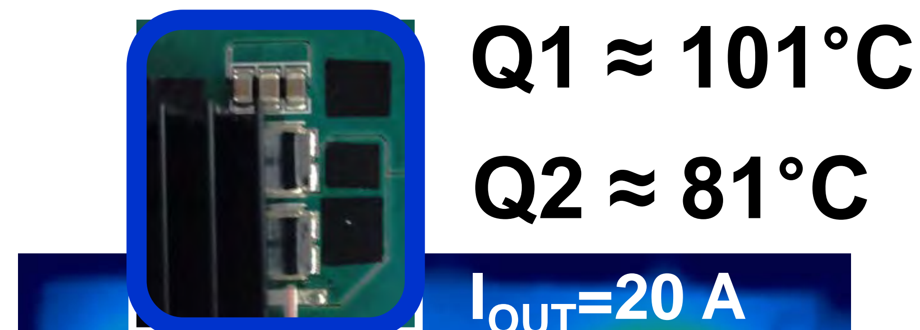
Q2 ≈ 100°C

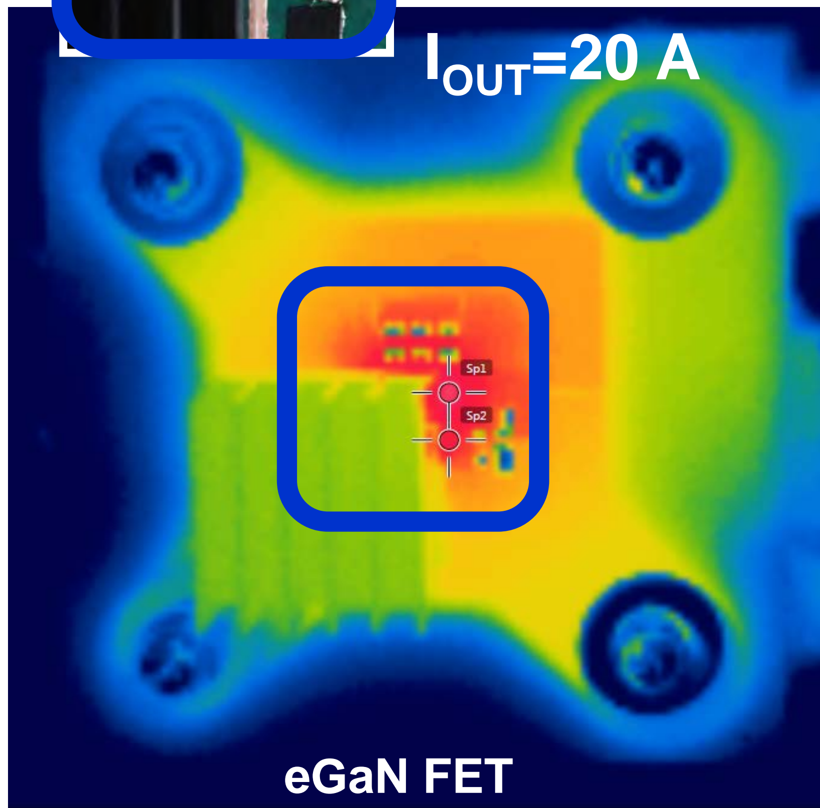
100°C

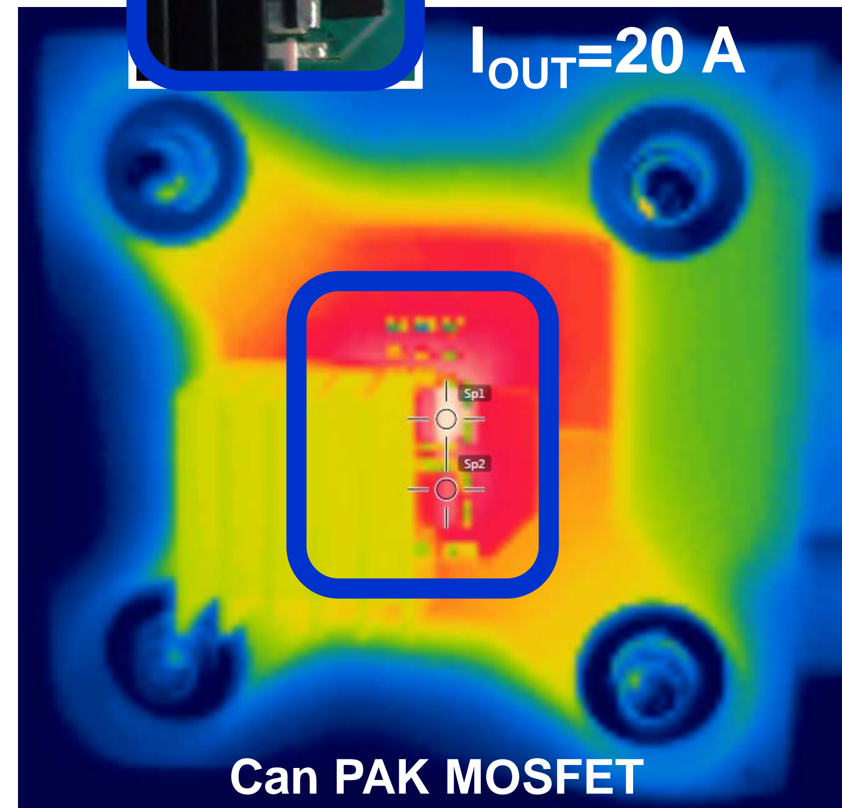
25°C

Fan Speed=400 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 µH

eGaN FET and CanPAK MOSFET

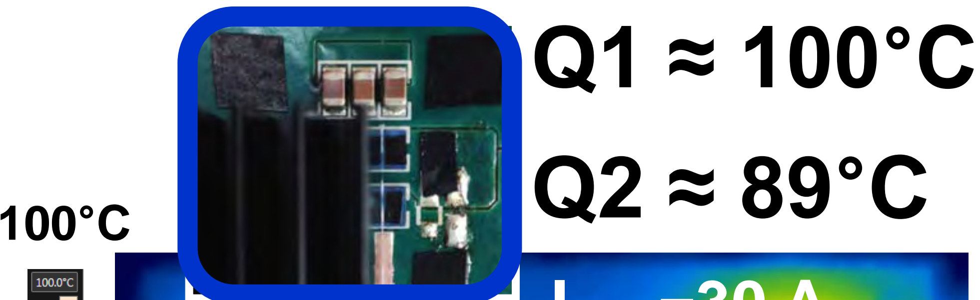






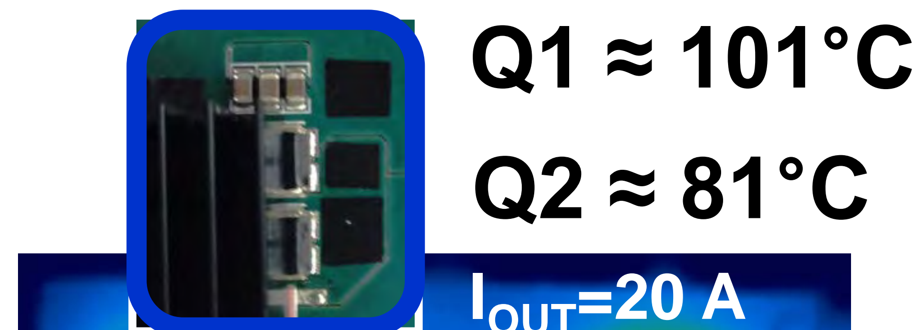
Fan Speed=400 LFM I_{OUT}=20 A V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

eGaN FET and CanPAK MOSFET



Q1 ≈ 100°C

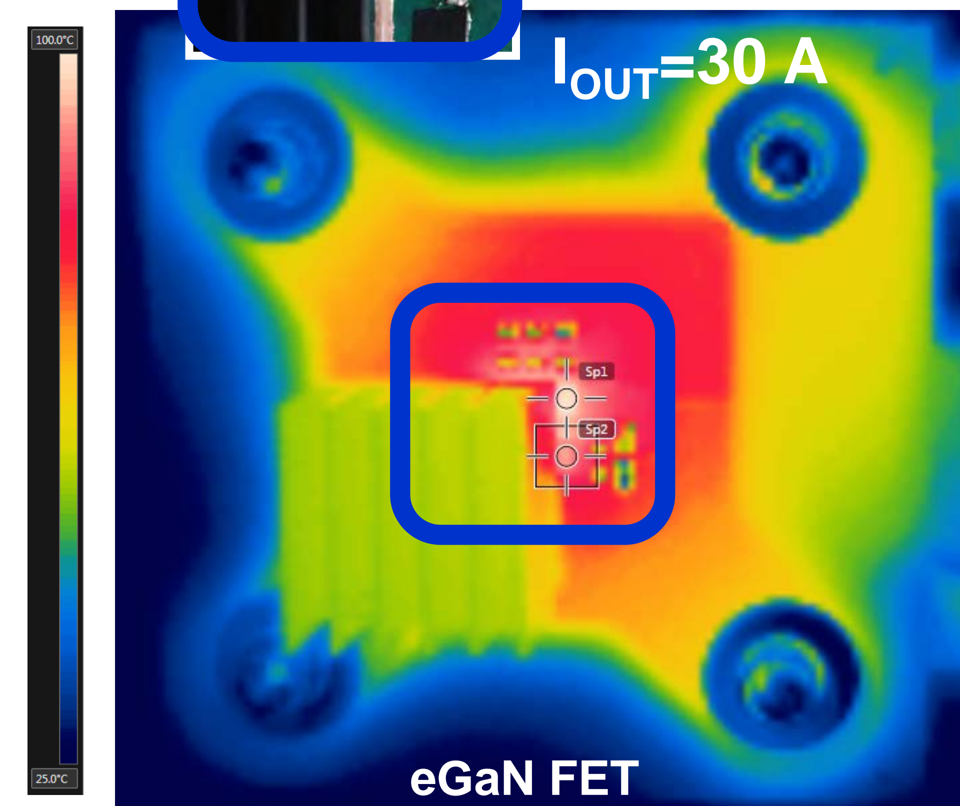
Q2 ≈ 89°C

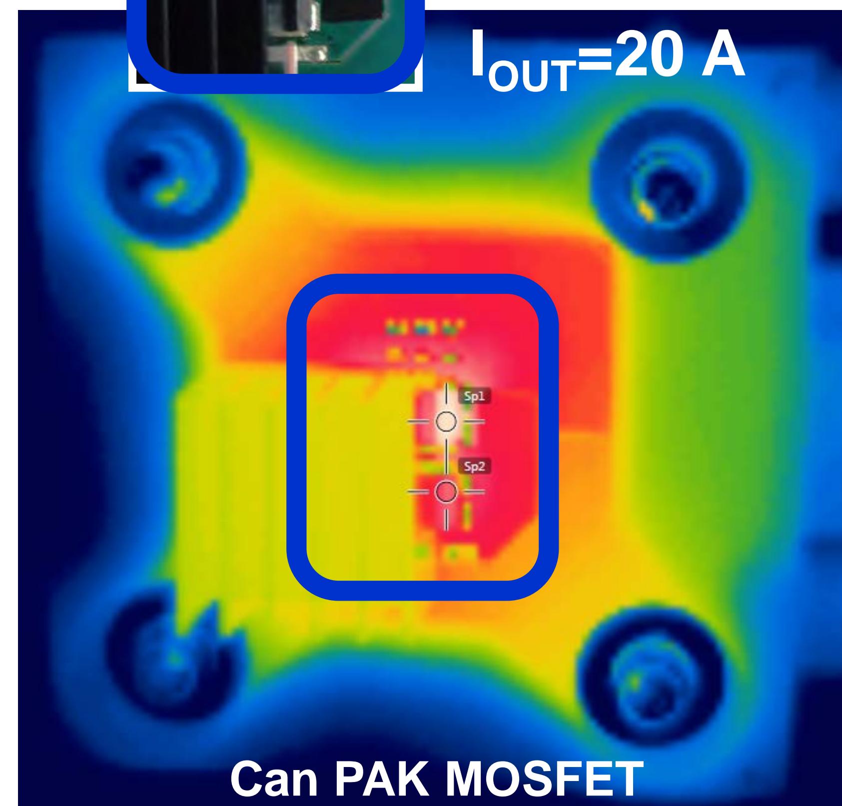


Q1 ≈ 101°C

Q2 ≈ 81°C

100°C

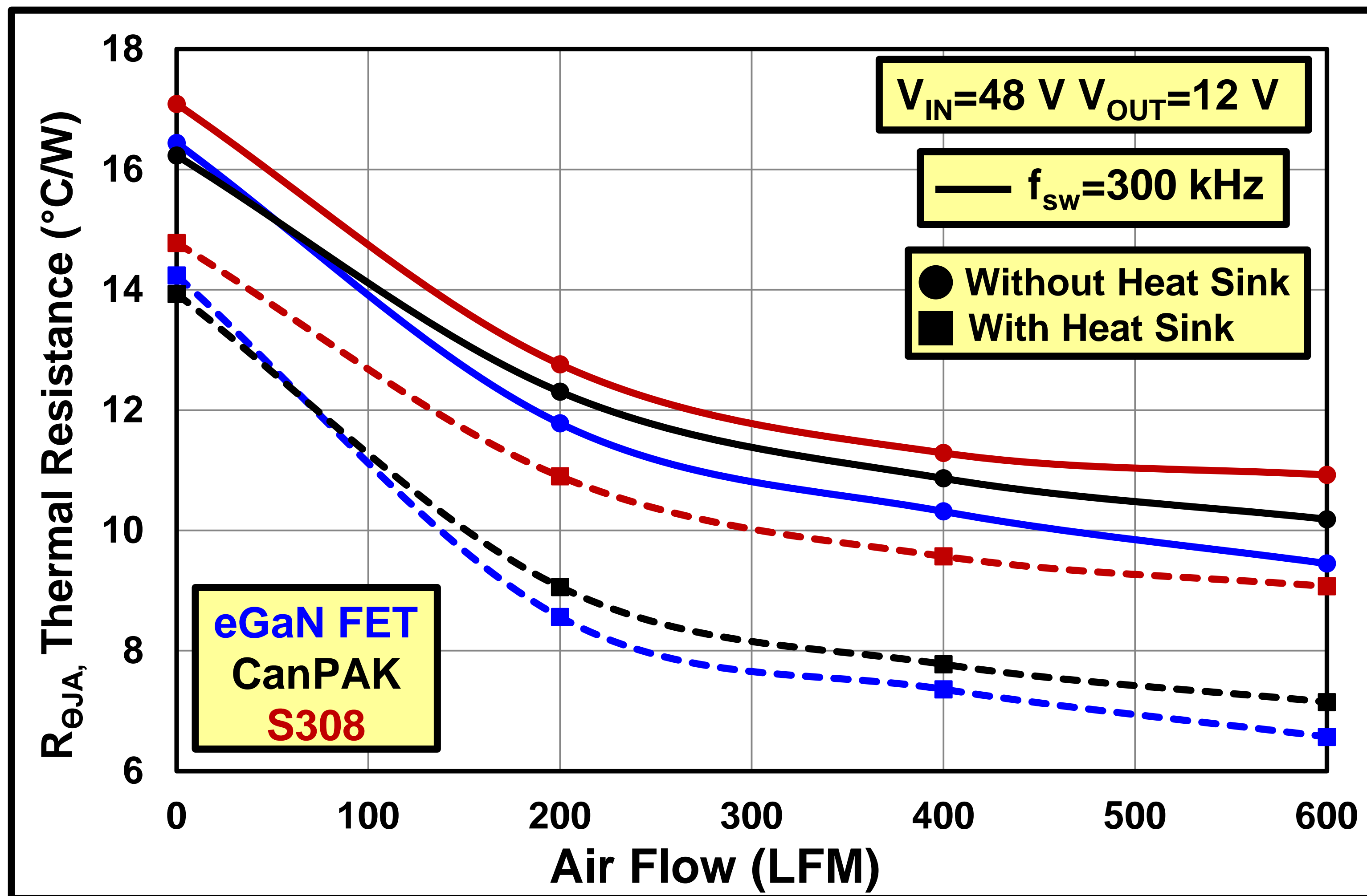




25°C

Fan Speed=400 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 μH

Impact of Heat Sink



Design Examples
48 V_{IN} to Load Voltage

Power Architecture Requirements

- Power density
- Efficiency
- Availability
- Cost
- Ease of design
- Safety

Intermediate Bus Architecture (IBA)

DC Bus Architecture

48 V Isolated Hard-switched Regulated 1/8th Brick Converter

APEC

Some typical high-power *regulated* eighth-bricks

EPC EFFICIENT POWER CONVERSION

V_{in}	**38-55**
V_{out}	9.6
I_{out}	31
P_{out}	**300**
η_{max}	96.1%

V_{in}	**42-60**
V_{out}	12
I_{out}	25
P_{out}	**300**
η_{max}	96%

V_{in}	**40-60**
V_{out}	12
I_{out}	25
P_{out}	**300**
η_{max}	95.5

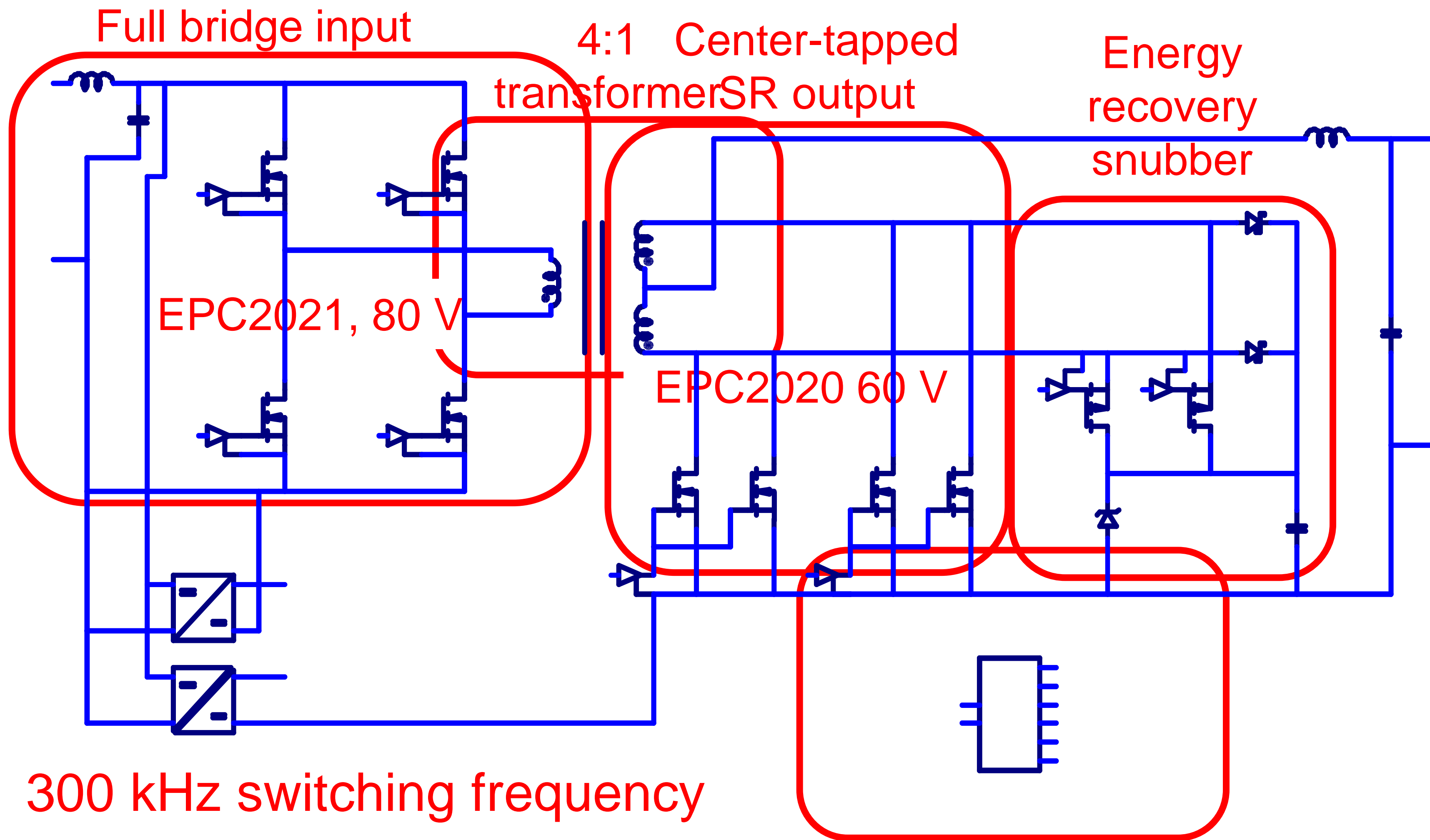
V_{in}	**45-55**
V_{out}	9.6
I_{out}	33
P_{out}	**320**
η_{max}	95.5%

eGaN FETs can boost power up to 500W and beyond!

500 W Eighth-brick Specifications

- 500 W at 12 V out
- 48 V to 60 V in
- Fully regulated
- Isolated
- > 96% full load efficiency
- DOSA-compliant footprint

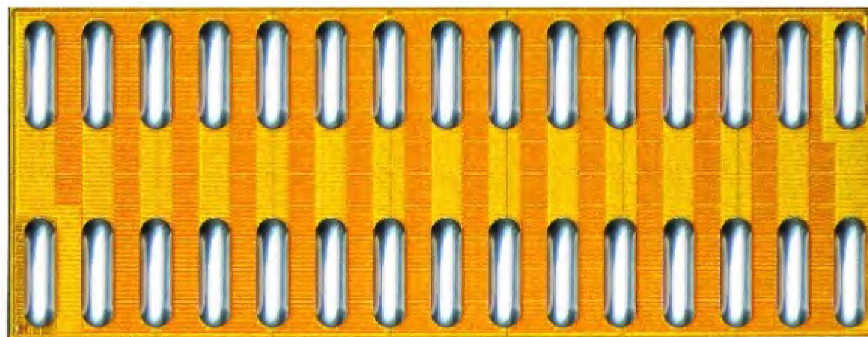
Design Approach



300 kHz switching frequency

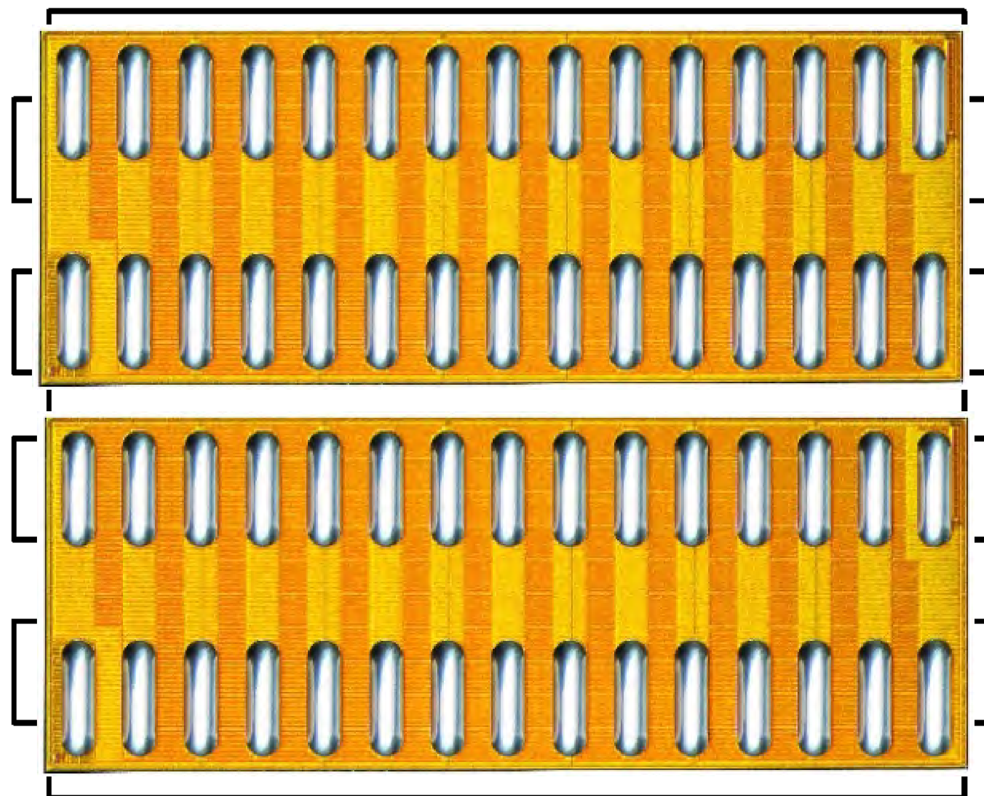
Conventional hard-switched PWM

Large area eGaN FETs



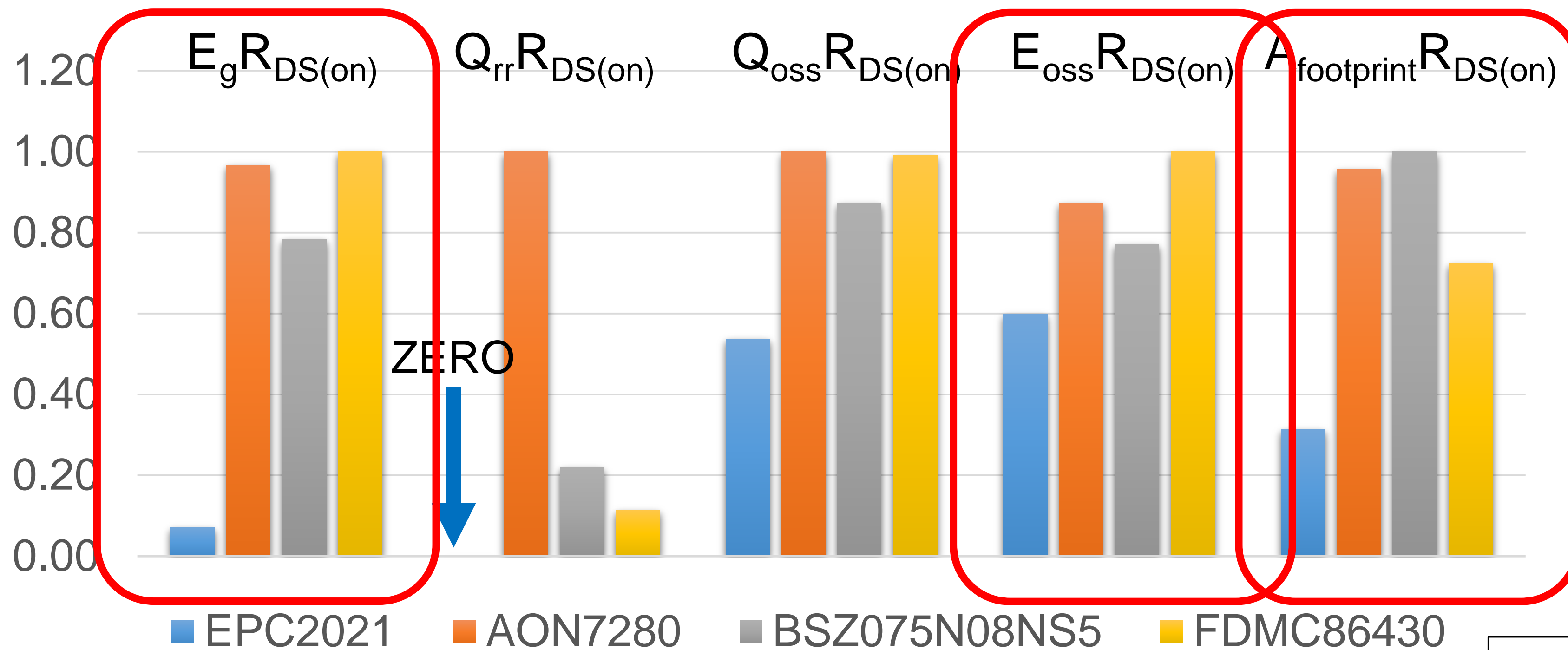
Part	Max V_{DS} [V]	I_D [A]	Max $R_{DS(on)}$ [mΩ]
EPC2020	60 V	60 A	2.0
EPC2021	80 V	60 A	2.5
EPC2022	100 V	60 A	3.2
EPC2023	30 V	60 A	1.3
EPC2024	40 V	60 A	1.5

Don’t forget about size!



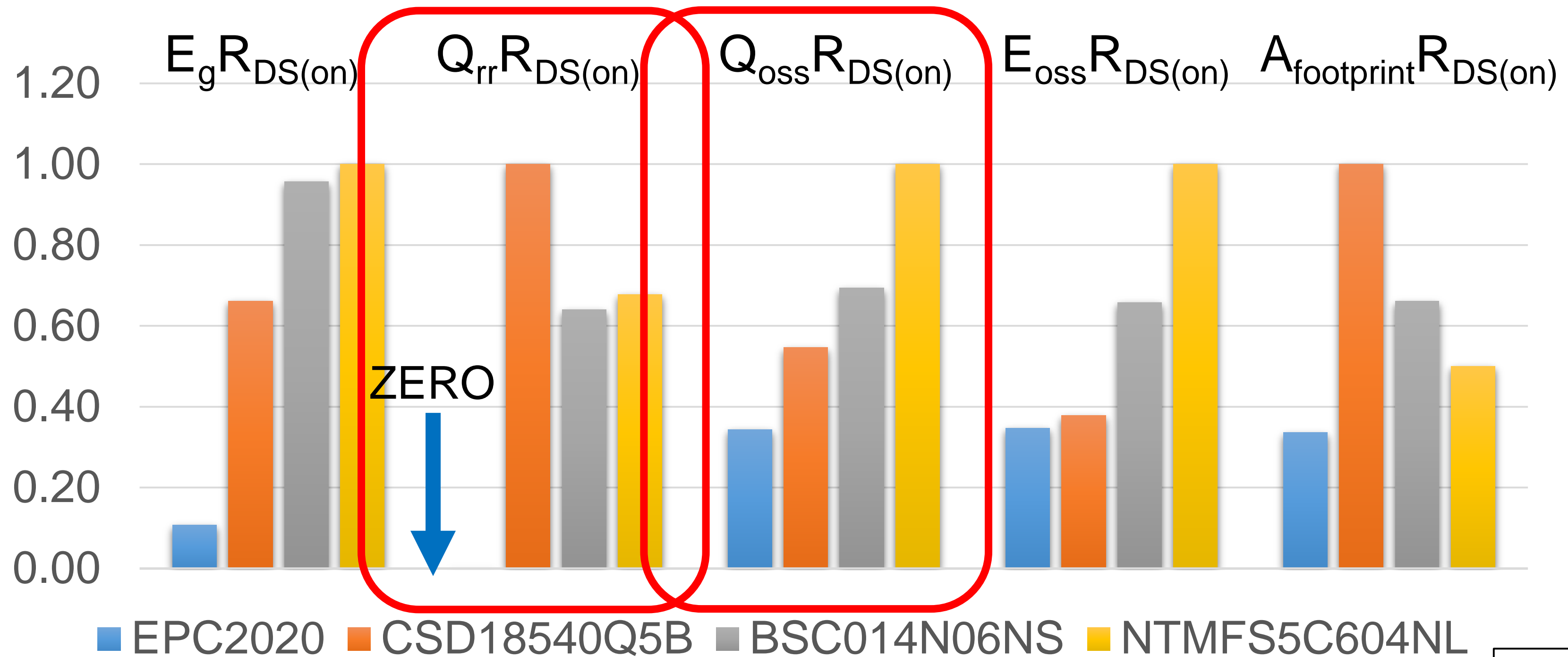
5X6 PQFN

80 V FOM Comparison



V_{DS} = 52 V

60 V FOM Comparison



V_{DS} = 26 V

APEC

Layout Considerations

EPC EFFICIENT POWER CONVERSION

- Minimize loop inductance
- Symmetry for V-s balance
- Copper for thermals
- Guide power currents away from signal ground
- Takes diligence, but doable – the effort pays off!

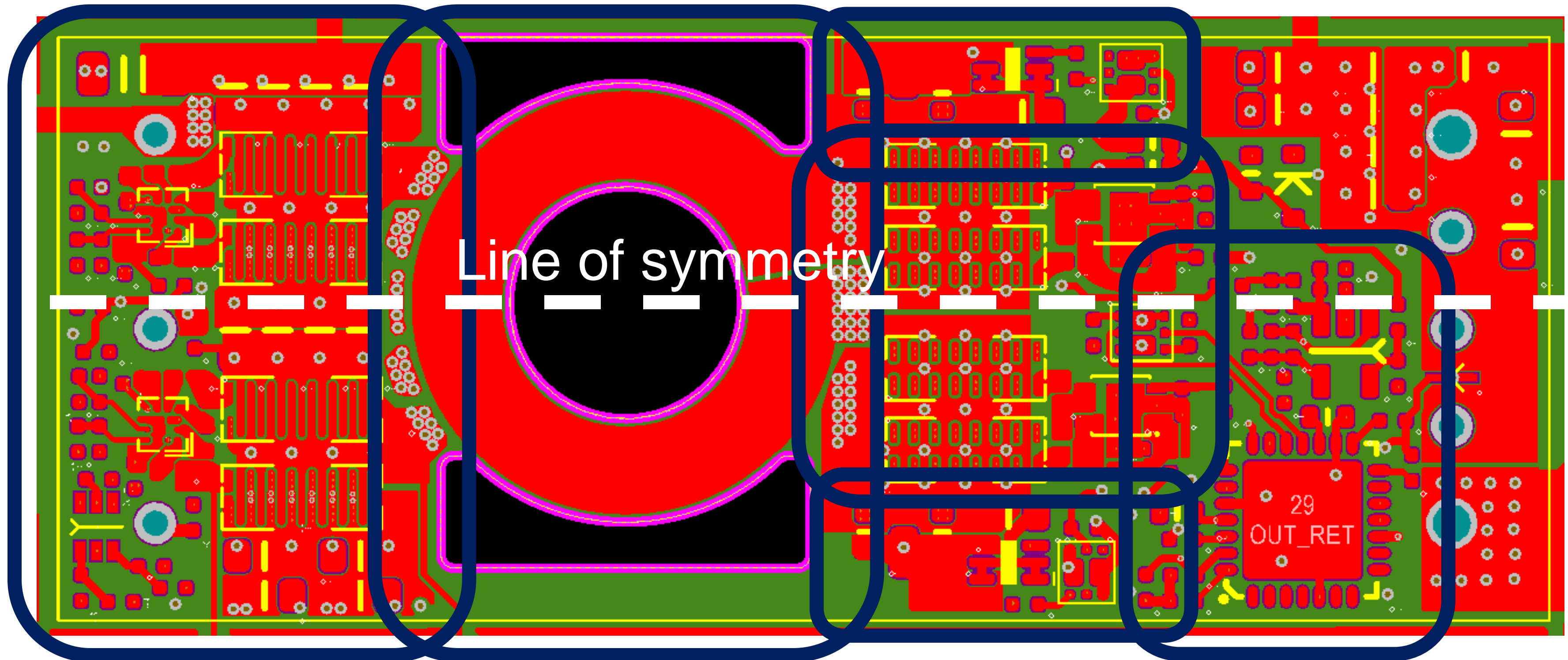
Overall layout

Full bridge input

4:1 transformer

Center-tapped SR

Energy recovery snubber



Digital control

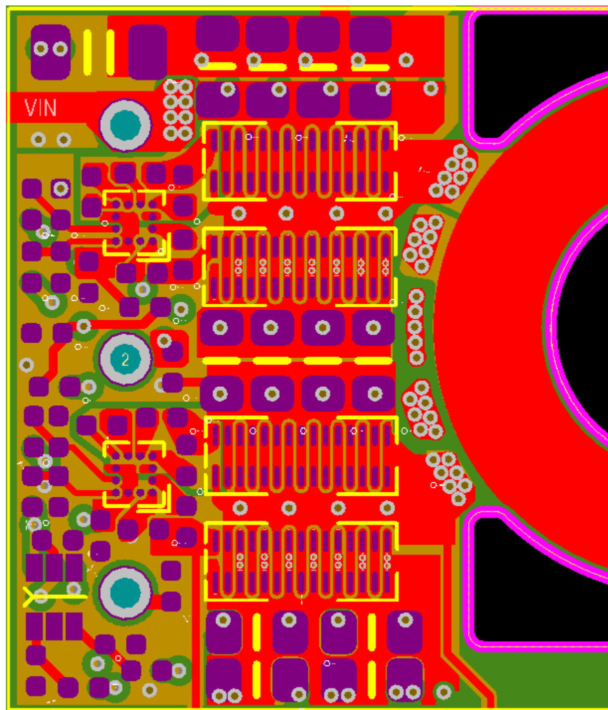
Bottom side: input and output filter inductors, bias supply

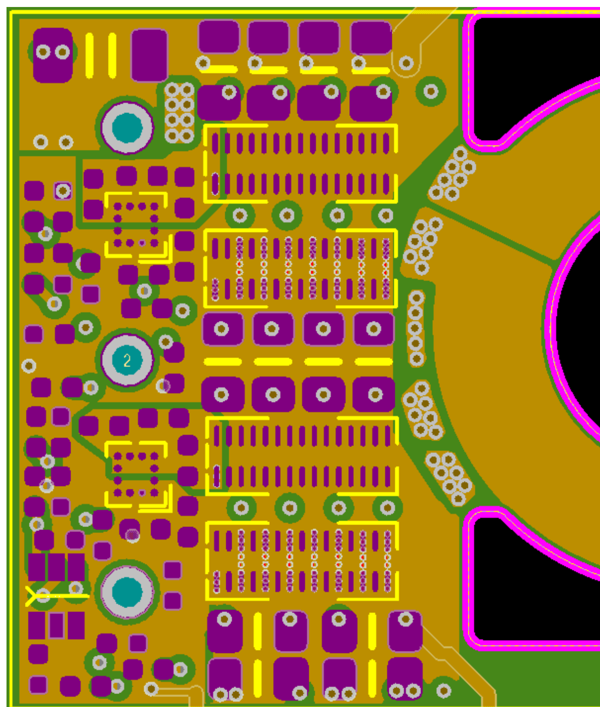
Primary side optimal layout

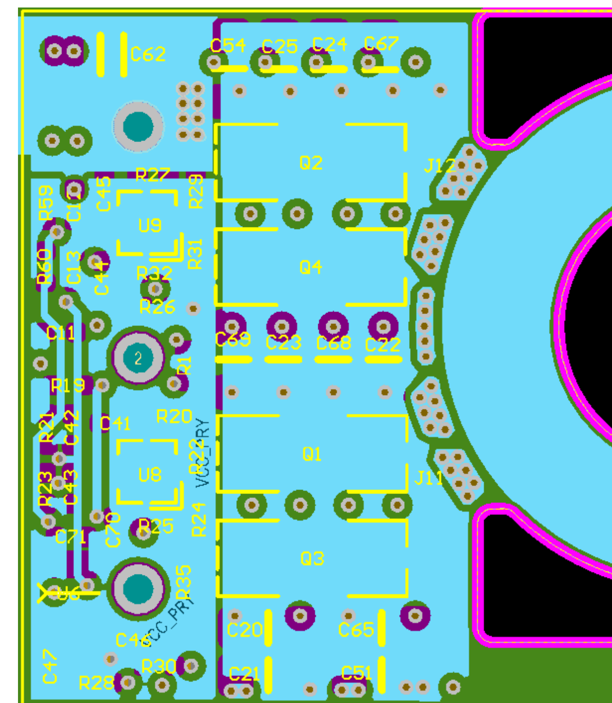
Top layer:
V_{IN}, GND, Primary

Layer 2:
GND

Layer 3:
V_{IN}





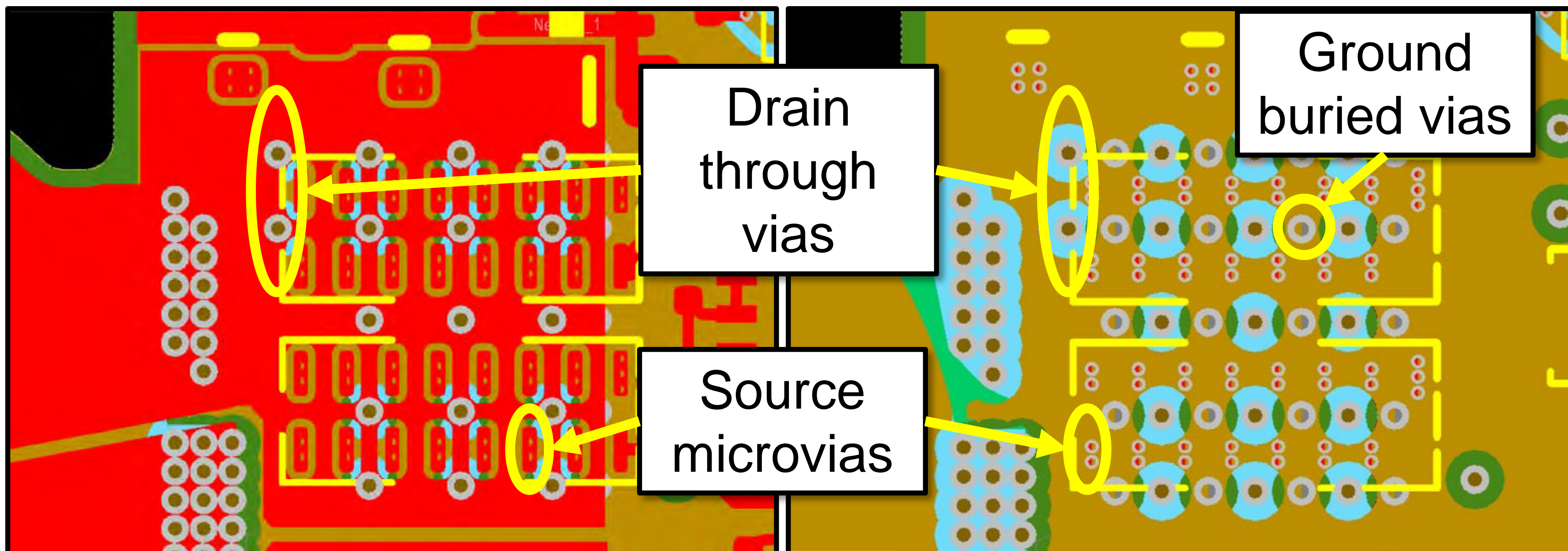


Repeat 4X

SR layout – two FETs in parallel

Top layer: Drain

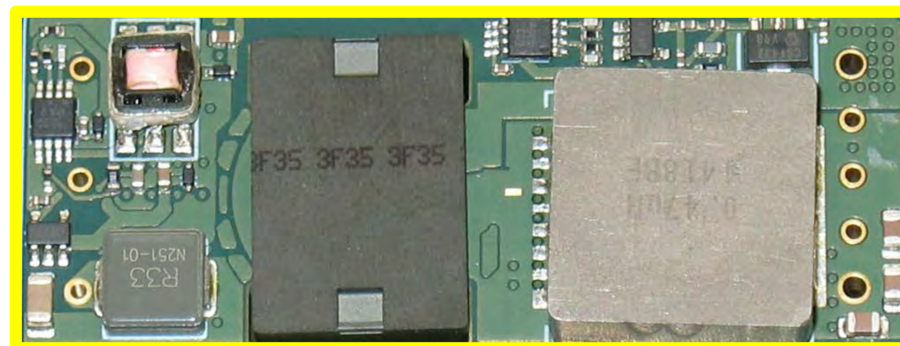
Layer 2: Ground



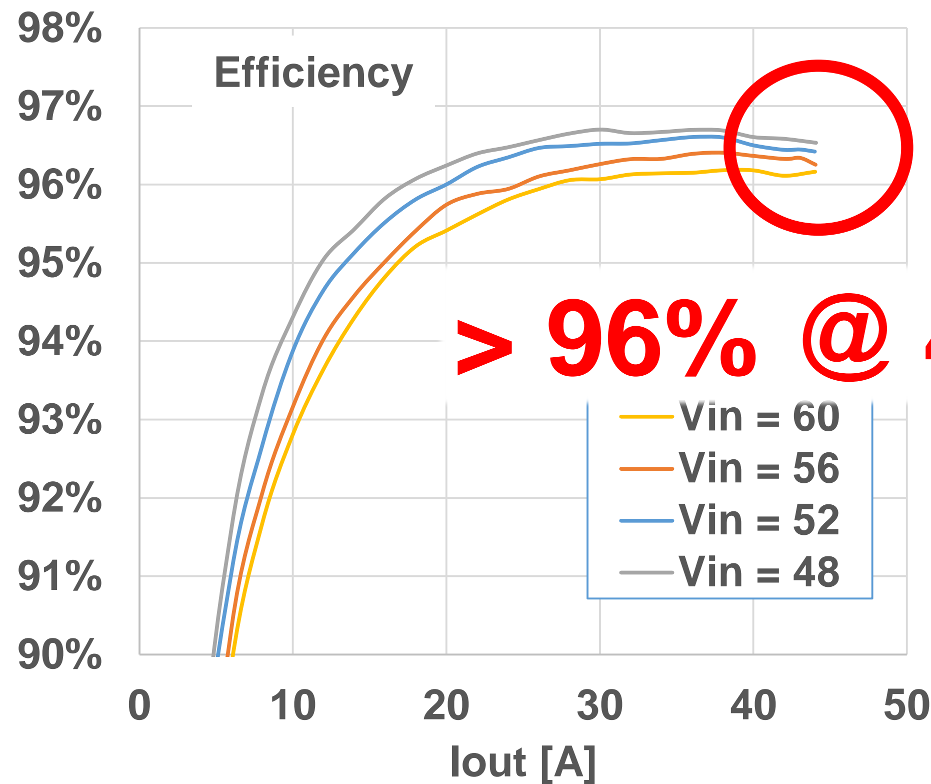
Repeat 4X

EPC9115 Demo Board Layout

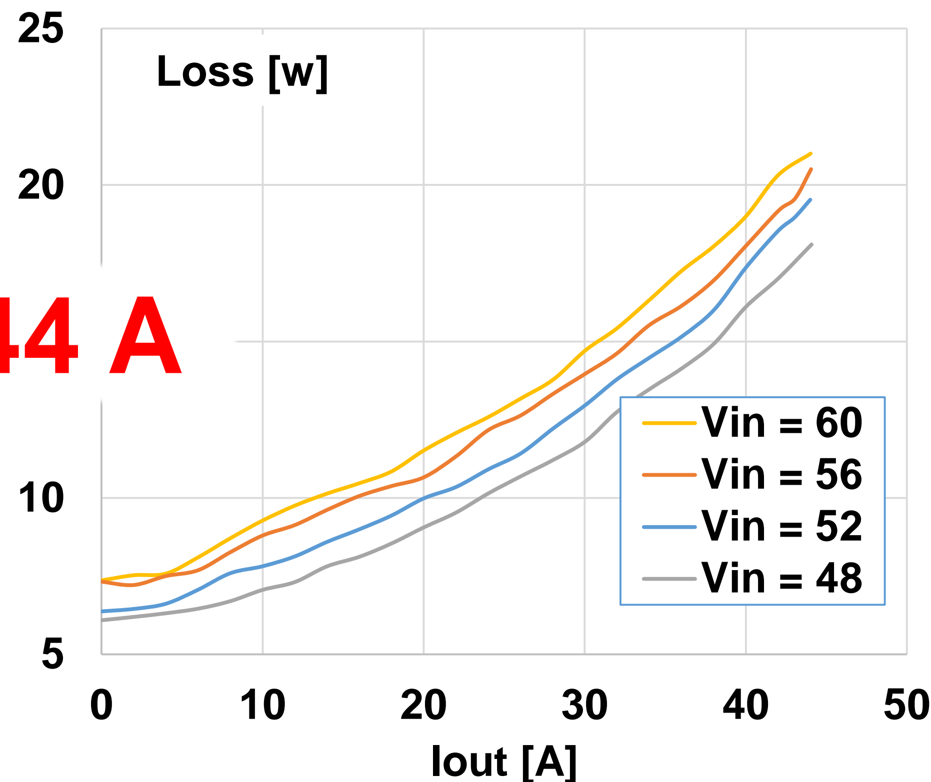
TOP and Bottom views



Typical Performance Curves



> 96% @ 44 A

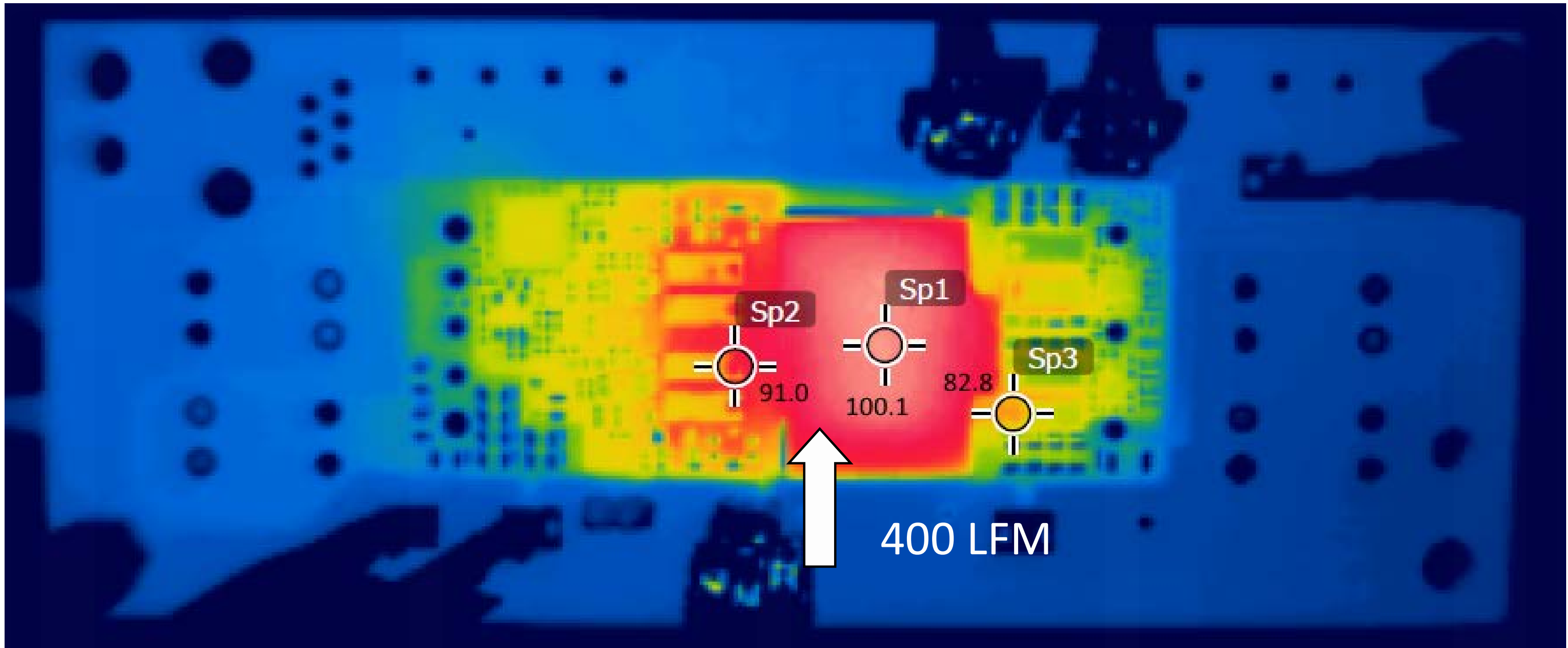


Thermal steady state:

400 LFM (2 m/s) forced convection

ambient temperature 27° C

Nominal Thermal Image

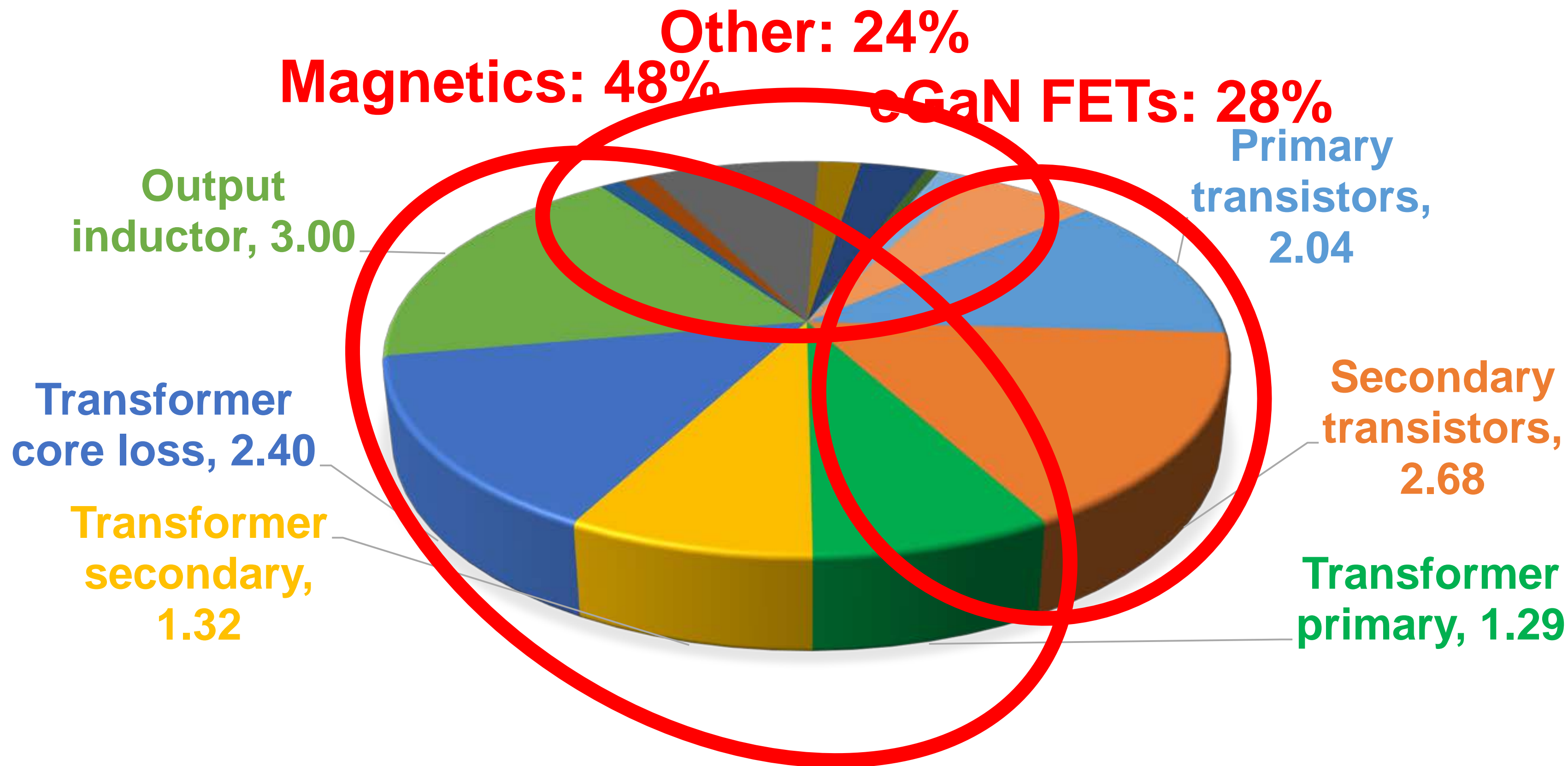


Thermal steady state:

400 LFM (2 m/s) forced convection

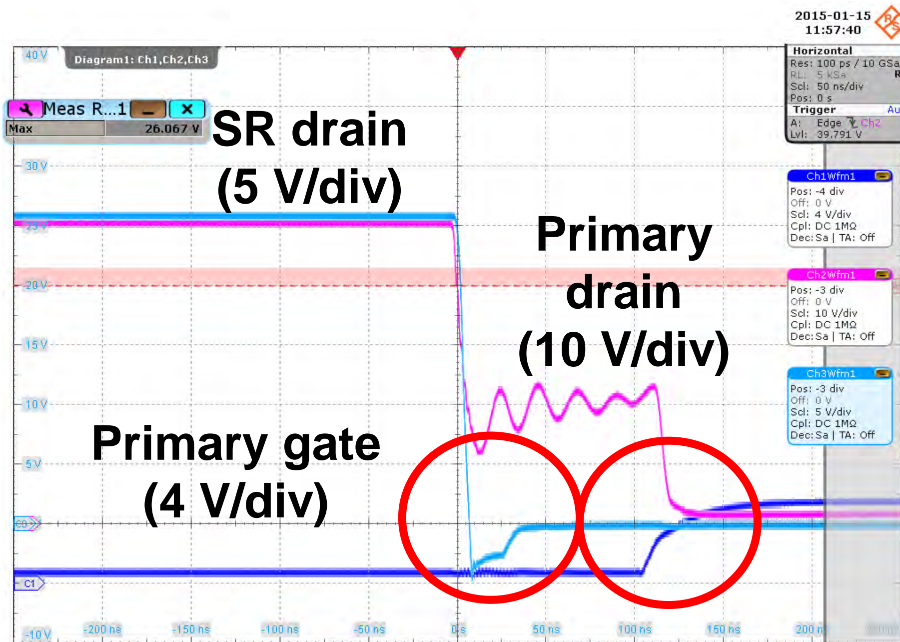
ambient temperature 27° C

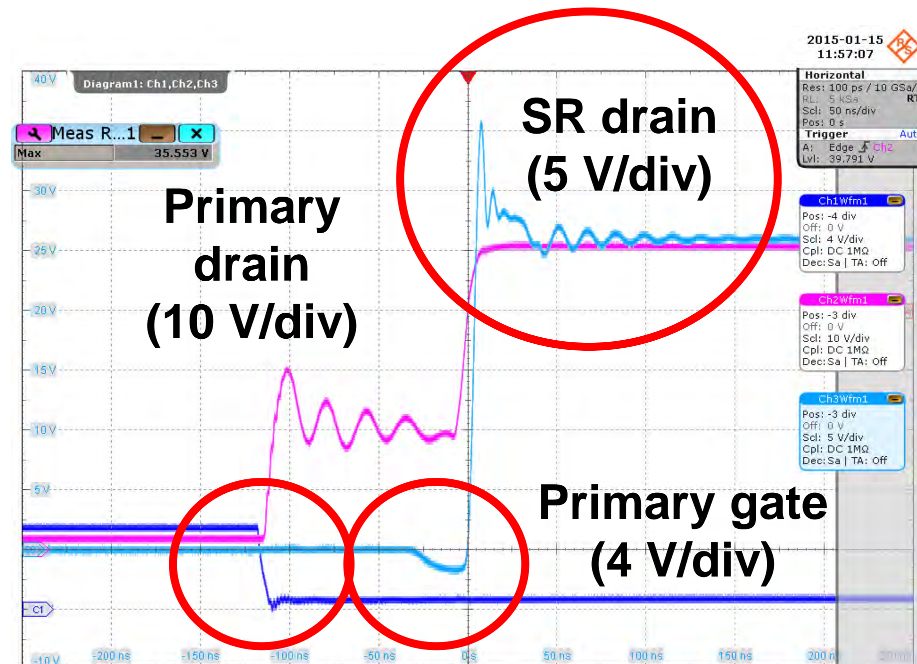
Power loss breakdown (estimate)



Total: 16.6 W @ 100°C
Excludes: Vias, solder joints, traces

Switching transition waveforms





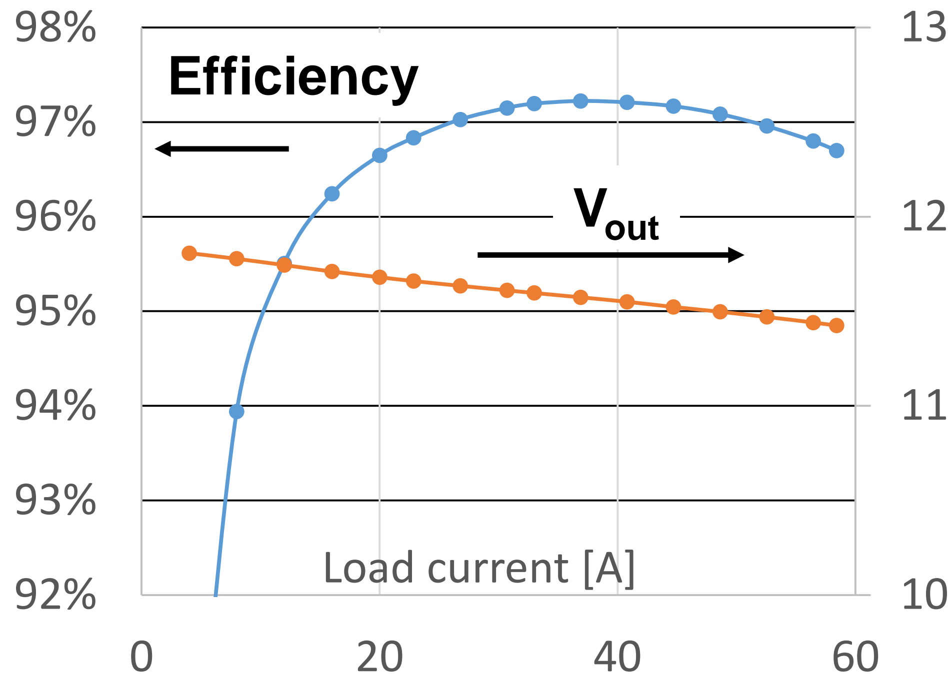
50 ns/div

V_{in} = 52 V, V_{out} = 12 V, I_{out} = 42 A

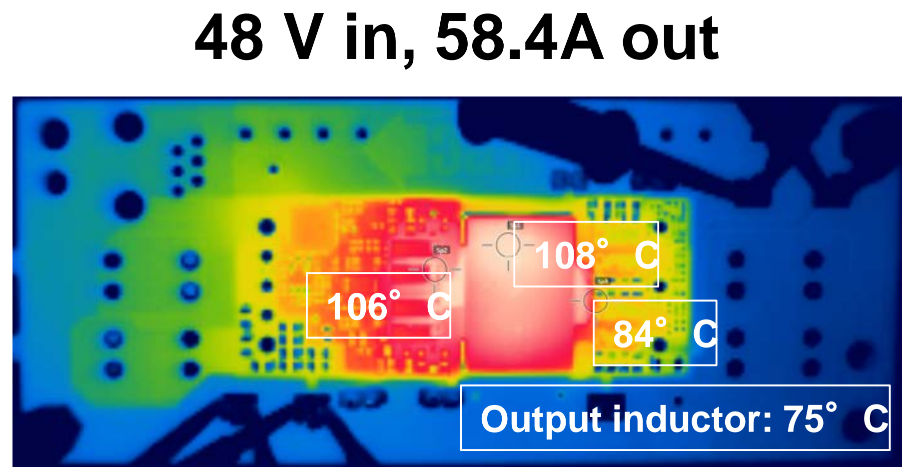
Ways to improve E-brick efficiency

- Improve bias supply (draws 1.3W, but bias load 0.6W)
- Add heat sink
- Optimize gate resistors
- Optimize dead time
- Use custom magnetics
- Optimize switching frequency

DCX performance with smaller inductor



48 V in, 58.4A out



667 W Output

Operating conditions:

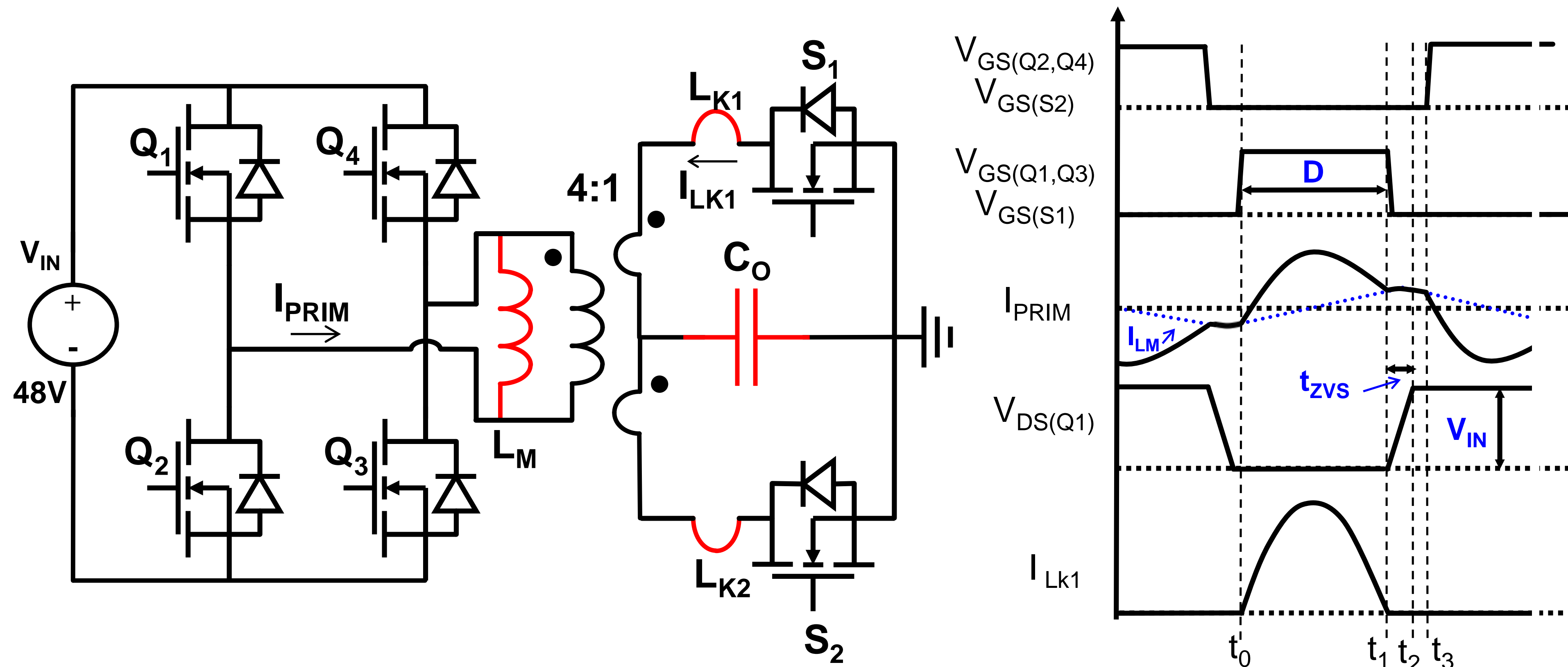
400 LFM (2 m/s) forced convection

ambient temperature 24°C

thermal steady state.

Resonant Bus Converter

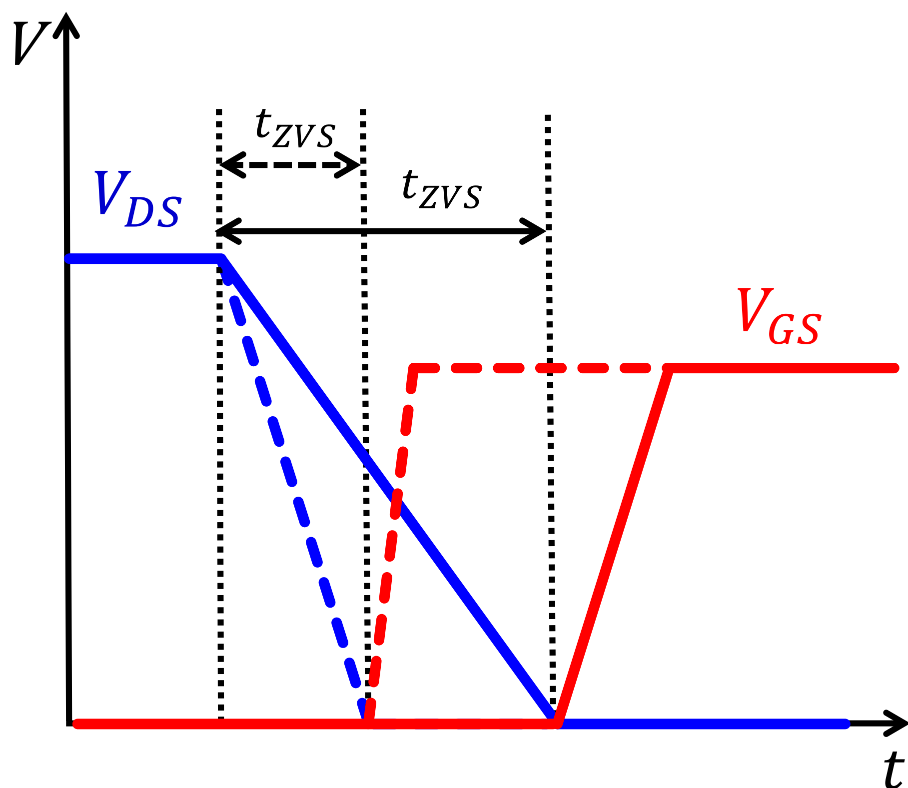
High Frequency DC/DC Transformer

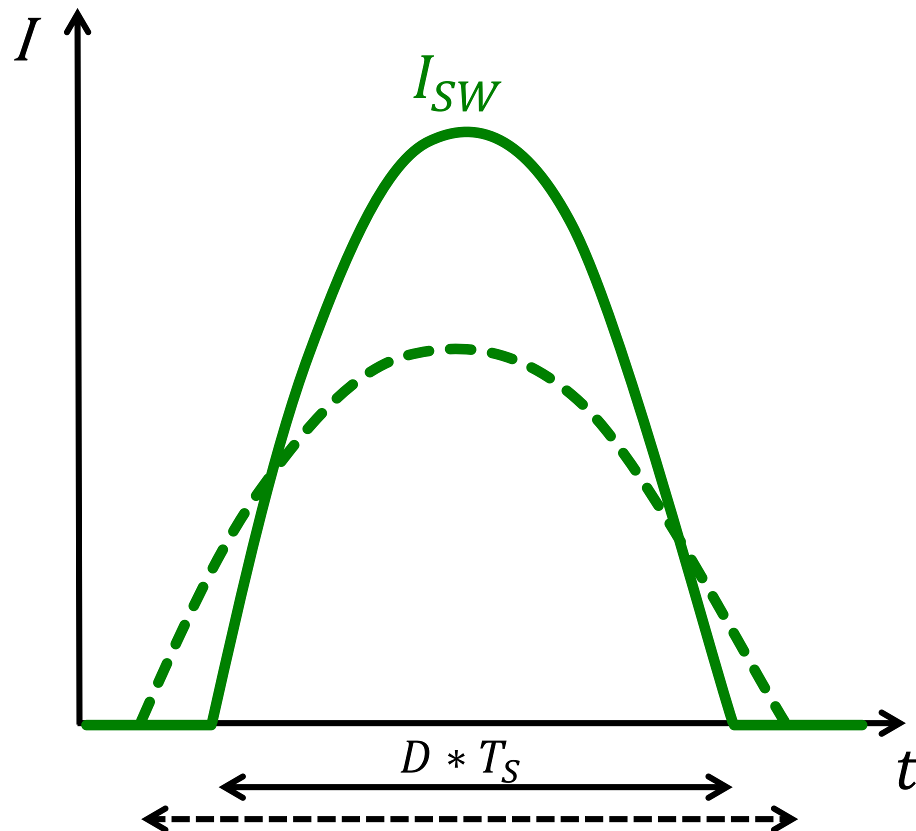


Ref: Y. Ren, M. Xu, J. Sun, and F. C. Lee, “A family of high power density unregulated bus converters,” IEEE Trans. Power Electron., vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

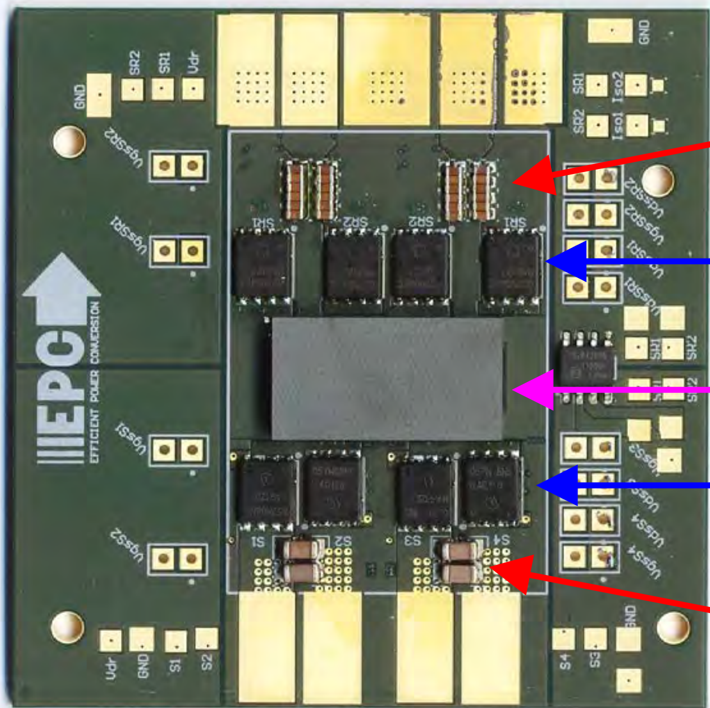
Output Charge

Q_{OSS} ↓ t_{ZVS} ↓ I_{RMS} ↓ P_{CON} ↓





eGaN FET vs. MOSFET



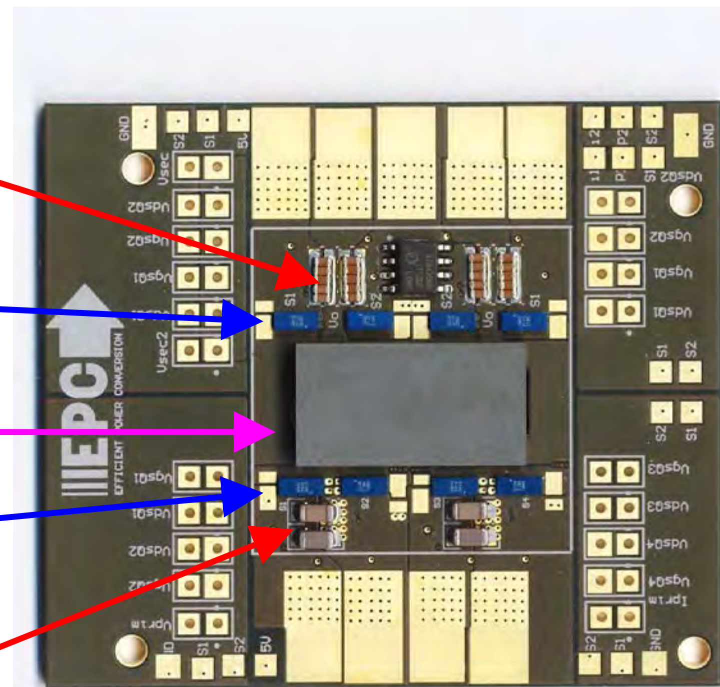
Resonant Capacitors

Secondary Devices

Transformer

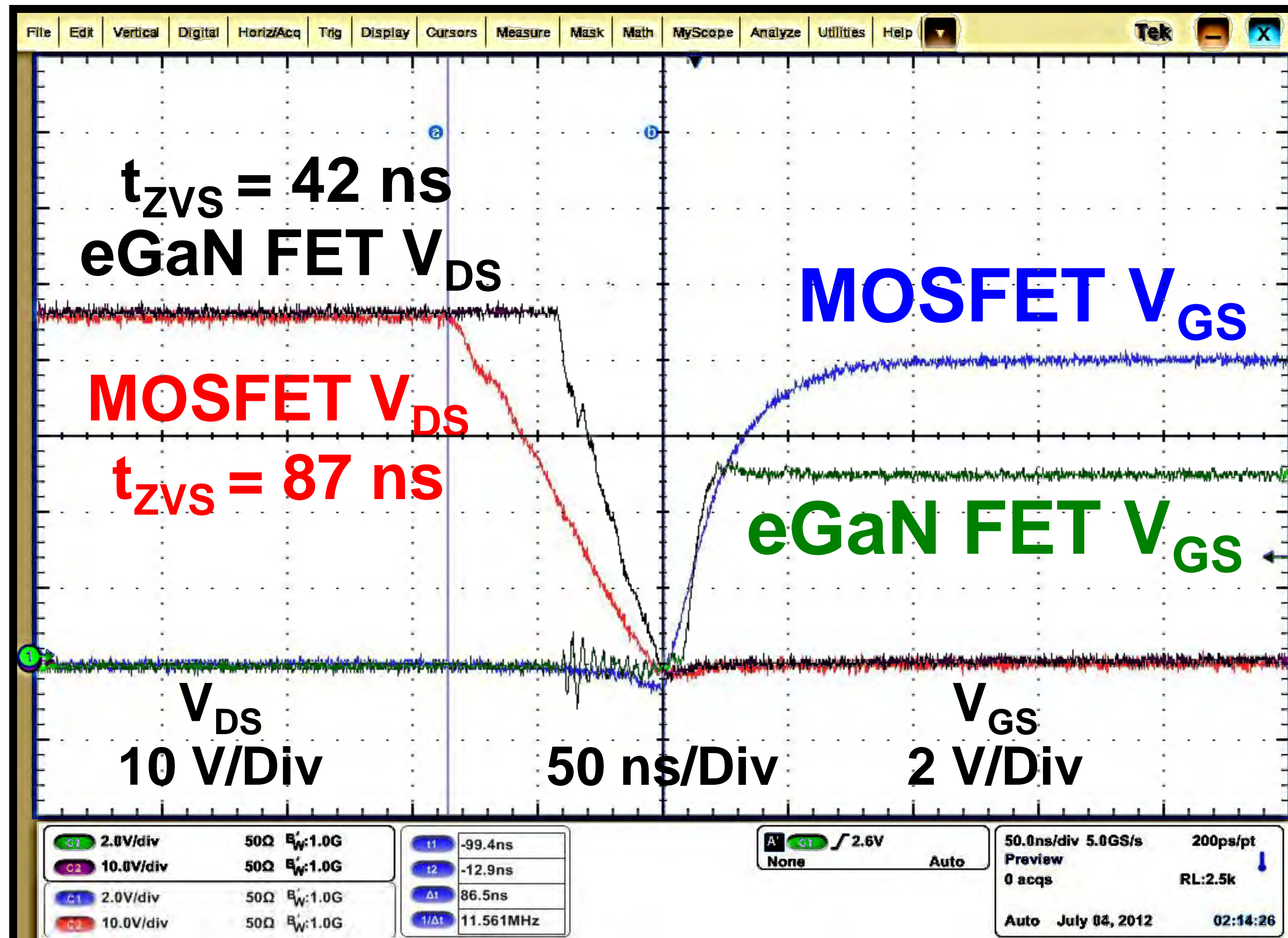
Primary Devices

Input Capacitors



MOSFET **vs.** **eGaN® FET**

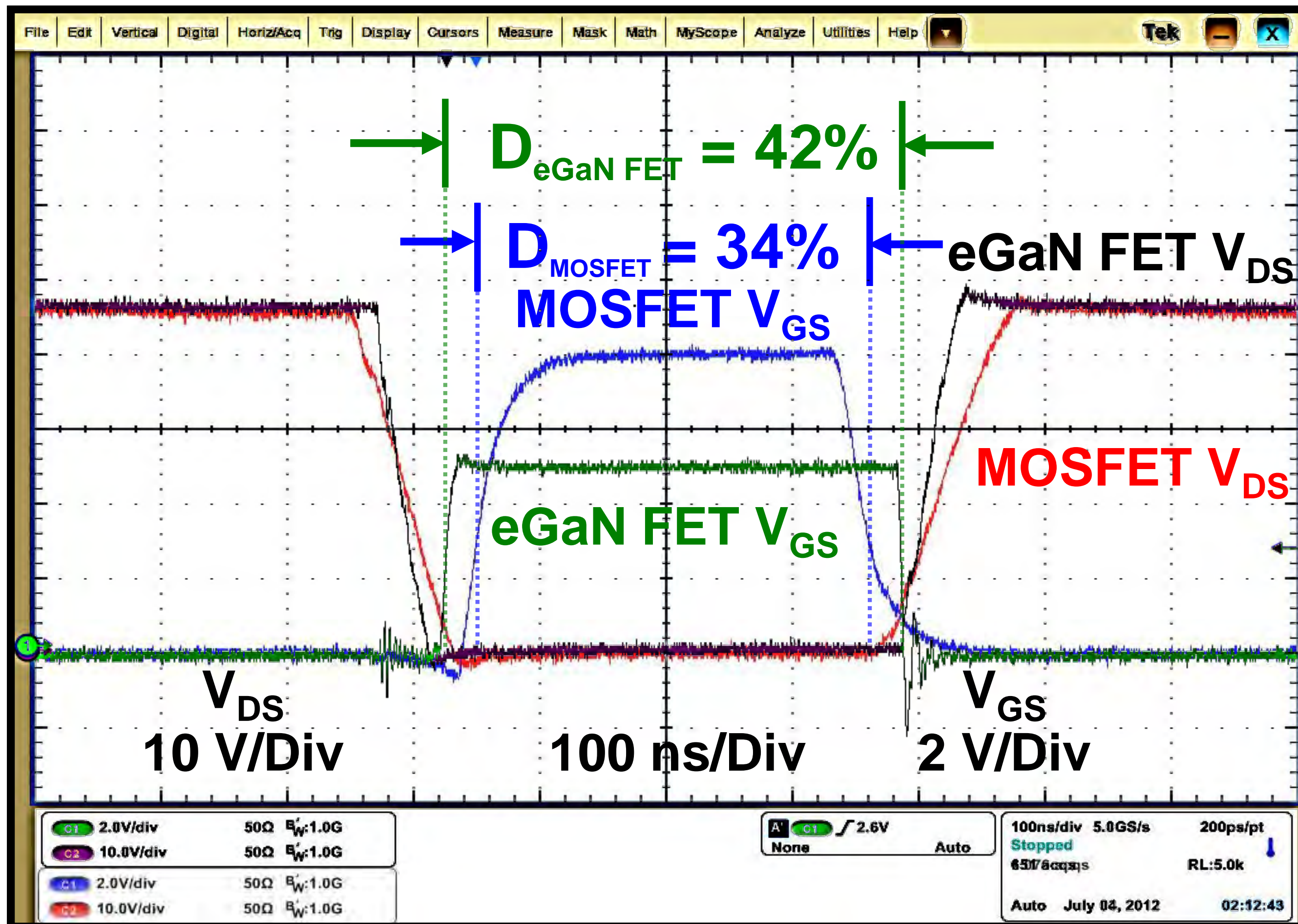
ZVS Switching Comparison



f_{sw} = 1.2 MHz, V_{IN} = 48 V, and $V_{OUT} \approx$ 12 V

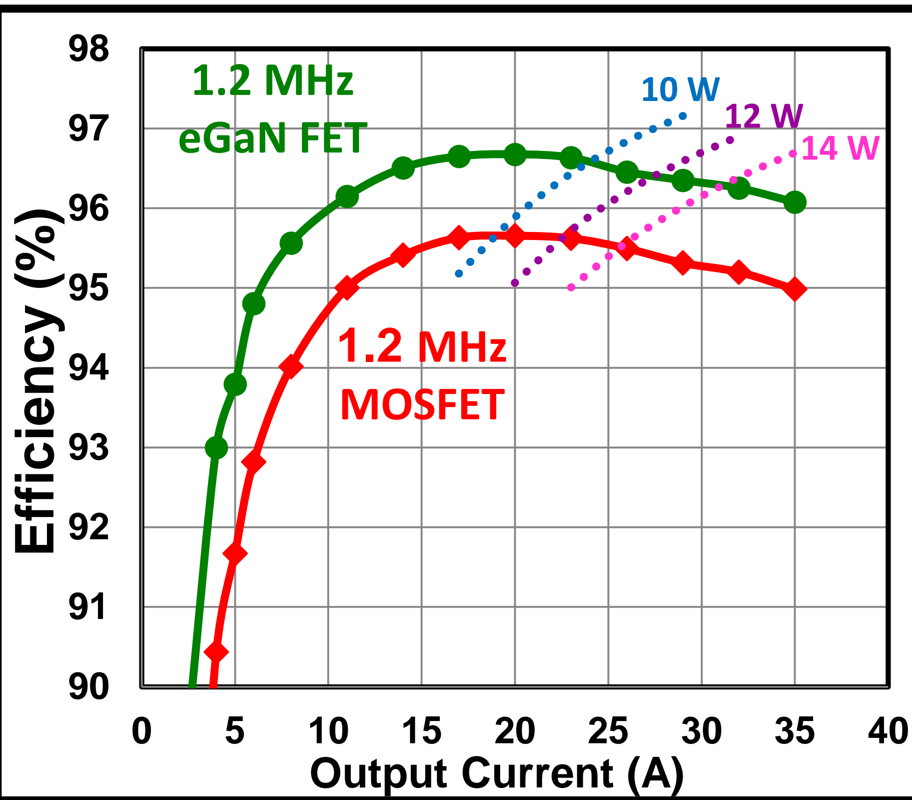
Ref: D. Reusch, J. Strydom, "Evaluation of Gallium Nitride Transistors in High Frequency Resonant and Soft-Switching DC-DC Converters," APEC 2014, IEEE Transactions on Power Electronics 2015

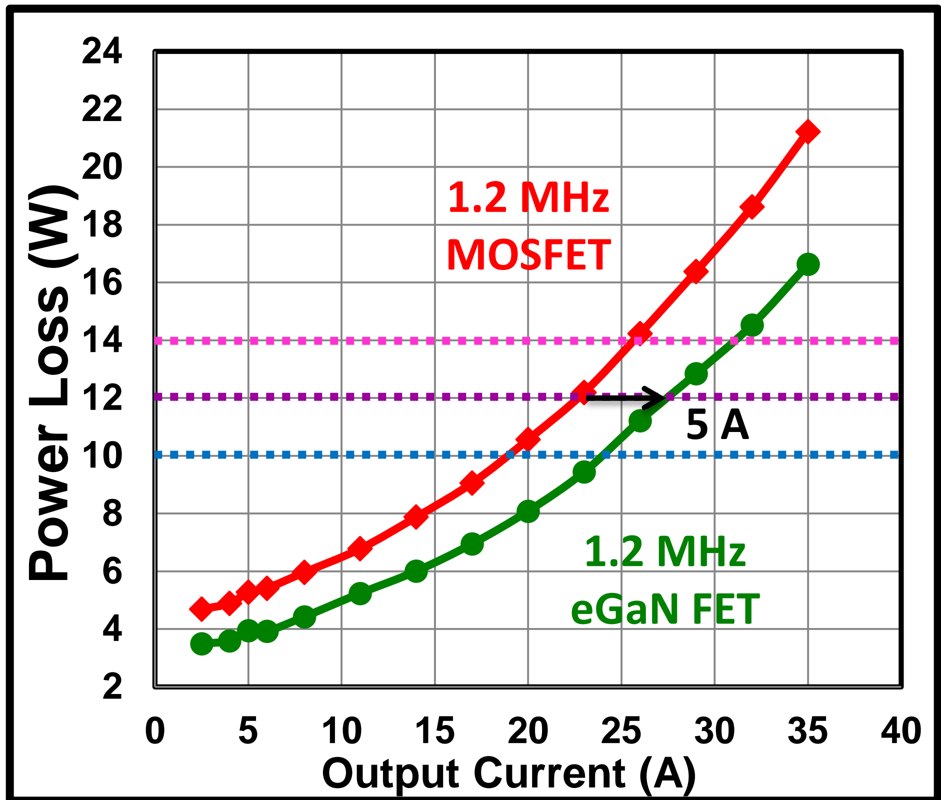
Duty Cycle Comparison



f_{sw} = 1.2 MHz, V_{IN} = 48 V, and $V_{OUT} \approx$ 12 V

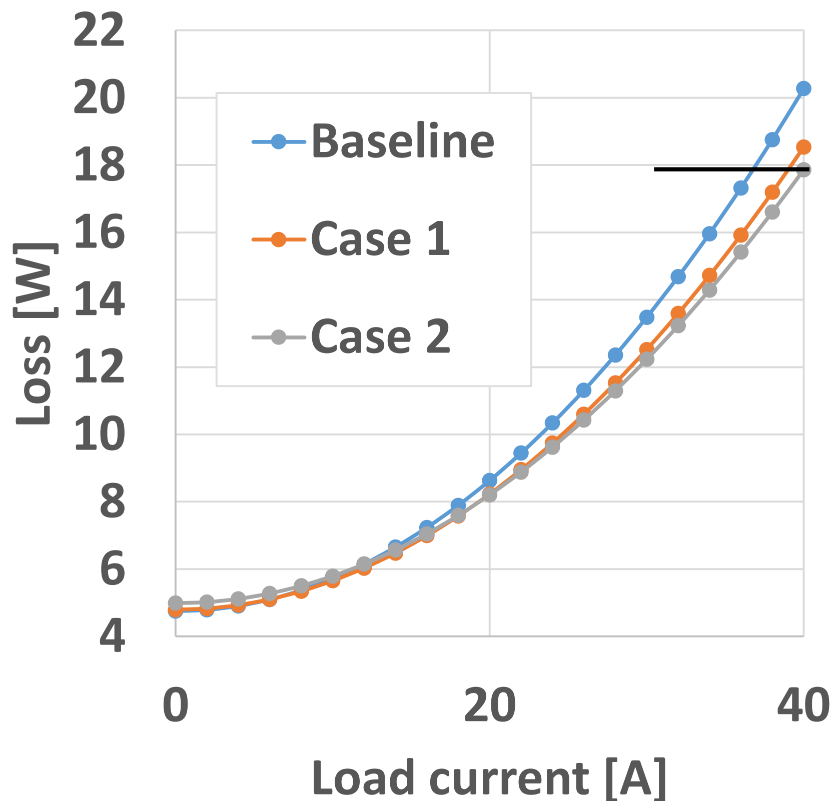
Efficiency Comparison

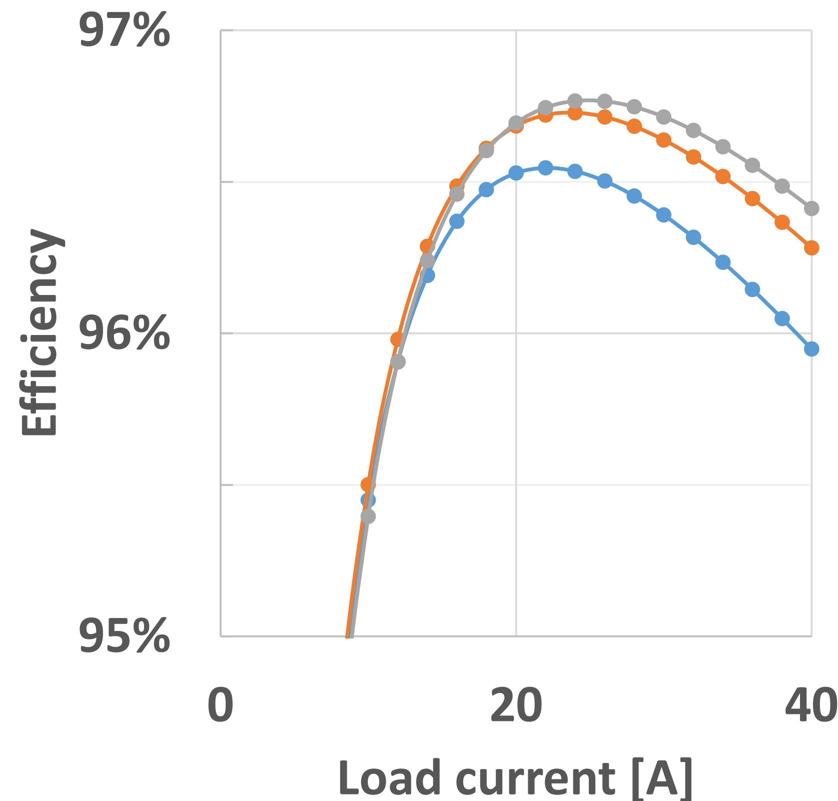




f_{sw} = 1.2 MHz, V_{IN} = 48 V, and $V_{OUT} \approx$ 12 V

Projected results with Latest Generation FETs





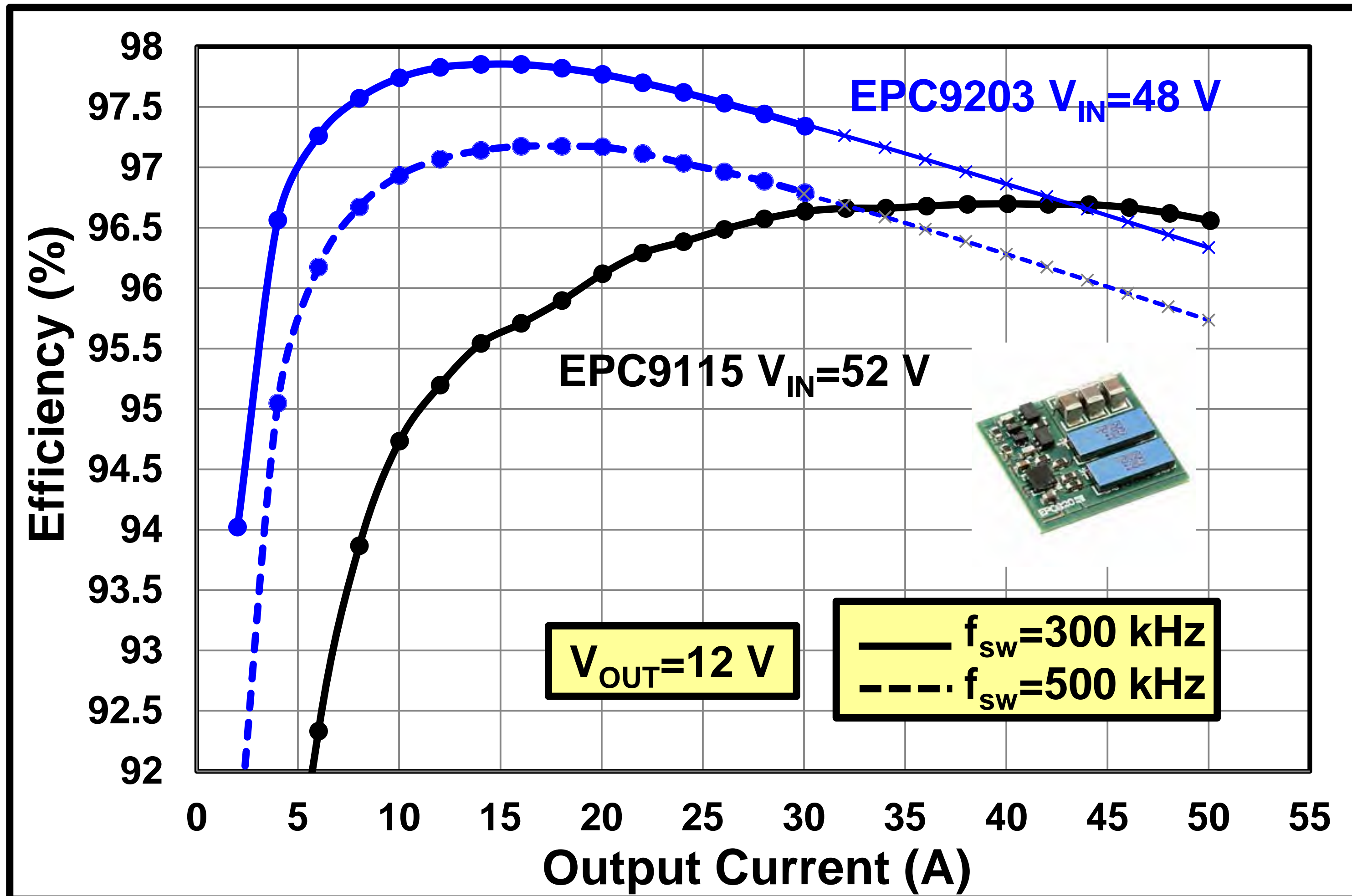
$$P_{loss} = R_{out}\, I_{OUT}^2 + P_{fixed}$$

Non-isolated bus converter

APEC

Efficiency Comparisons

EPC EFFICIENT POWER CONVERSION

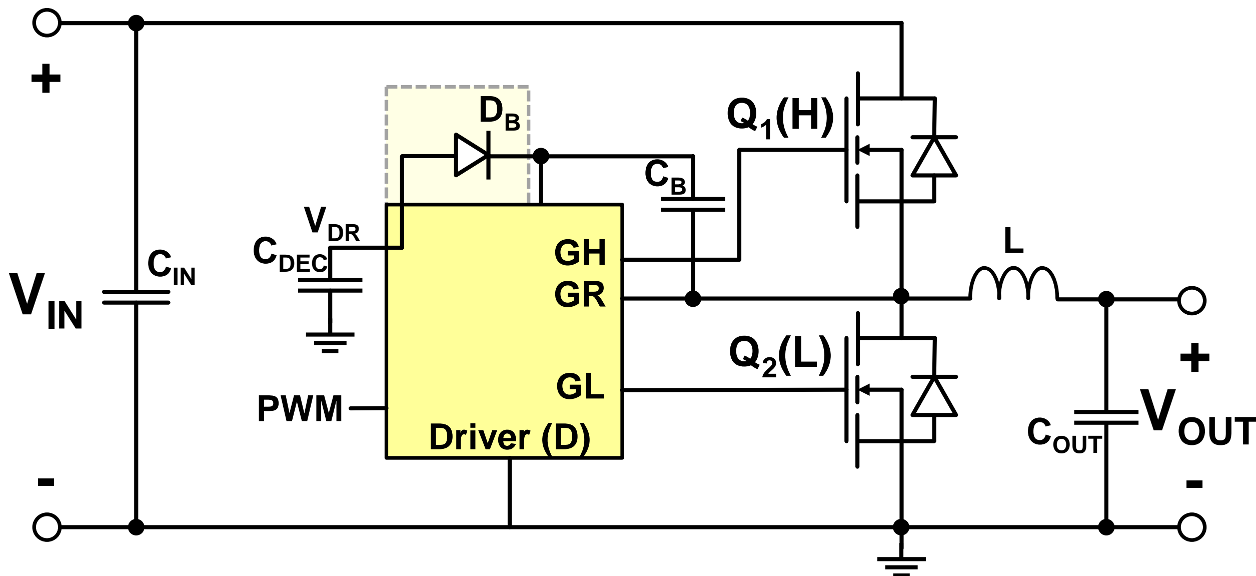


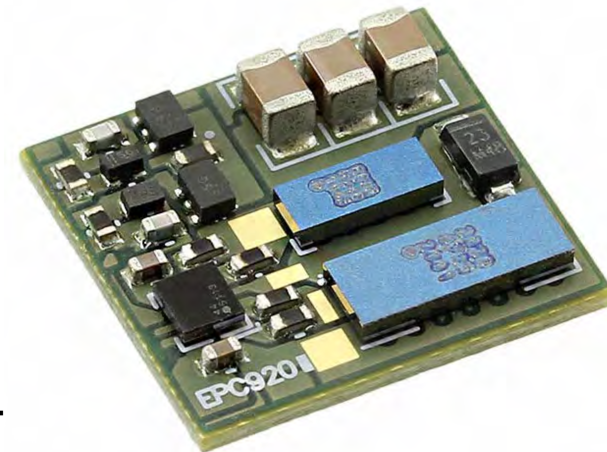
Comparison

	Units	1/8th-brick	Buck
Converter volume	in^3 (cm^3)	0.92 (15)	0.73 (12)
Input voltage	V	49-60	13-65
Output current	A	42	42
Power density	W/in^3 (W/cm^3)	550 (34)	690 (42)
# FETs		8	2
# Gate drivers		4	1
# PCB layers		12	4

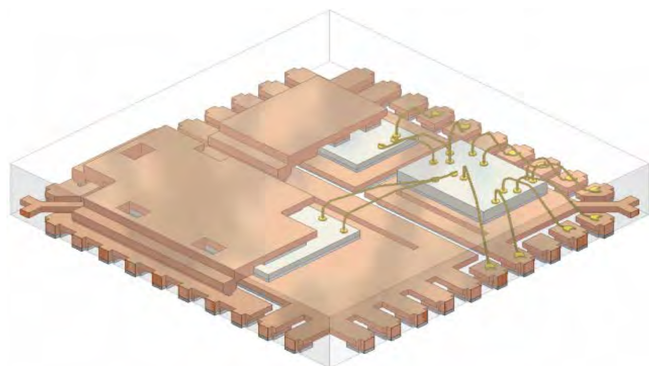
12 V_{IN} to 1 V_{OUT} POL Converter

12 V_{IN} POL Topology

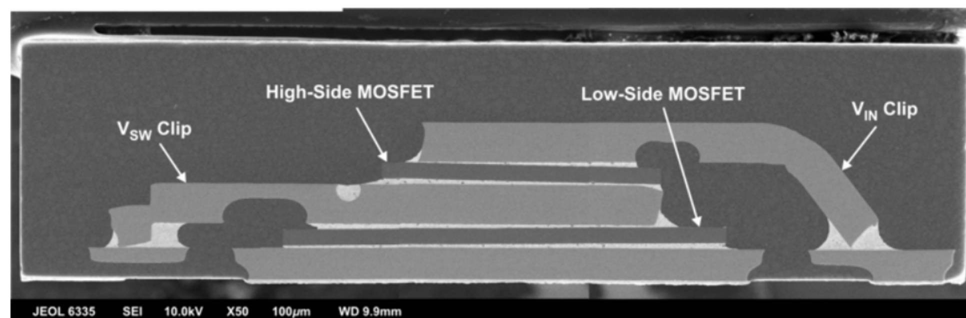




http://media.digikey.com/
photos/EPC/EPC9201.JPG

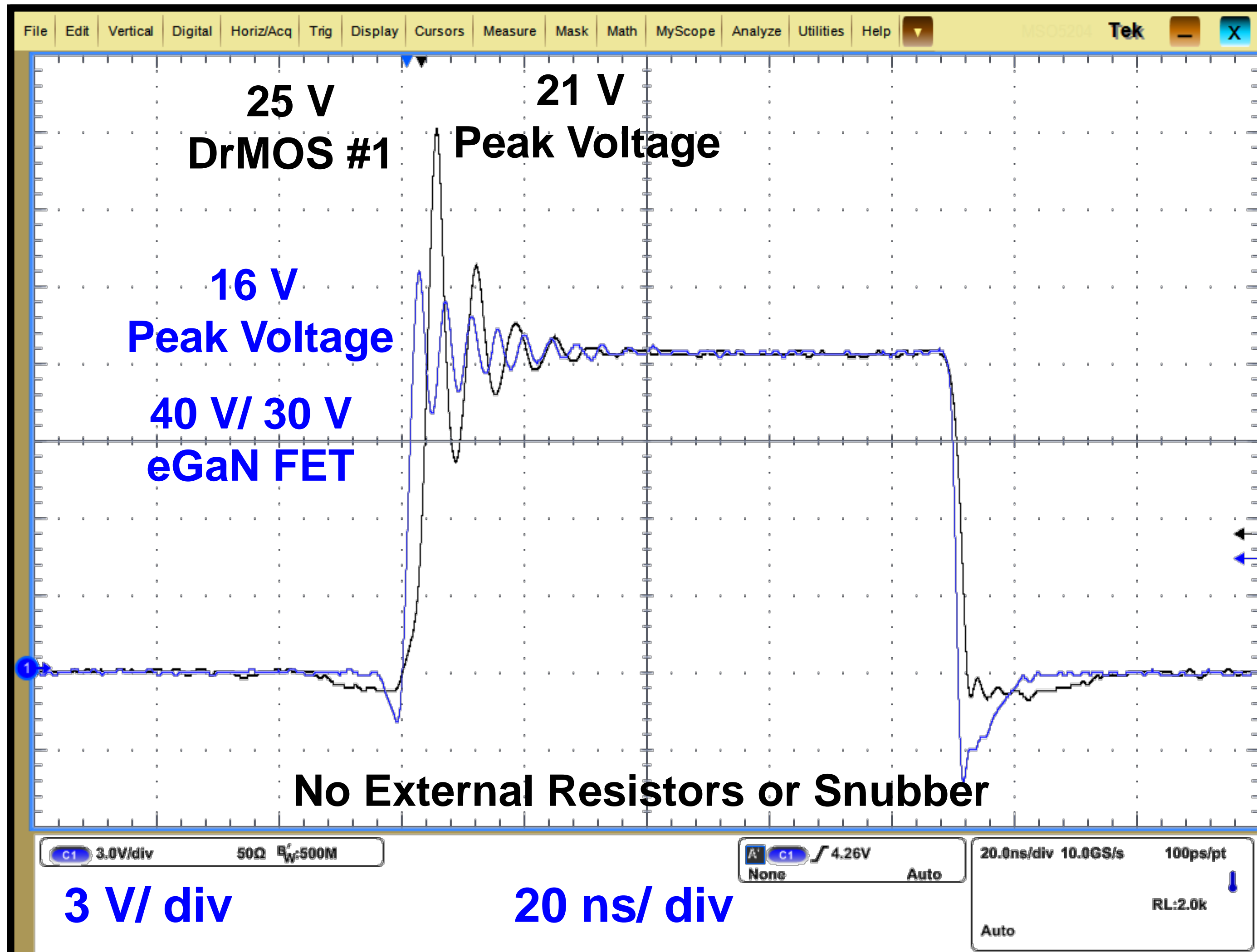


https://www.fairchildsemi.com/collateral/
Generation-II-XS-DrMOS-Family.pdf



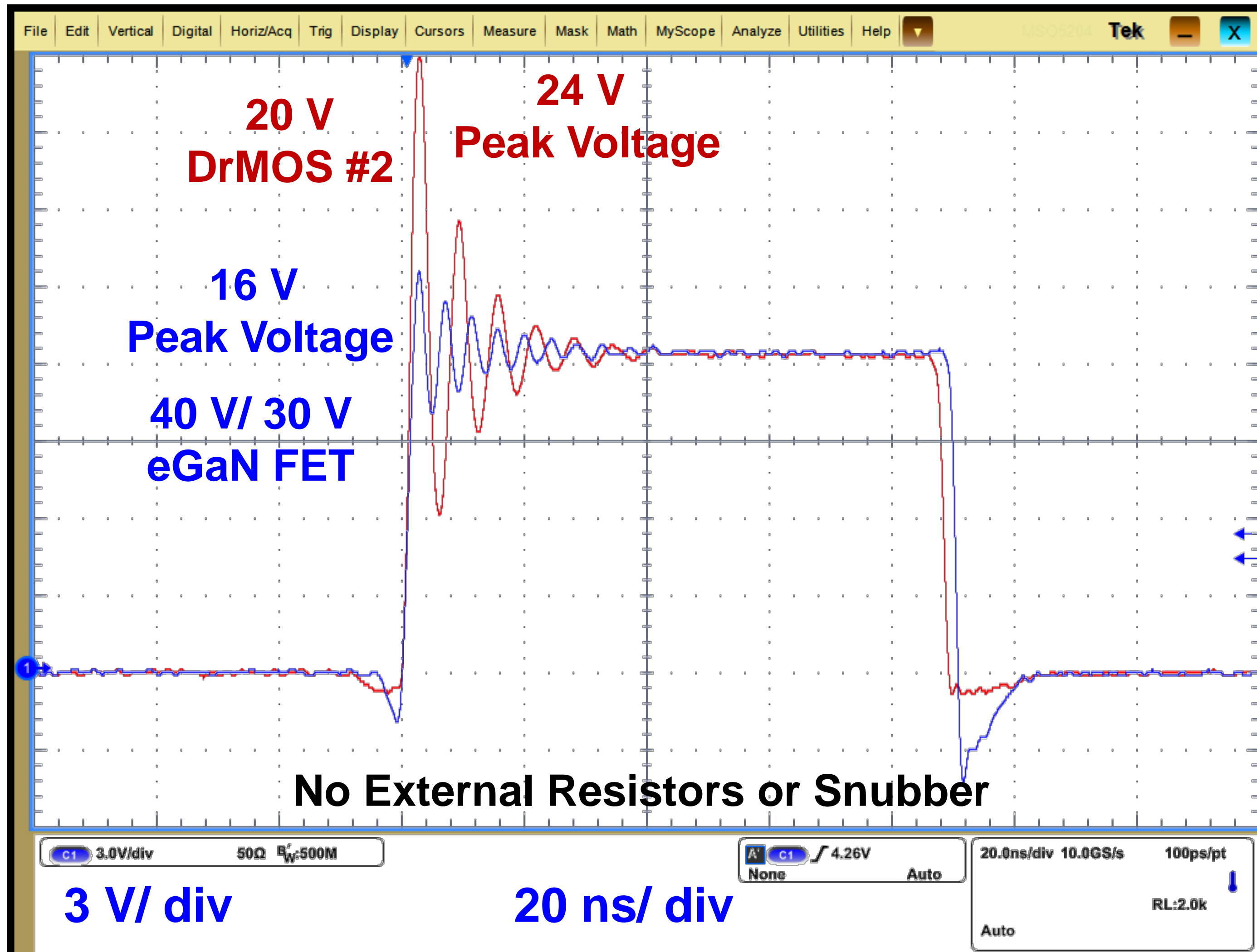
3D packaging advancements drive performance, power and density in power devices
http://www.ti.com/lit/an/slit126/slit126.pdf

Switching Waveforms



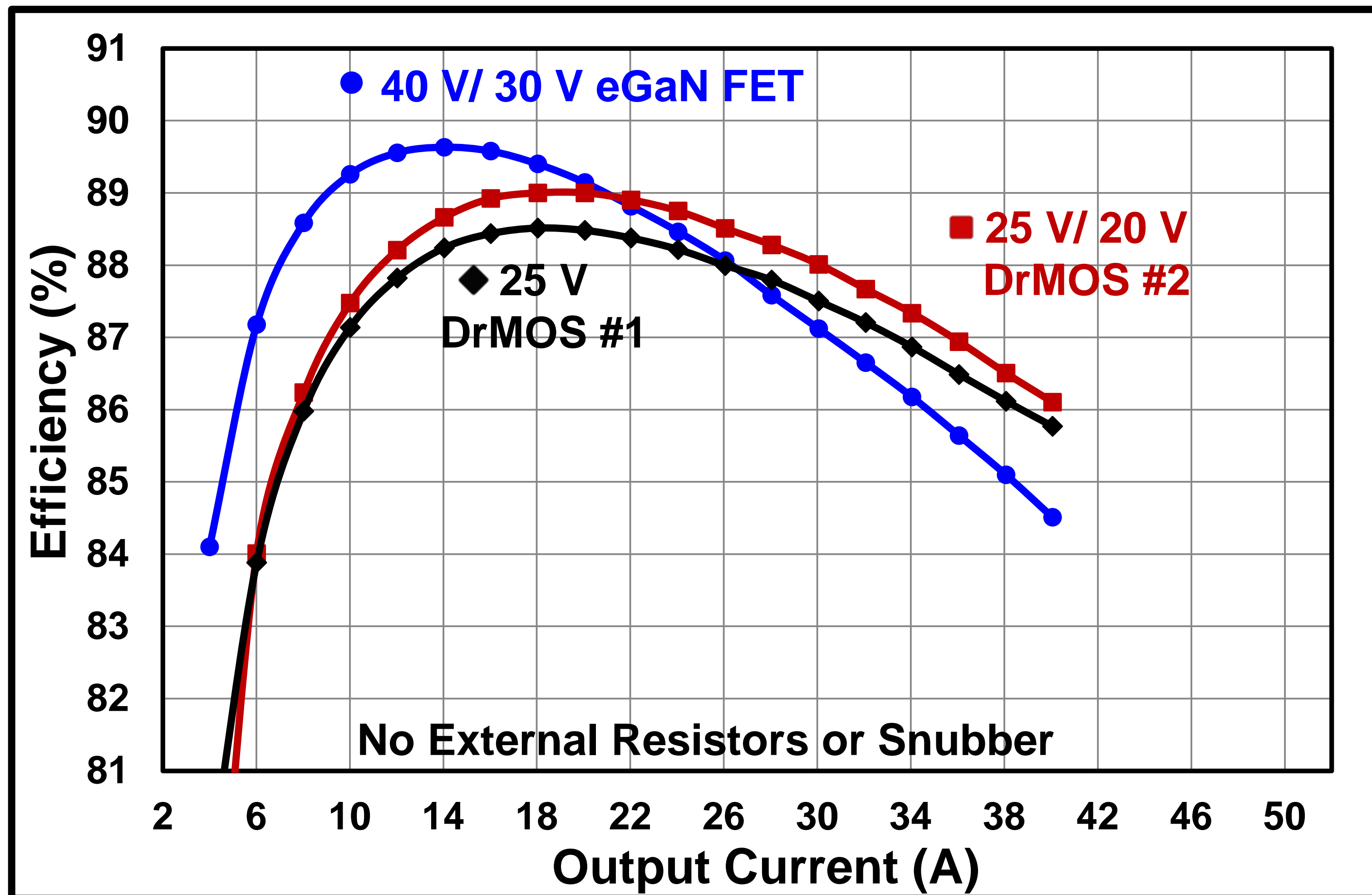
V_{IN}=12 V V_{OUT}=1 V I_{OUT}=20 A f_{sw}=1 MHz L=250 nH

Switching Waveforms



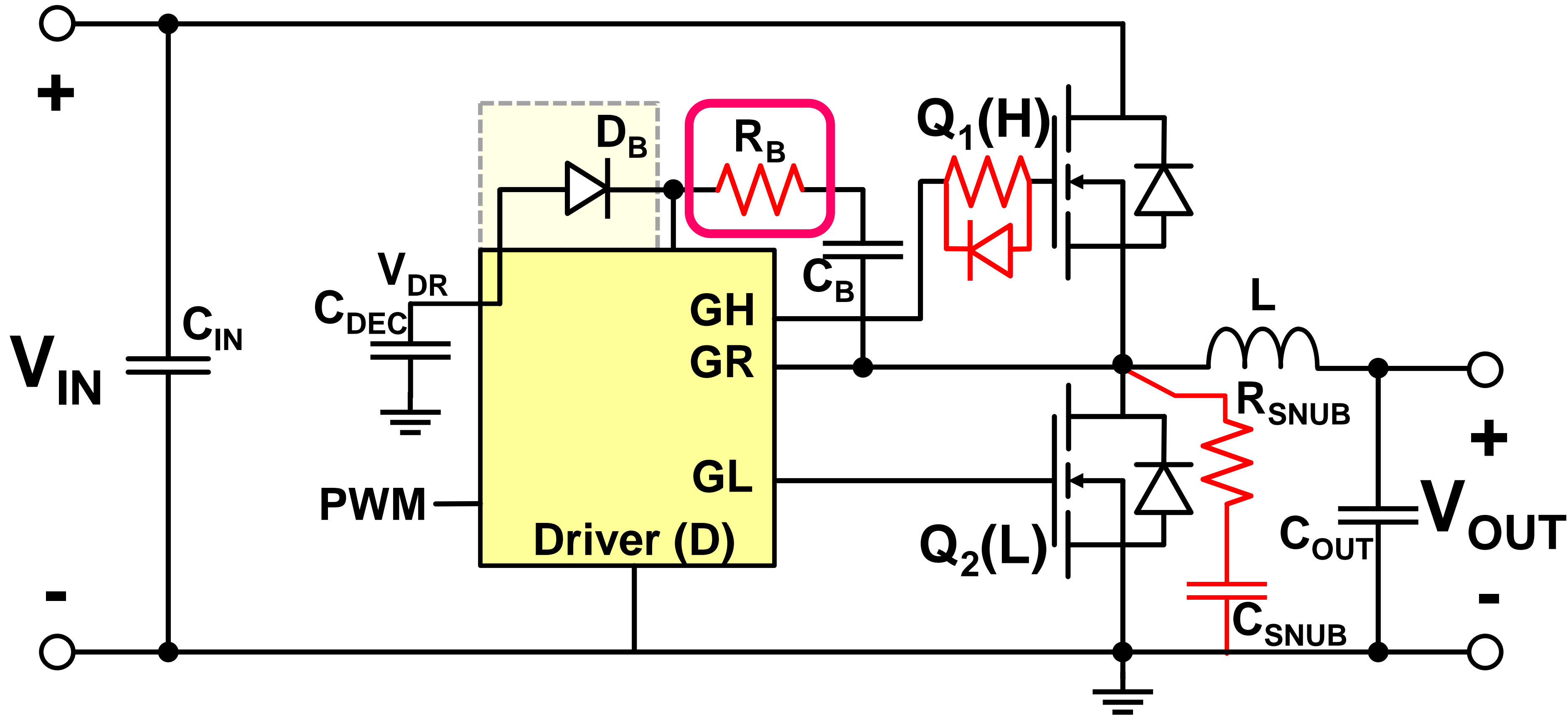
V_{IN}=12 V V_{OUT}=1 V I_{OUT}=20 A f_{sw}=1 MHz L=250 nH

Efficiency Comparisons

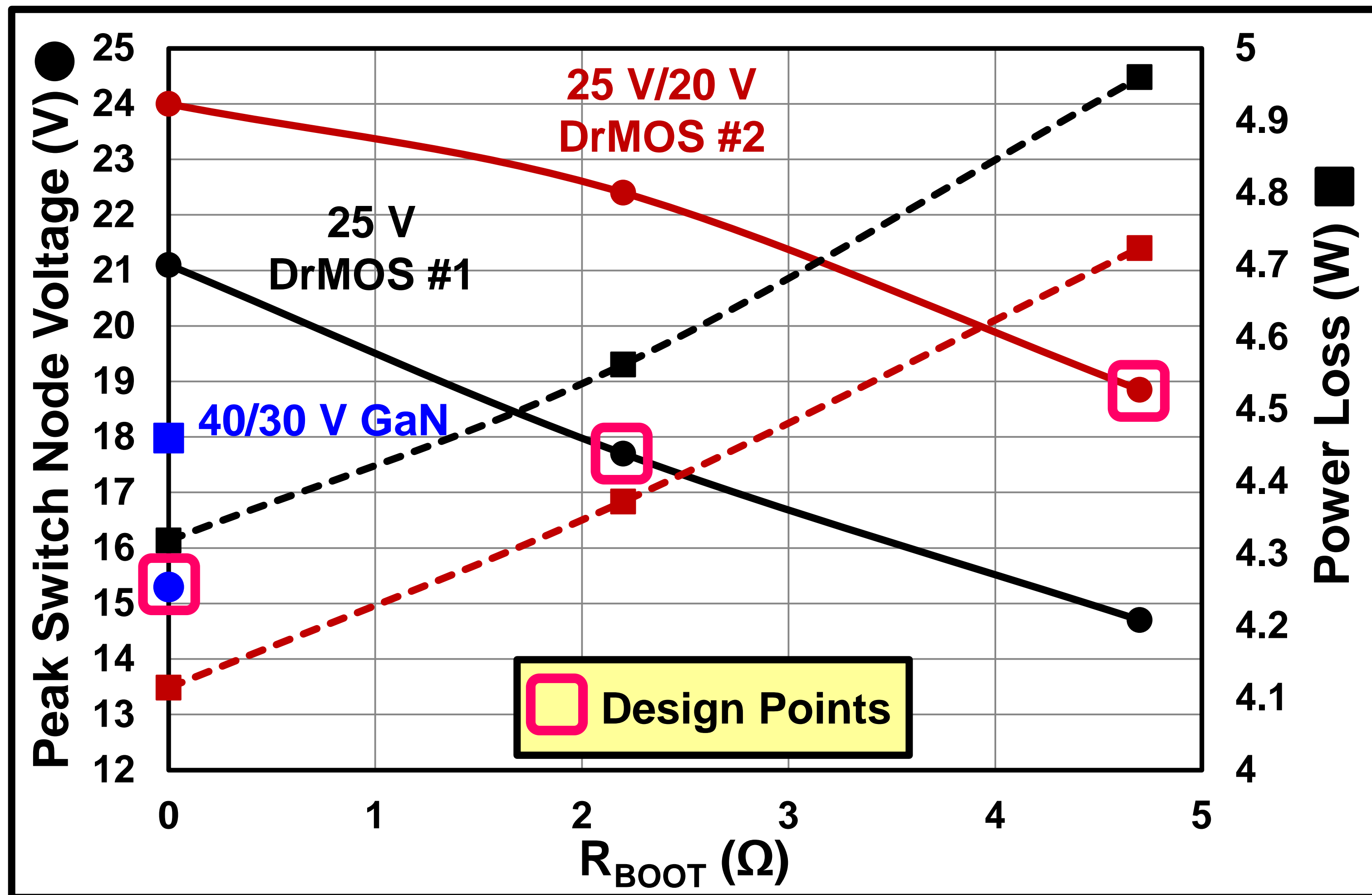


V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz L=250 nH

Managing Voltage Spike

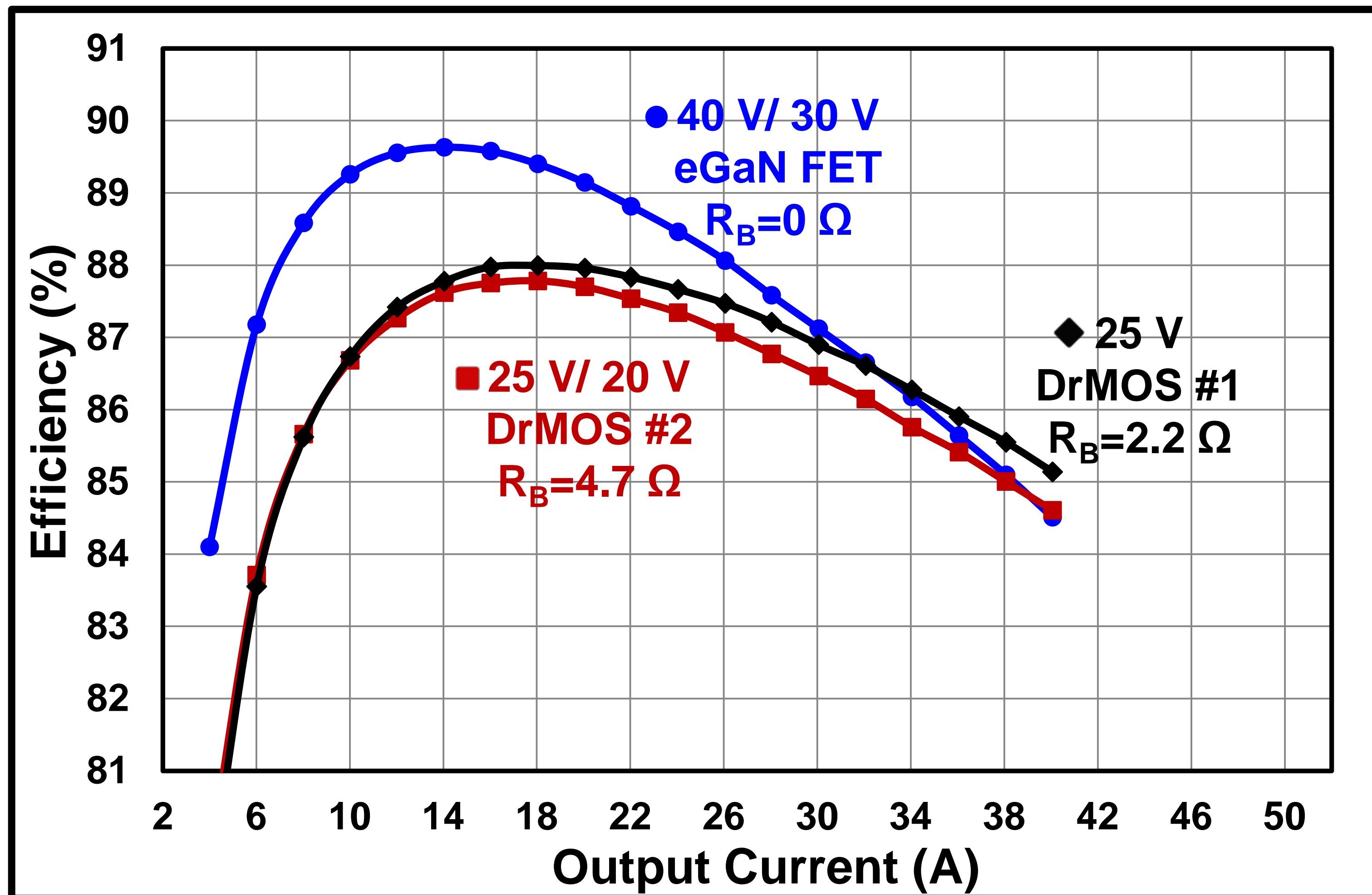


Efficiency Comparisons



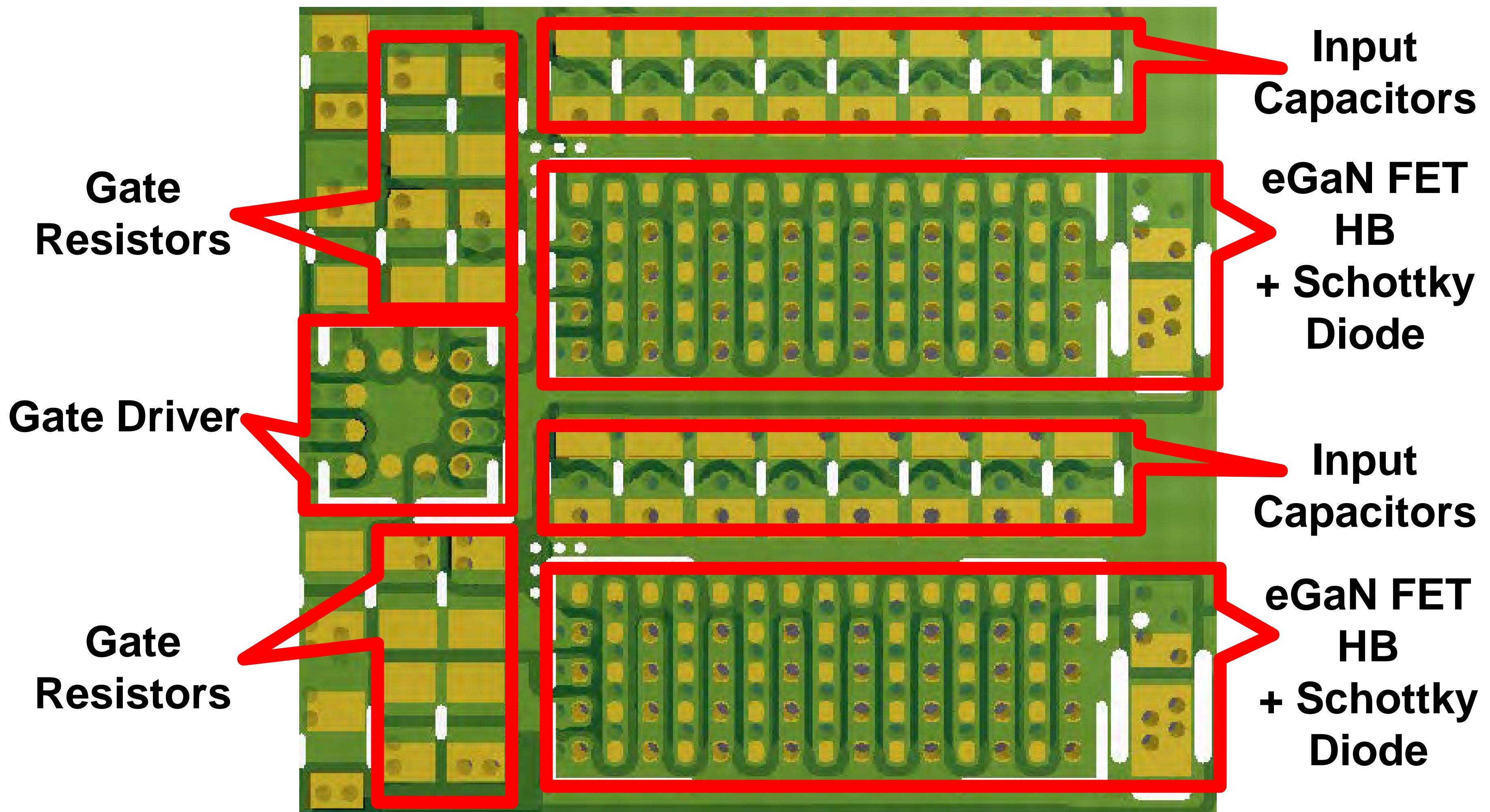
V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz I_{OUT}=30 A L=250 nH

Efficiency Comparisons

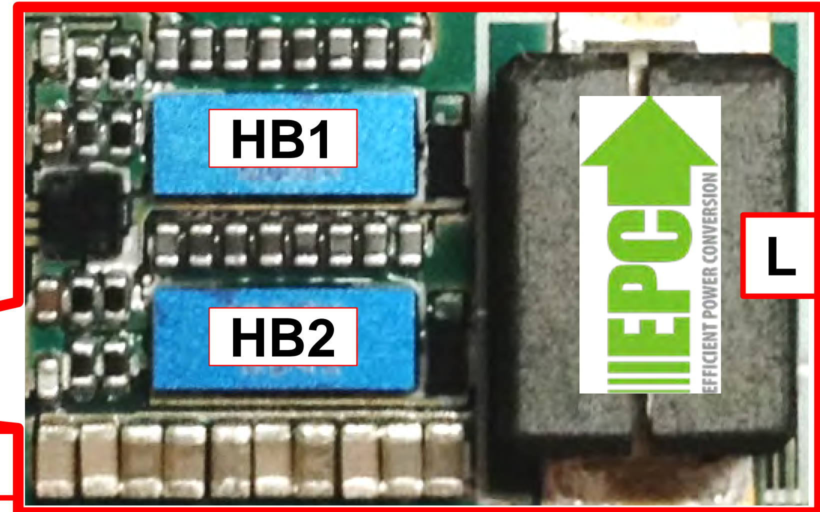


V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz L=250 nH

High Current GaN POL



High Current GaN POL

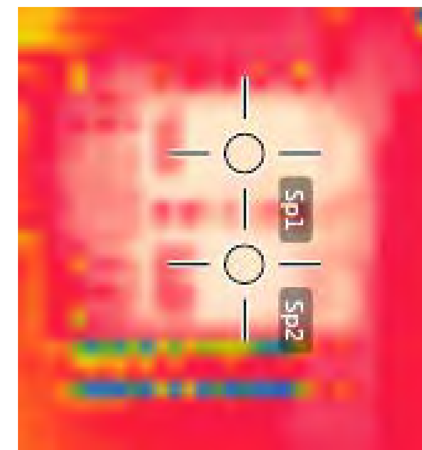


HB1 ≈ 103°C

HB2 ≈ 101°C

100°C

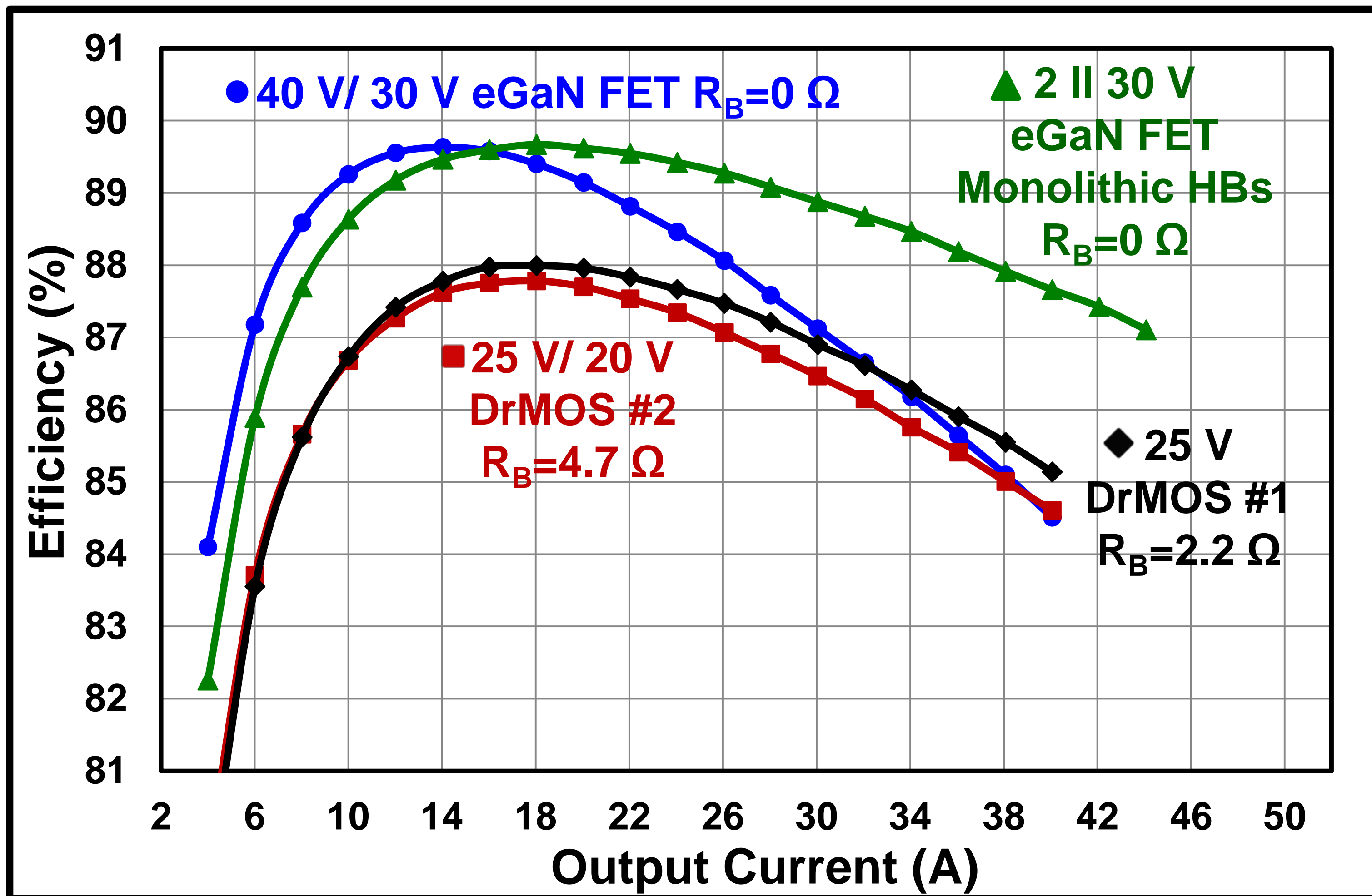
25°C



Natural Convection

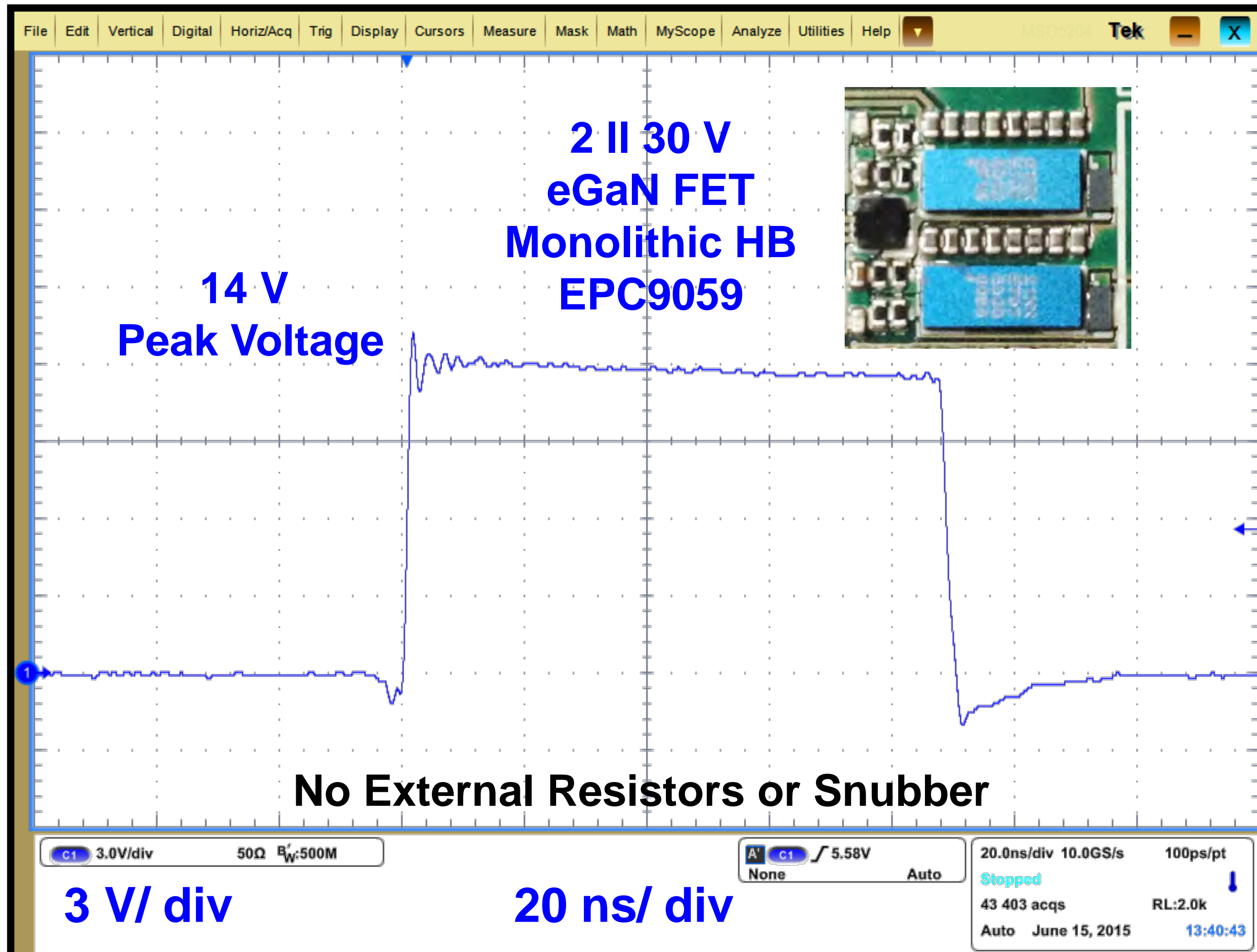
V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz I_{OUT}=32 A

High Current GaN POL



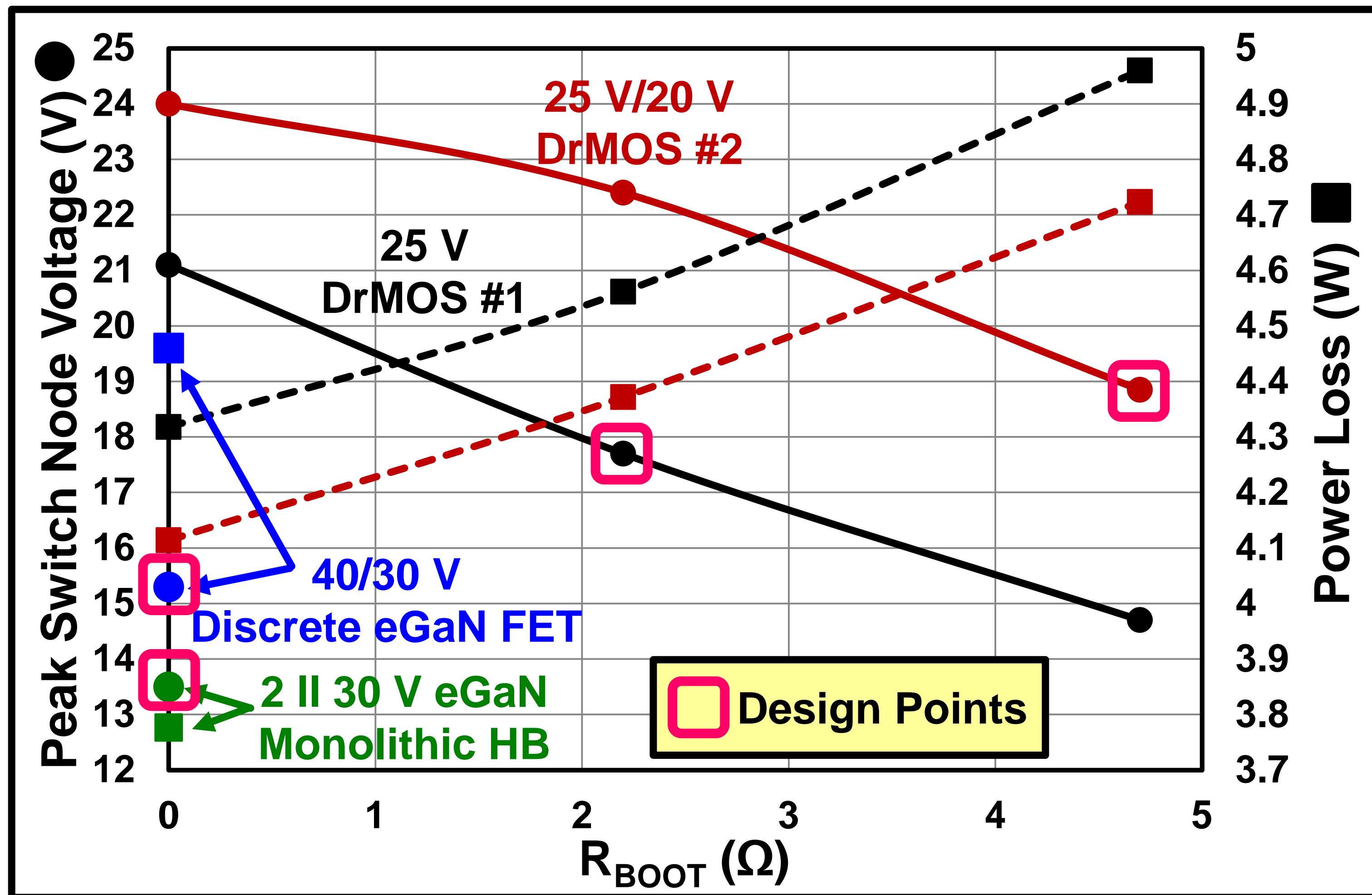
V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz L=250 nH

High Current GaN POL



V_{IN}=12 V V_{OUT}=1 V I_{OUT}=20 A f_{sw}=1 MHz L=250 nH

Design Comparisons

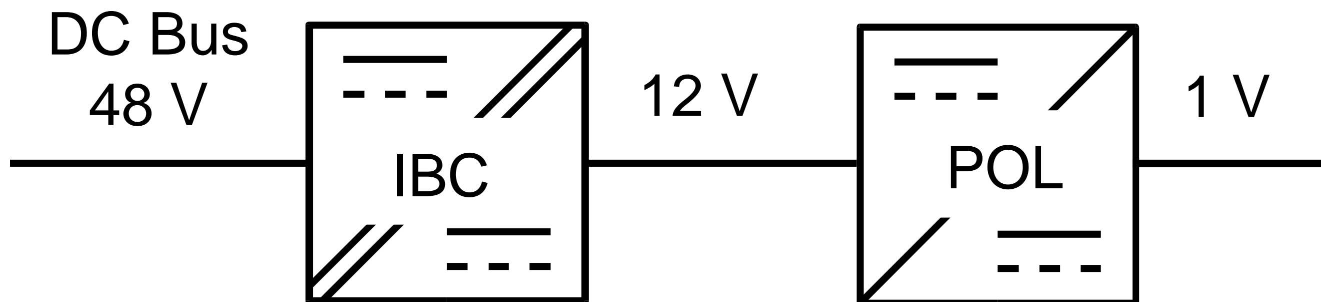


V_{IN}=12 V V_{OUT}=1 V f_{sw}=1 MHz I_{OUT}=30 A L=250 nH

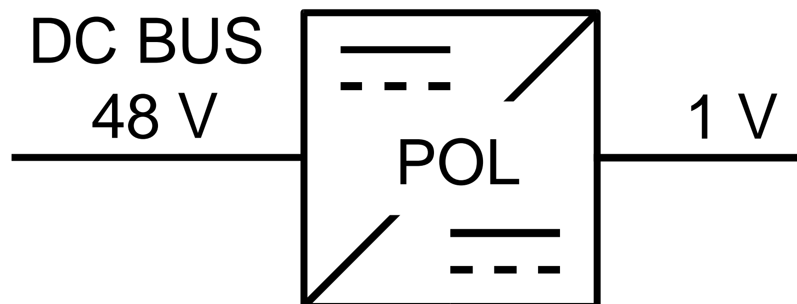
48 V_{IN} to 1 V_{OUT} POL Converter

48 V_{IN} to LOAD

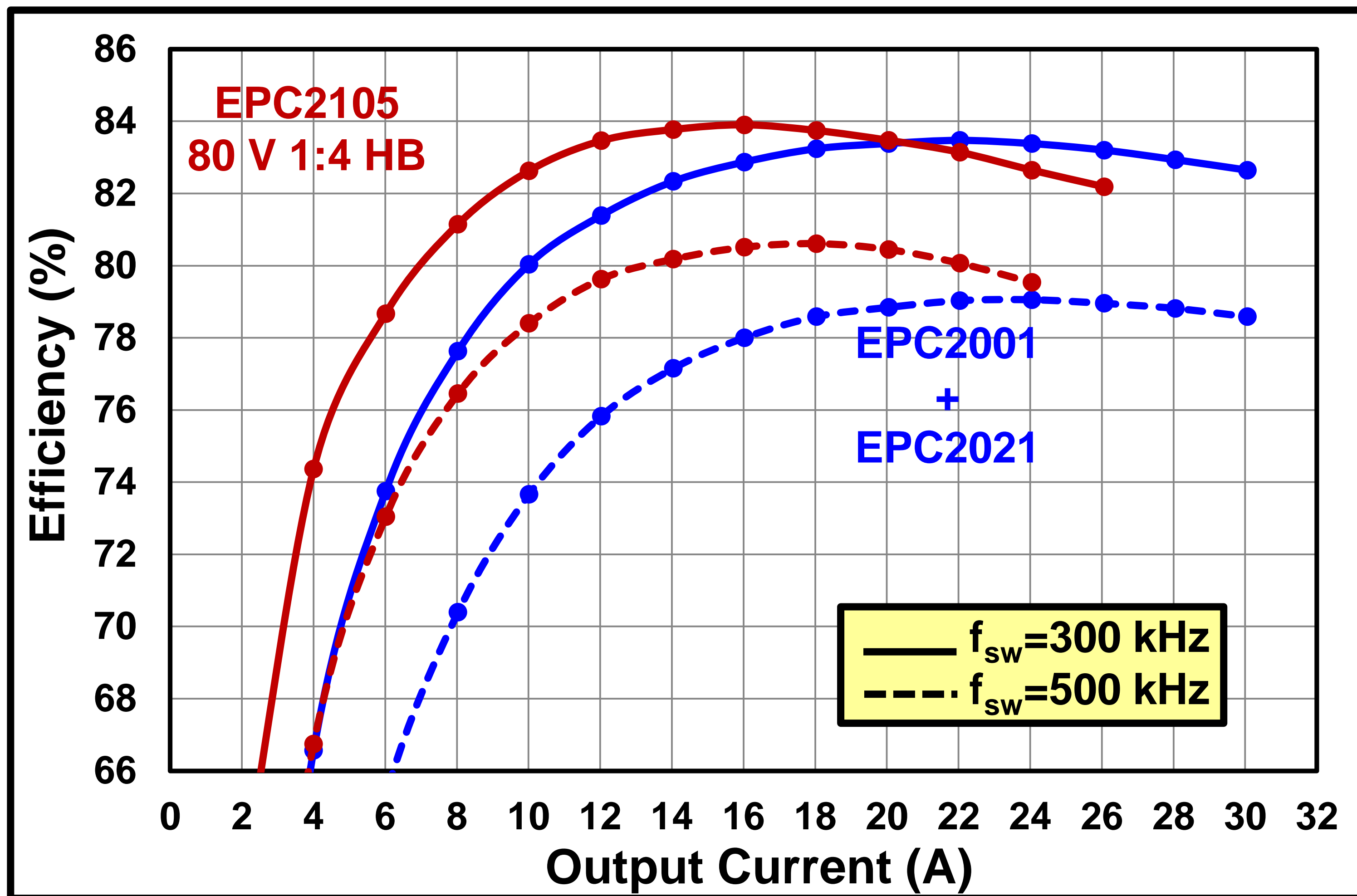
Intermediate Bus Architecture



DC Bus Architecture



48 V_{IN} to LOAD



V_{IN}=48 V V_{OUT}=1 V L=330 nH

48 V_{IN} to LOAD

Intermediate Bus Architecture

DC Bus
48 V

96%

IBC

98%
12 V

88%

POL

1 V

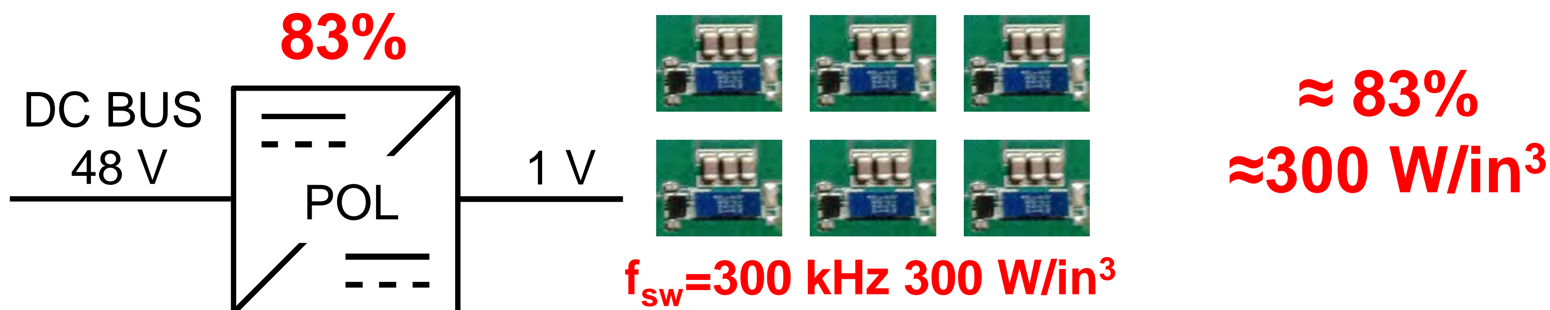
f_{sw}=300 kHz 550 W/in³

f_{sw}=1 MHz 500 W/in³

96% x 98% x 88%
≈ 83%
≈250 W/in³

DC Bus Architecture

83%



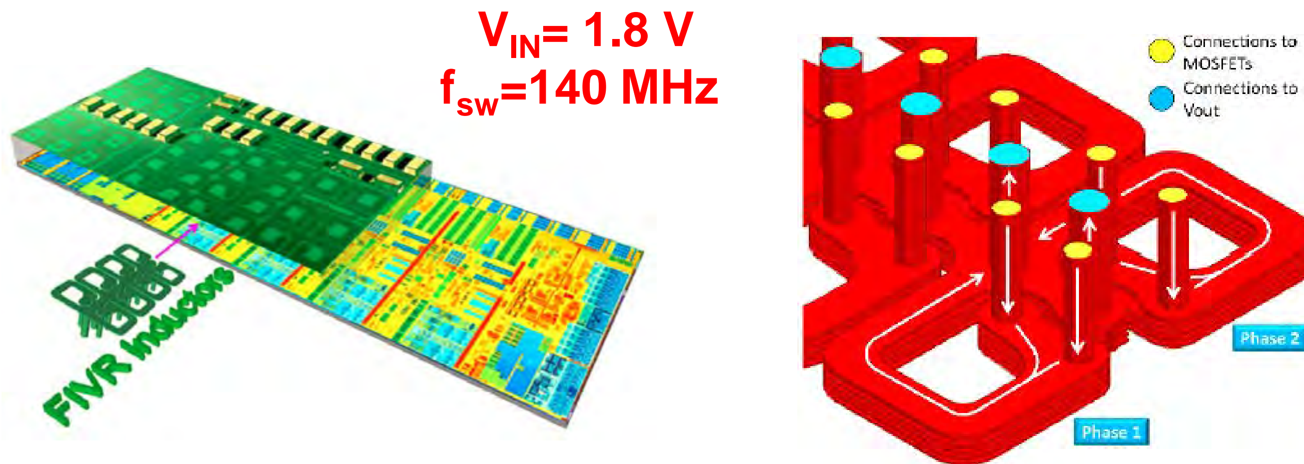
f_{sw}=300 kHz 300 W/in³

≈ 83%
≈300 W/in³

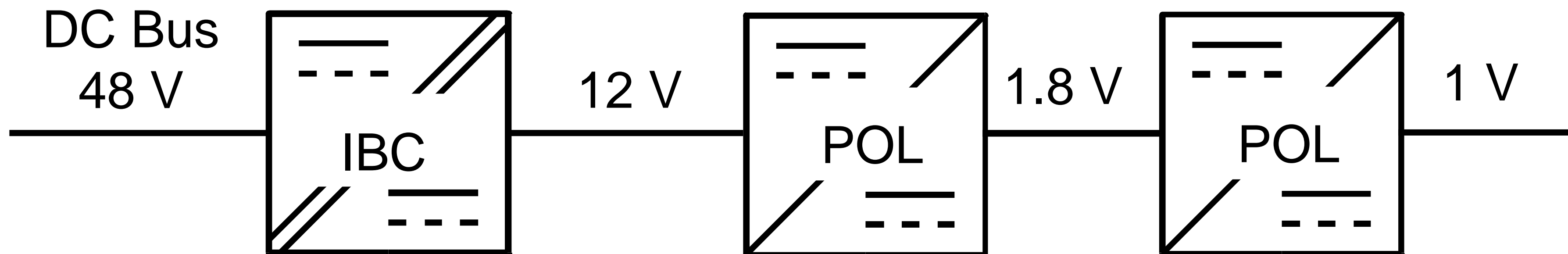
48 V_{IN} to 1.8 V_{OUT} Bus Converter

Integrated VR Architecture

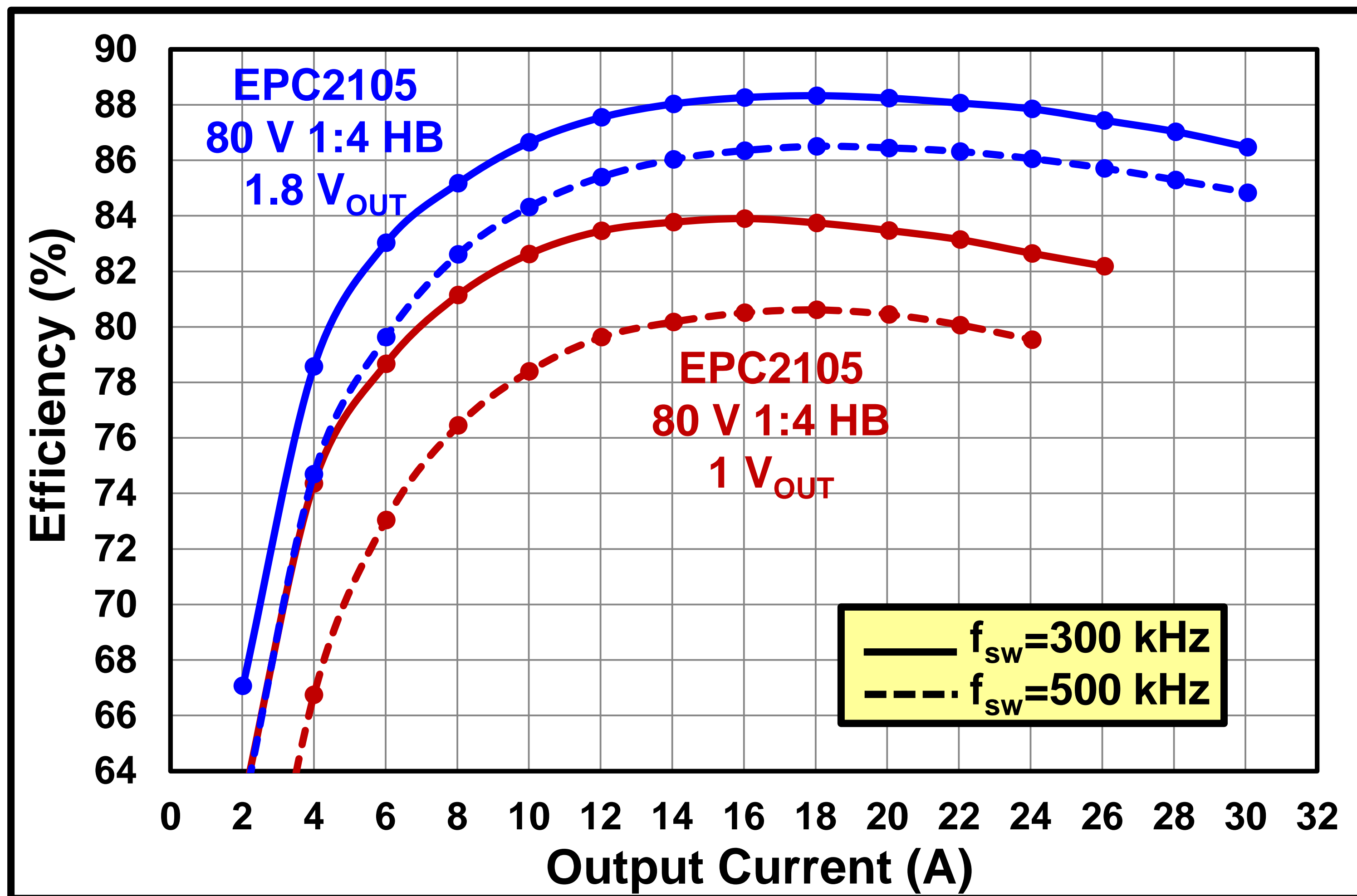
"FIVR – Fully Integrated Voltage Regulators on 4th Generation Intel® Core™ SoCs" APEC2014



Three Stage Intermediate Bus Architecture

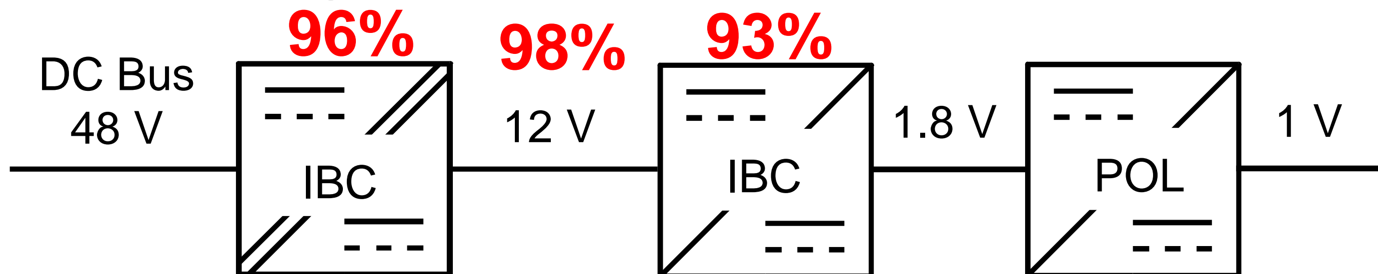


48 V_{IN} to Integrated VR

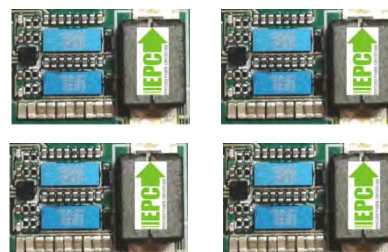


V_{IN}=48 V V_{OUT}=1 V L@ 1V_{OUT}=330 nH V L@1.8 V_{OUT}=470 nH

Three Stage Intermediate Bus Architecture



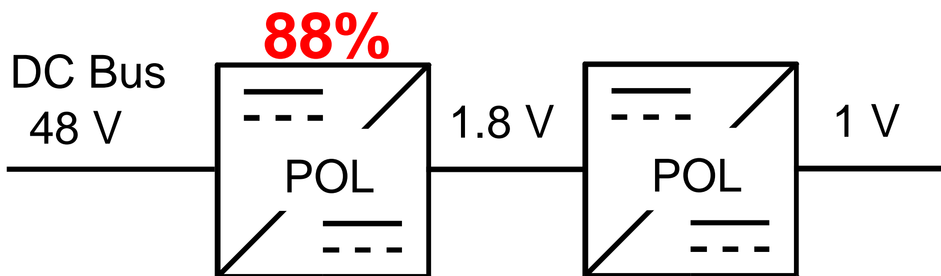
f_{sw}=300 kHz 550 W/in³

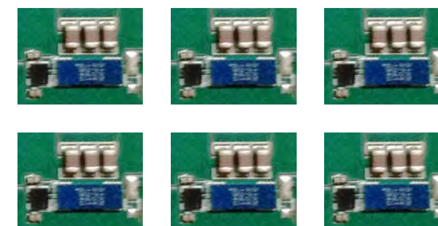


f_{sw}=1 MHz 700 W/in³

96% x 98% x 93%
≈ 88%
≈300 W/in³

Two Stage Non-Isolated Intermediate Bus Architecture





f_{sw}=300 kHz 500 W/in³

≈ 88%
≈500 W/in³

Power Architecture Comparison

Parameter	Units	48 V_{IN} IBA		48 V_{IN} Direct Conversion
		48 V_{IN} – 12 V_{OUT} IBC	12 V_{IN} – 1.8 V_{OUT} IBC	48 V_{IN} – 1.8 V_{OUT} IBC
Stage Switching Frequency	kHz	300	1000	300
Total Power Devices[a]		22 [b]		18 [b]
System Transformer Isolation		Yes		No
PCB Complexity		High	Low	Low
Stage Efficiency	%	96	93	88
Bus Efficiency	%	98[c]		99.9%
Total System Efficiency	%	87.5		87.9
Stage Power Density	W/in^3 (W/cm^3)	550 (34)	700 (43)	500 (31)
Total System Power Density	W/in^3 (W/cm^3)	300 (18)		500 (31)
Total System Cost		High		Low

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Summary

EPC EFFICIENT POWER CONVERSION

- Initial comparison of Intermediate Bus Architecture and non-isolated DC Bus Architecture for Integrated VR
  - Cost of non-isolated converter will be **much** lower
  - Redundant 12 V_{IN} can be removed
  - Efficiency is similar, power density can be higher
  - Transient no longer a concern
- Potential improvements
  - 48 V_{IN} to 1.8 V_{OUT} isolated bus converter may provide higher efficiency

A Look into the Future

Breaking Down the Barriers

- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

Breaking Down the Barriers

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- Is it easy to use?
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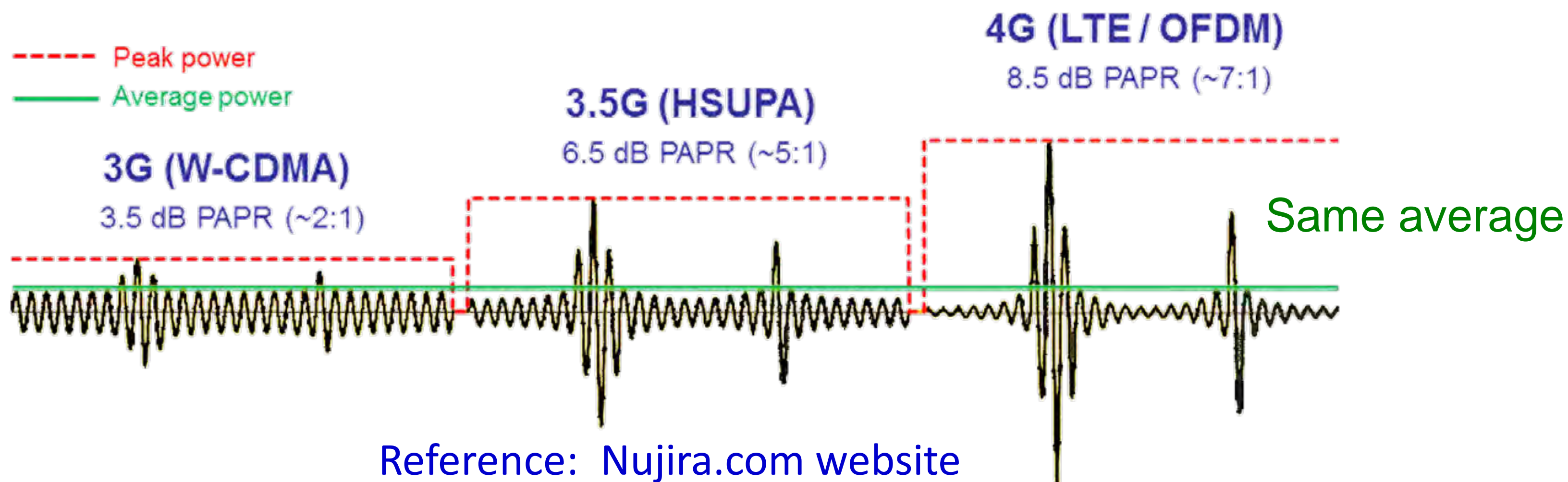
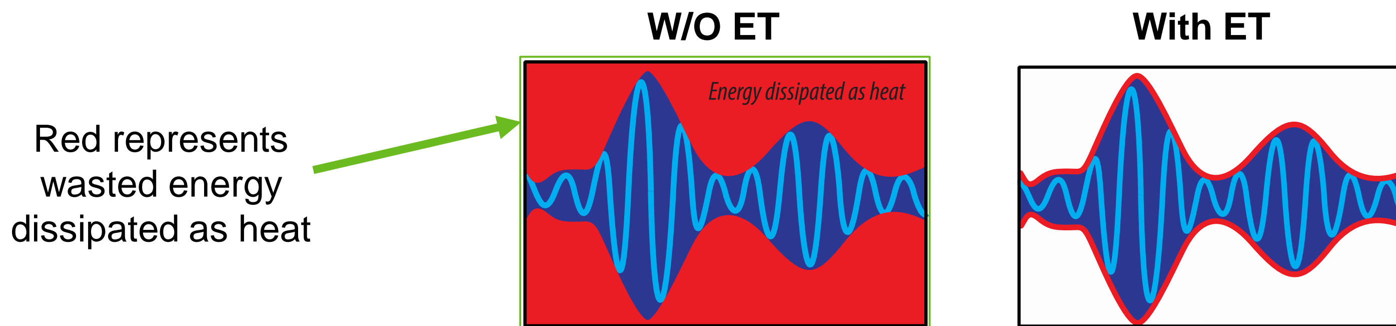
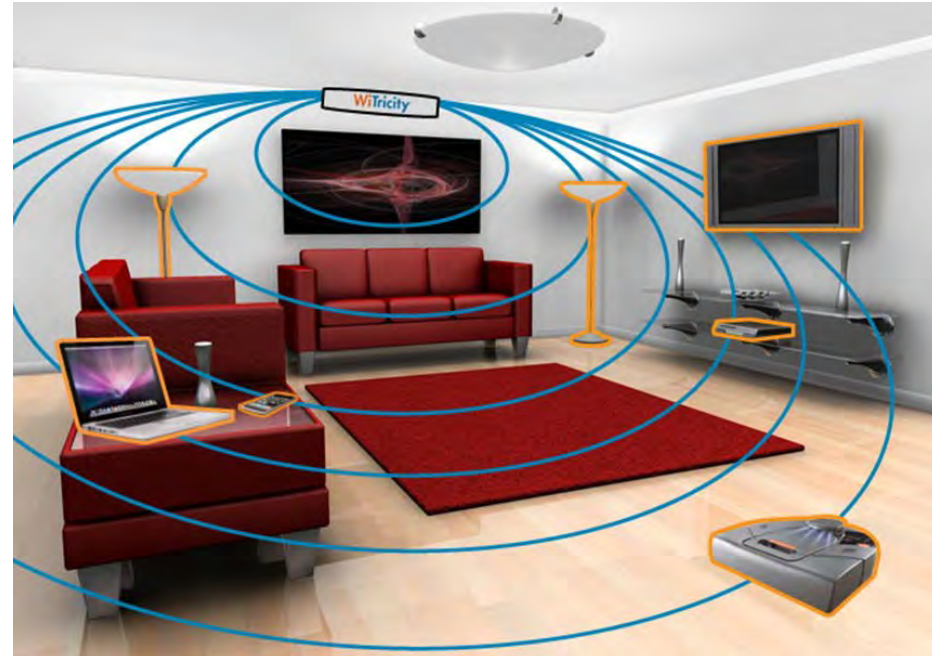
More Wireless Bandwidth



Reference: Nujira.com website



No Power Cords



Augmented Reality and Autonomous Cars

Other Key Applications

- RadHard
- Energy Efficient Lighting
- Class D Audio
- Various Medical

Breaking Down the Barriers

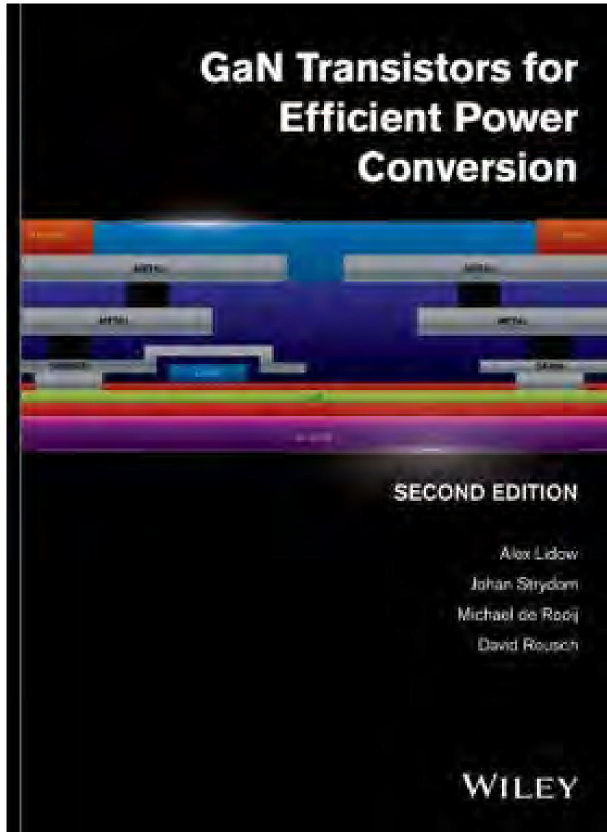
- Does it enable significant new capabilities?
- Is it easy to use?
- Is it VERY cost effective to the user?
- Is it reliable?

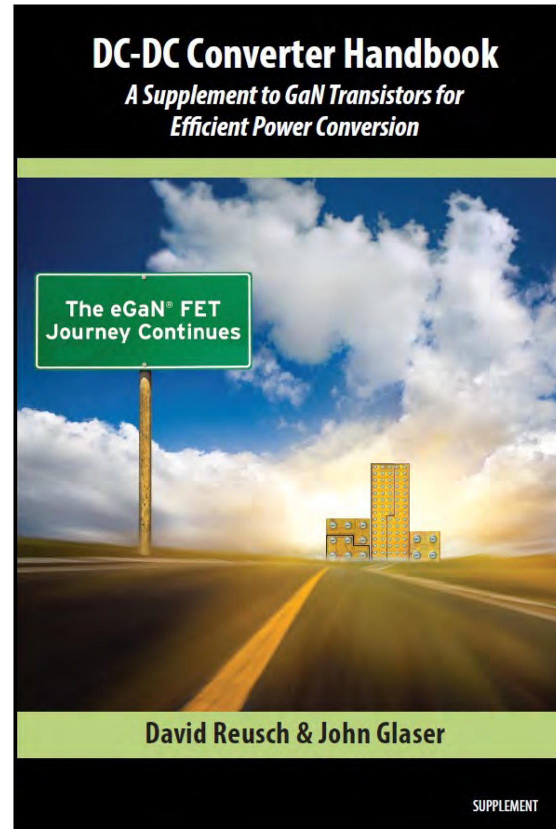
Is an eGaN FET Easy to Use?

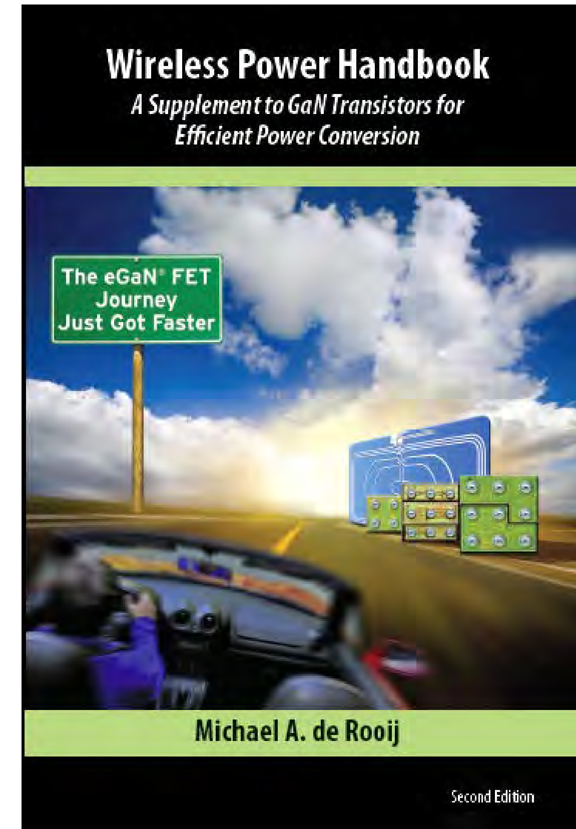
It's just like a MOSFET

except

The high frequency capability makes circuits using eGaN FETs sensitive to layout


GaN Transistors for Efficient Power Conversion
SECOND EDITION
Alex Lidow
Johan Strydom
Michael de Rooij
David Reusch
WILEY


DC-DC Converter Handbook
A Supplement to GaN Transistors for Efficient Power Conversion
The eGaN® FET Journey Continues
David Reusch & John Glaser
SUPPLEMENT


Wireless Power Handbook
A Supplement to GaN Transistors for Efficient Power Conversion
The eGaN® FET Journey Just Got Faster
Michael A. de Rooij
Second Edition

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Universities with GaN Transistor Programs

EPC EFFICIENT POWER CONVERSION

Universities all over the world are graduating well-trained engineers experienced in the use of GaN Transistors

- Virginia Tech
- MIT
- Auburn University
- National Chiao Tung University
- Zhejiang University
- Kyusu Institute of Technology
- University of Tennessee
- University of Illinois
- University of Southern Denmark
- University of Texas
- North Carolina State University
- University of Valencia
- Universität Kassel
- Case Western University
- Colorado State University
- University of Sheffield
- Delft University of Technology
- National Tsing Hua University
- Yamaguchi University
- FH Joanneum - University of Applied Sciences
- University of Cambridge
- Rensselaer Polytechnic Institute
- ETH Zurich
- University of Michigan
- Nanyang Technological University
- Hong Kong University
- Aalborg University
- University of Toronto
- Universidad Miguel Hernandez
- Mid Sweden University
- RFSS Lab
- New Mexico State University
- Seoul Technical University
- Clausthal University of Technology
- Universita Di Padova
- University of Johannesburg
- University of North Carolina - Charlotte
- Oregon Tech
- DEEEA-ETSE URV
- University of Maryland
- University of Stuttgart
- The Hong Kong University of Science & Technology
- Tallinn University of Technology
- Harvard University
- University of Toledo
- University of Akron
- University of Dayton
- University of Zaragoza
- Stanford University
- University of Applied Sciences
- University of Bologna
- Missouri University
- University of Wisconsin
- Yale University
- Reutlingen University
- Kyushu University
- Ecomas
- Universidad de Oviedo
- University of Arkansas
- Chiba University
- Shimane University
- University of Florida
- University of Bristol
- Universitat Erlangen
- Seoul National University
- University of Hamburg - Institute of Experimental Physics
- Otto-Von-Guerick University
- City University of Hong Kong
- National Central University
- Missouri University of Science and Technology
- DTU Elektro
- Florida State University
- University of North Carolina
- University of Auckland
- Universidad Politenica de Madrid
- UCLA
- Universita di Roma la Sapienza
- Purdue University
- Oita University
- Arizona State University
- University of South Carolina
- University of Utah
- Catholic University of Leuven
- LAPLACE
- Pontifical Xavierian University
- Macquarie University
- Austrian Institute of Technology GmbH
- Auckland University of Technology
- Friedrich-Alexander University
- University of Warwick
- Centro De Estudios E Investigaciones
- Supelec
- University of Nottingham
- Universitat Rovira i Virgili
- University of Waikato
- University of Bremen
- Ferdinand-Braun-Institut
- The Ohio State University
- Bloomsburg University
- Queens University
- Pennsylvania State University
- University of Central Florida
- University of Nevada
- University of Manchester
- NTB Hochschule Fur Technik
- University of Hong Kong
- Iowa State University
- Newcastle University
- Imperial College
- Faculte Des Sciences
- Braunschweig University of Technology
- Center for Advanced Power Systems
- University of New South Wales
- Flensburg University of Applied Sciences
- ASIC Lab
- Universite Lille
- Xian JiaoTong Electric
- Queensland University of Technology
- Institute of Technology Sligo
- Dresden University of Technology
- Concordia University ECE
- Korea University
- National University of Colombia
- Universitat Politecnica de Catalunya - EETAC
- Dalhousie University
- Xi'An Jiaotong University
- Federal University of Santa Catarina
- University of Hannover
- Nikhef Institute
- University of Connecticut
- Brunel University
- UC Santa Barbara
- Oregon State University
- University of Applied Sciences Rosenheim
- Instituto de Telecomunicacoes
- Lausitz University
- SUPSI-TTHF Lab
- Naval Postgraduate School
- Texas Tech University
- Curtin University
- Pukyong National University
- Soongsil University
- Space Flight Lab - UTIAS
- National Taiwan University
- University of Pittsburgh
- University of Colorado
- University of Cassino
- Ruhr University Bochum
- University of Zagreb
- Technische Universitaet Berlin
- Integrated System Research Lab
- Denmark Technical University
- University of Washington
- Embry-Riddle Aeronautical University
- Georgia Tech
- Mississippi State University
- Hogeschool van Amsterdam - University of Applied Sciences
- Oregon Institute of Technology
- LS Simulation - Imtek
- University of Applied Sciences Ravensburg-Weingarten
- University of Oulu
- Beijing Jiaotong University
- University of Applied Science Austria
- Sun Yat-Sen University
- Hongik University
- Nagasaki University
- Dartmouth College
- Hochschule Kempten - University of Applied Sciences
- Singapore University of Technology and Design
- Université Laval
- University of Parma
- University of Iowa
- Harbin Industry University
- Rochester Institute of Technology
- Texas A&M University
- Fraunhofer
- University of Applied Sciences Kiel
- Kookmin University
- University of Alberta
- University of Applied Sciences Deggendorf
- University of Windsor
- Carleton University
- College de Maisonneuve
- Chalmers University of Technology
- Wright State University
- Universitat Freiburg
- King's College London
- Rowland Institute at Harvard
- Cardiff University
- Universitat Konstanz
- Cornell University

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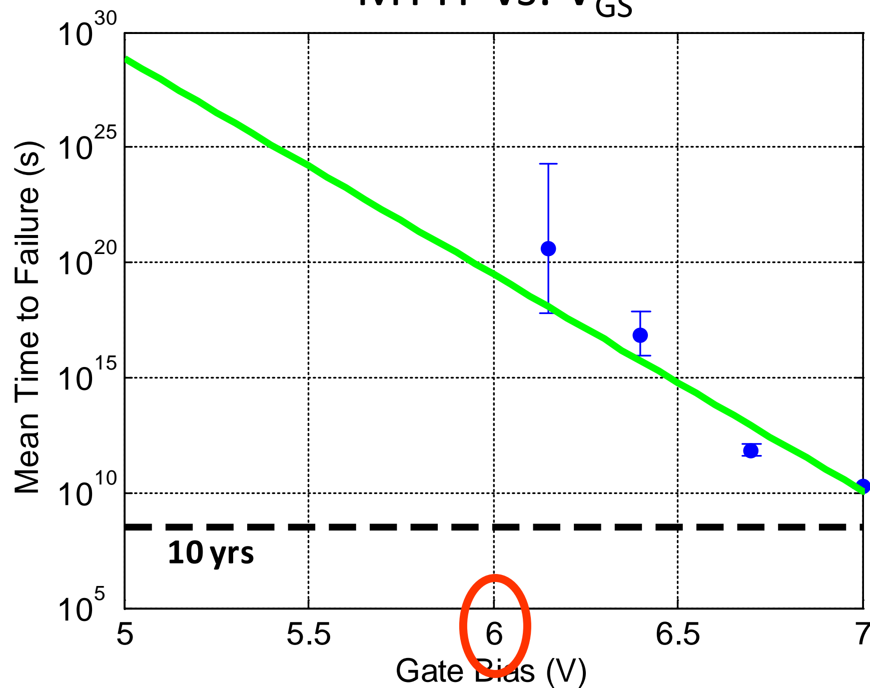
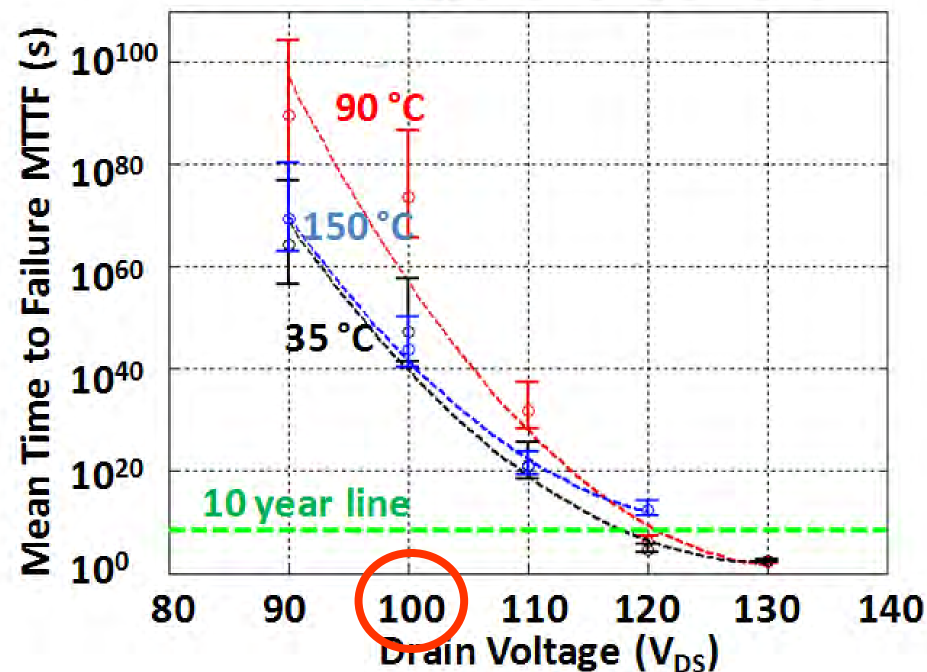
Gate and Drain Stress

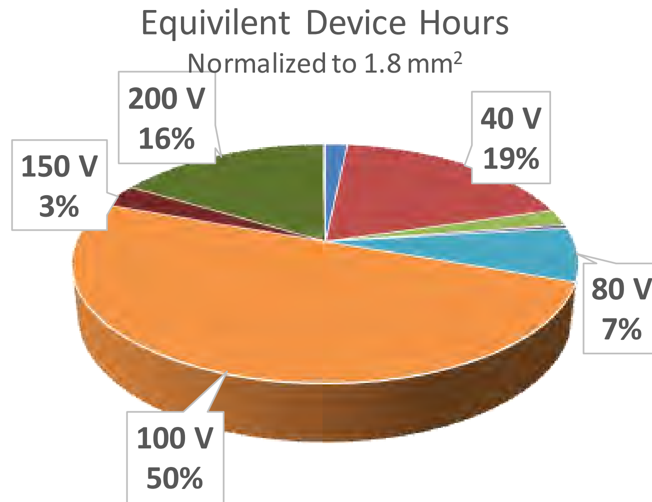




Alex Lidow and Rob Strittmatter, "Enhancement Mode Gallium Nitride Transistor Reliability", IEEE First International Conference On DC Microgrids (ICDCM) 2015

Field Reliability

Data as of Oct, 2015



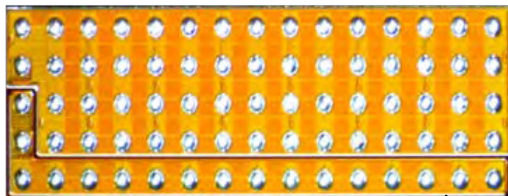
35B equivalent device hours in the field

15B total device hours

- 127 Field Returns (39 Good, 88 Failed)
  - 23 Layout Related
  - 62 Assembly Related
  - 1 Physical Abuse
  - 3 Device degradation (addressed in Gen 4 and screening)
- **3 Device Failures in 15B Hours equals 0.2 FIT**

Moore's Law Revival

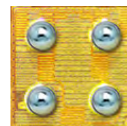
Gen 3 & 4 FETs and ICs
2014
30 V - 450 V
3 GHz



Higher Power
RF FETs and ICs
Broadband to 6 GHz

Higher Scale Integrated Circuits

MOSFET killers



Generation 5
Lower R x A

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Summary

EPC EFFICIENT POWER CONVERSION

- **GaN is rapidly improving**
- **GaN is not a drop in replacement**
- **GaN transistors will replace silicon power MOSFETs with a lower-cost and higher-efficiency solution.**

Thank You For Your Time ! Questions?