The eGaN® FET Journey Continues

Low Voltage GaN Transistors – Applications and Reliability

Alex Lidow
Agenda

• Technology Update
• Reliability Update
• Application Update
• Summary
Power Switch Wish List

- Lower On Resistance
- Less Capacitance
- Less Inductance
- Lower Thermal Impedance
- Smaller
- Lower Cost
On-Resistance Comparison

\[ V_{GS} = 5 \text{ V} \]

For different drain-to-source voltage (V) values:
- **eGaN FETs Gen 2**:
  - Size: 4.1 x 1.63 mm, 6.68 mm²
  - On-Resistance: 2.3x

- **eGaN FETs Gen 4**:
  - Size: 6.05 x 2.3 mm, 13.92 mm²
  - On-Resistance: 2.6x
Hard Switching FOM

FOM_{HS} = (Q_{GD} + Q_{GS2}) \cdot R_{DS(on)} (pC \cdot \Omega)

V_{DS} = 0.5 \cdot V_{DSS}, I_{DS} = 20 \text{ A}

- EPC Gen 4
- Vendor A
- Vendor B
- Vendor C
- Vendor D
- Vendor E

Si MOSFETs 2014

eGaN FETs Gen 2

eGaN FETs Gen 4
Package Inductance

Device Loss Breakdown


Vin = 12 V Vout = 1.2 V
Iout = 20 A fsw = 1 MHz
Thermal Efficiency

Silicon Substrate

Active GaN Device Region

$R_{\theta CA}$

$R_{\theta JC}$

$T_J$

$R_{\theta JB}$

$R_{\theta BA}$
Package Comparisons

The graph shows the thermal resistance ($R_{\theta JB}$) in °C/W as a function of device area (mm²). The data points are color-coded to distinguish between $R_{\theta JB_{-Si}}$ (red) and $R_{\theta JB_{-GaN}}$ (blue) for different device packages.
Package Comparisons

![Graph showing Package Comparisons with thermal resistance (°C/W) on the y-axis and device area (mm²) on the x-axis. The graph compares RθJC_Si and RθJC_GaN.]
DC-DC Performance

Efficiency (%) vs. Output Current (A)

- Blue curve: 40 V/30 V EPC Gen 4
- Red curve: 30 V MOSFET Module
- 30% Loss Reduction
- $f_{sw} = 1 \text{ MHz}$

$V_{IN} = 12 \text{ V} \quad V_{OUT} = 1.2 \text{ V}$
Higher Voltage DC-DC Performance

![Graph showing efficiency vs. output current for 80 V MOSFET and 100 V/80 V EPC Gen 2/4. The graph includes a 60% loss reduction at higher current levels, indicated by a vertical arrow. The graph also shows different switch frequencies (f_sw = 300 kHz and f_sw = 500 kHz) and input and output voltages (V_IN=48 V, V_OUT=12 V).]
Take It Up Another Notch!
GaN Integration

**Generation 2/4**
Discrete HB

*Top Switch (T)* + *Synchronous Rectifier (SR)*

**Generation 4**
Monolithic 4:1 HB

33% die size reduction
Monolithic Half Bridge

EPC2100
30 V 1:4 HB

Gen 4
Discrete Transistors

33 % die size reduction

--- f_{sw} = 2 MHz --- f_{sw} = 4 MHz

V_{IN} = 12 V V_{OUT} = 1.2 V L = 100 nH
Monolithic Half Bridge

EPC2105
80 V 1:4 HB
33 % die size reduction

EPC2001 +
EPC2021

V_{IN}=48 V \ V_{OUT}=1 V \ L=330 \text{nH}

f_{sw}=300 \text{ kHz}
Reliability
# HTRB and HTGB Reliability

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Part Number</th>
<th>Voltage (V)</th>
<th>Die Size (mm x mm)</th>
<th>Test Condition</th>
<th># of Failures</th>
<th>Sample Size (sample x lot)</th>
<th>Duration (Hrs)</th>
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</thead>
<tbody>
<tr>
<td>HTRB</td>
<td>EPC2001C</td>
<td>100</td>
<td>L (4.11 x 1.63)</td>
<td>$T=150^\circ C, V_{DS}=80$ V</td>
<td>0</td>
<td>77 x 2</td>
<td>2000</td>
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<tr>
<td>HTRB</td>
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<td>100</td>
<td>M (2.11 x 1.63)</td>
<td>$T=150^\circ C, V_{DS}=80$ V</td>
<td>0</td>
<td>77 x 3</td>
<td>2000</td>
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<tr>
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<td>40</td>
<td>M (1.70 x 1.09)</td>
<td>$T=150^\circ C, V_{DS}=32$ V</td>
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## Environmental Reliability

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<th>Part Number</th>
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<th>Die Size (mm x mm)</th>
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<th># of Failure</th>
<th>Sample Size (sample x lot)</th>
<th>Duration</th>
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<tbody>
<tr>
<td><strong>H3TRB (JEDEC Standard JESD22A101)</strong></td>
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<td>H3TRB</td>
<td>EPC2001C</td>
<td>100</td>
<td>L (4.11 x 1.63)</td>
<td>T=85°C, RH=85%, V&lt;sub&gt;DS&lt;/sub&gt;=80 V</td>
<td>0</td>
<td>25 x 1</td>
<td>1000 Hrs</td>
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<tr>
<td>H3TRB</td>
<td>EPC2016C</td>
<td>100</td>
<td>M (2.11 x 1.63)</td>
<td>T=85°C, RH=85%, V&lt;sub&gt;DS&lt;/sub&gt;=80 V</td>
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<td>H3TRB</td>
<td>EPC2010</td>
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<td>L (3.55 x 1.63)</td>
<td>T=85°C, RH=85%, V&lt;sub&gt;DS&lt;/sub&gt;=100 V</td>
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<td>T=85°C, RH=85%, V&lt;sub&gt;DS&lt;/sub&gt;=100 V</td>
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<td>1000 Hrs</td>
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<td><strong>HTS</strong></td>
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<tr>
<td>HTS</td>
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<td>100</td>
<td>L (4.11 x 1.63)</td>
<td>T=150°C, Air</td>
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<td>HTS</td>
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<td><strong>TC (JEDEC Standard JESD22A104)</strong></td>
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<td>TC</td>
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<td>1000 Cys</td>
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<td>TC</td>
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<td>L (3.55 x 1.63)</td>
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<td>0</td>
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<td>1000 Cys</td>
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<td><strong>MSL1 (IPC/JEDEC joint Standard J-STD-020)</strong></td>
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<td>25 x 1</td>
<td>168 Hrs</td>
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<td>MSL1</td>
<td>EPC8007</td>
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<td>S (2.05 x 0.85)</td>
<td>T=85°C, RH=85%, 3 reflow</td>
<td>0</td>
<td>25 x 1</td>
<td>168 Hrs</td>
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<td><strong>AC (JEDEC Standard JESD22A102)</strong></td>
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<tr>
<td>AC</td>
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<td>L (4.11 x 1.63)</td>
<td>T=121°C, RH=100%</td>
<td>0</td>
<td>25 x 1</td>
<td>96 Hrs</td>
</tr>
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<td>AC</td>
<td>EPC2016C</td>
<td>100</td>
<td>M (2.11 x 1.63)</td>
<td>T=121°C, RH=100%</td>
<td>0</td>
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</tr>
</tbody>
</table>
Failure under Drain Stress

Time to Failure vs $V_{DS}$ (150°C)

- 0.01%
- 1%
- 0.0001%

Age of the Universe

EPC2016C

20 yrs
Gate Stress

**MTTF vs. V\textsubscript{GS}**

- Mean Time to Failure (s)
- Gate Bias (V)

**FIT Rate vs. V\textsubscript{GS}**

- FIT Rate (#/10^9 hours)
- Gate Bias (V)

10 yrs

EPC2016C

150 °C
eGaN FET Applications

- Wireless Power
- LiDAR
- Envelope Tracking
- Network and Server Power Supplies
- Satellite Systems
- High Resolution Class-D Audio
- Energy Efficient Lighting
- High Resolution MRI Imaging
- AC Adapters
- Robotics
Wireless Power

The global wireless charging market is estimated to grow to $10B by 2018, a CAGR of 42.6%.
LiDAR uses lasers pulsed by eGaN FETs to rapidly create a 3D image of the surrounding area.

LiDAR system used for 3D orientation in virtual reality systems

eGaN FETs in a LiDAR system on an autonomous prototype
Envelope Tracking

- **Peak power**
- **Average power**

**3G (W-CDMA)**
- 3.5 dB PAPR (~2:1)

**3.5G (HSUPA)**
- 6.5 dB PAPR (~5:1)

**4G (LTE / OFDM)**
- 8.5 dB PAPR (~7:1)

Reference: Nujira.com website
DC-DC 1/8th Brick

- Fully regulated
- Isolated
- 52 V nominal input (4:1 transformer)
- DOSA-compliant footprint
- 500 W output at 12V
500 W 1/8 Brick Efficiency

2m/s airflow

Efficiency vs. i_{out} [A]

- Vin = 60
- Vin = 56
- Vin = 52
- Vin = 48

82.8°C
Pri. FET

91.0°C
Sec. FET

100.1°C
Transformer core
### MOSFET vs. eGaN Costs*

<table>
<thead>
<tr>
<th></th>
<th>2014</th>
<th>2016</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting Material</td>
<td>lower</td>
<td>lower</td>
</tr>
<tr>
<td>Epi Growth</td>
<td>~higher</td>
<td>~same?</td>
</tr>
<tr>
<td>Wafer Fab</td>
<td>lower</td>
<td>lower</td>
</tr>
<tr>
<td>Test</td>
<td>same</td>
<td>same</td>
</tr>
<tr>
<td>Assembly</td>
<td>lower</td>
<td>lower</td>
</tr>
<tr>
<td><strong>OVERALL</strong></td>
<td>~higher</td>
<td>lower!</td>
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</tbody>
</table>

* Product with the same on resistance and voltage rating
## MOSFET vs. eGaN Costs*

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<th>Process</th>
<th>2014</th>
<th>2016</th>
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<tr>
<td>Starting Material</td>
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<td><strong>OVERALL</strong></td>
<td><strong>lower!</strong></td>
<td><strong>lower!</strong></td>
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</table>

* Product with the same on resistance and voltage rating

Active die <3 mm²
Moore’s Law Revival

Generation 2
2010-2013
40 V - 200 V

Generation 3
Higher Frequency
Launched
September 2013

Generation 4
2 X Performance Improvement
Launched
June 2014
Half Bridge ICs
Launched
September 2014

Generation 5
Soon!

High Voltage
Launched
September 2014
Summary

• eGaN technology is moving quickly. The latest generation of products more than doubles DC-DC converter power density.
• eGaN technology is proving to be very thermally efficient and reliable.
• eGaN technology is making serious inroads into silicon’s territory.
Where is GaN going...