Design and Evaluation of a 10 MHz Gallium Nitride Based 42 V DC-DC Converter

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Agenda

- Requirements for HF hard switching
- EPC8000 Series Parts
- Experimental Results
- Limiting Factors
- Summary
HF Hard Switching Requirements

- Reduce active area for lower power operation
- Minimize Hard Switching Figure of Merit
- Complete dv/dt immunity
- Separate gate and power loops
- Minimize power loop inductance
- Minimize gate loop inductance
Device Size

EPC8004 eGaN FET

EPC2014 eGaN FET

$V_{GS} \rightarrow$ Gate to Source Voltage (V)

$Q_G \rightarrow$ Gate Charge (nC)
Hard Switching FOM

<table>
<thead>
<tr>
<th>(Q_{GD}+Q_{GS2}) \cdot R_{D\text{S(on)}} (pC*Ω)</th>
<th>230mΩ</th>
<th>24mΩ</th>
<th>90mΩ</th>
<th>200mΩ</th>
<th>71mΩ</th>
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</thead>
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<tr>
<td>EPC8005</td>
<td>50</td>
<td>45</td>
<td>40</td>
<td>25</td>
<td>20</td>
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<td>CSD17381F4</td>
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<td>CSD17483F4</td>
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<td>Si8808DB</td>
<td>25</td>
<td>20</td>
<td>10</td>
<td>5</td>
<td>0</td>
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</tbody>
</table>

65 V eGaN FET

100 V eGaN FET

30 V BGA MOSFETS
dv/dt Immunity

$Q_{GS1} > Q_{GD}$

$\text{Id}=1\text{A}$
$\text{Vd}=20\text{V}$

$20\text{V}$
$40\text{V}$

EPC8004 eGaN FET
Low Parasitic Layout

Top Layer

- Vias to next layer
- To BUS caps
- Supply
- Switch node
- Gate Current orthogonal to drain current
- Vias to next layer
- Ground

Bottom Gate

- Top Gate
Low Parasitic Layout

First InnerLayer

To gate drive
Optimum gate loop return

To gate drive
Optimum gate loop return

Optimum power loop return

Drain
Source
Sub

Gate
Return

Gate
Return

Gate
Return

Source

S

S

Sub
ET Prototype Board

- EPC90 30.1V DEVELOPMENT BOARD
- eGaN® FET © EPC 2013
- EPC8010
- LM5113
- Bus caps
- EPC8010
- LM5113
- SO-8 footprint
42V<sub>IN</sub> at 1A<sub>OUT</sub>

No measurable overshoot

- dv/dt interval
- 75V/ns slew rate

- di/dt interval
- Rise time ~1.0 ns
- Total switching time ~1.2 ns

2 ns/div and 10 V/div, 1 GHz 100:1 1pF TM probe
42V_{IN}, 20V_{OUT}, 10MHz

EPC - The Leader in eGaN® FETs

www.epc-co.com
No-load Switching

10 MHz switching, no load, large dead-time

Expected commutation based on eGaN FET $C_{OSS}$

Initially slow rising edge

Actual voltage commutation slopes are different, even though currents are the same

Inductor current
Parasitic Losses

Bootstrap diode
Reverse recovery charge
V_{DD}
IC capacitance
Level Shift
Switch-node rising edge

LM5113 half-bridge driver
Loss Breakdown

10 MHz switching, no load, large dead-time

10V/div, 100mA/div, 10ns/div

Inductor current
Switch-node voltage
Bootstrap Q_{RR}
Actual commutation based on total C_{OSS} – including IC capacitance
42\text{V}_{\text{IN}}, 20\text{V}_{\text{OUT}}, 10\text{MHz}

Efficiency vs. Output power (W)

- Conduction
- Switching
- \text{C}_{\text{OSS}}
- Gate driver and Magnetics
- Switching
- \text{C}_{\text{OSS}} \text{ Driver}
- \text{Q}_{\text{RR}} \text{ Bootstrap diode}

Power Loss (W)

- 0
- 1
- 2
- 3
- 4
- 5
Calculated efficiency improvement

Reduction in $C_{\text{Driver}}$, $Q_{\text{BootRR}}$ and driver losses
Summary

• New devices enable higher switching frequencies
• Switching 42V, 40W at 10MHz at 89% possible
• Driver parasitics limit performance
  • Doubles light load losses
• Further improvements in efficiency possible
The end of the road for silicon.....

is the beginning of the eGaN FET journey!