GaN設計の性能を最大化するための簡単な設計のヒント

安田　昭一

議題

- Gate Drive
- Layout
- PCB design
- Thermal management
- EMI

ゲート駆動に関する考慮事項

It's Simple!

- Regulation of gate drive supply voltage
  - Ideal range 5 V – 5.5 V, maximum 6 V
- Gate power-loop inductance minimization
- Noise immunity

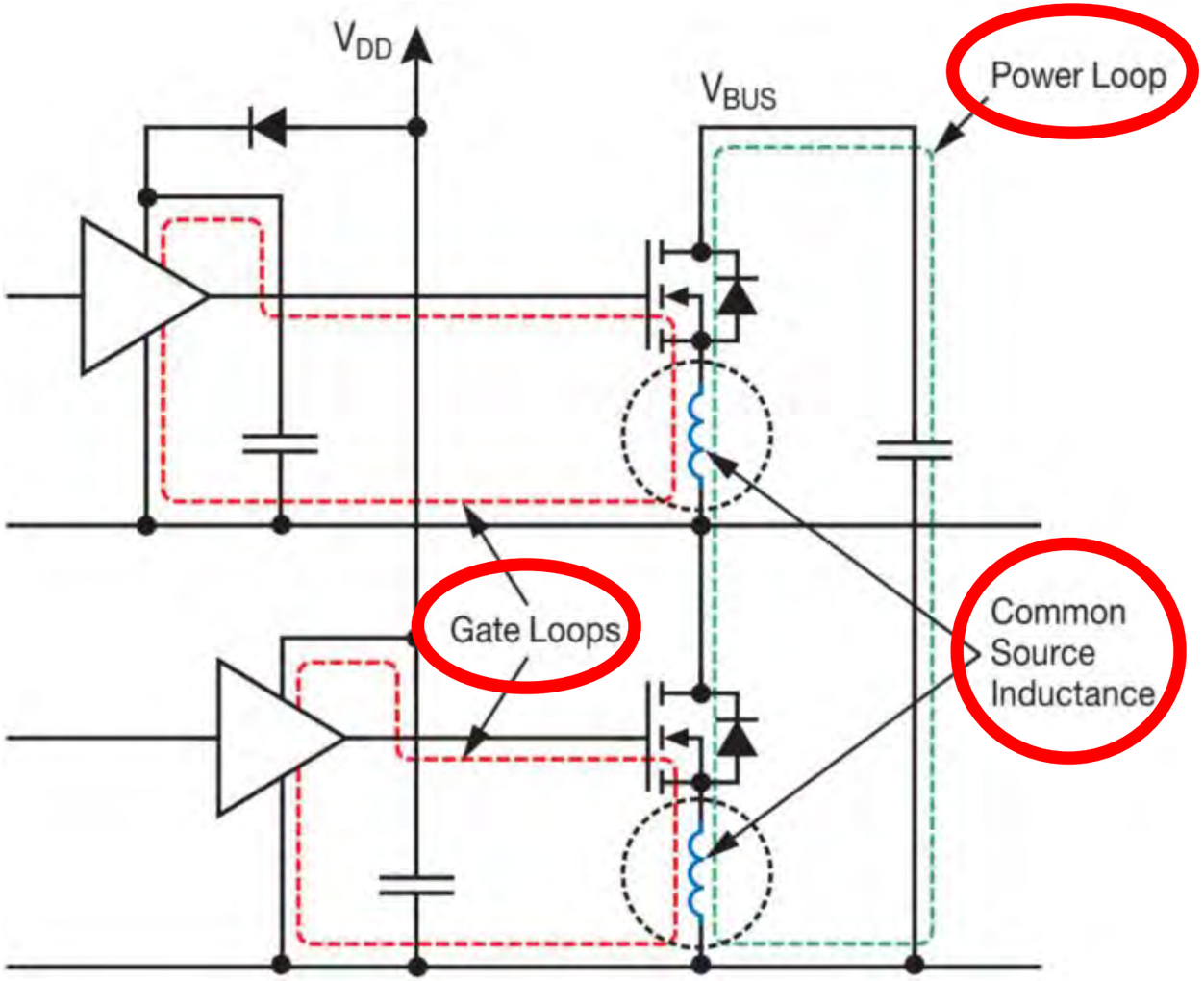
eGaN® FET向けのゲート・ドライバー

- Low-side gate drivers
- Half-bridge gate drivers
- Radiation resistant gate drivers
- Controllers for synchronous rectifiers
- Controllers for buck converters

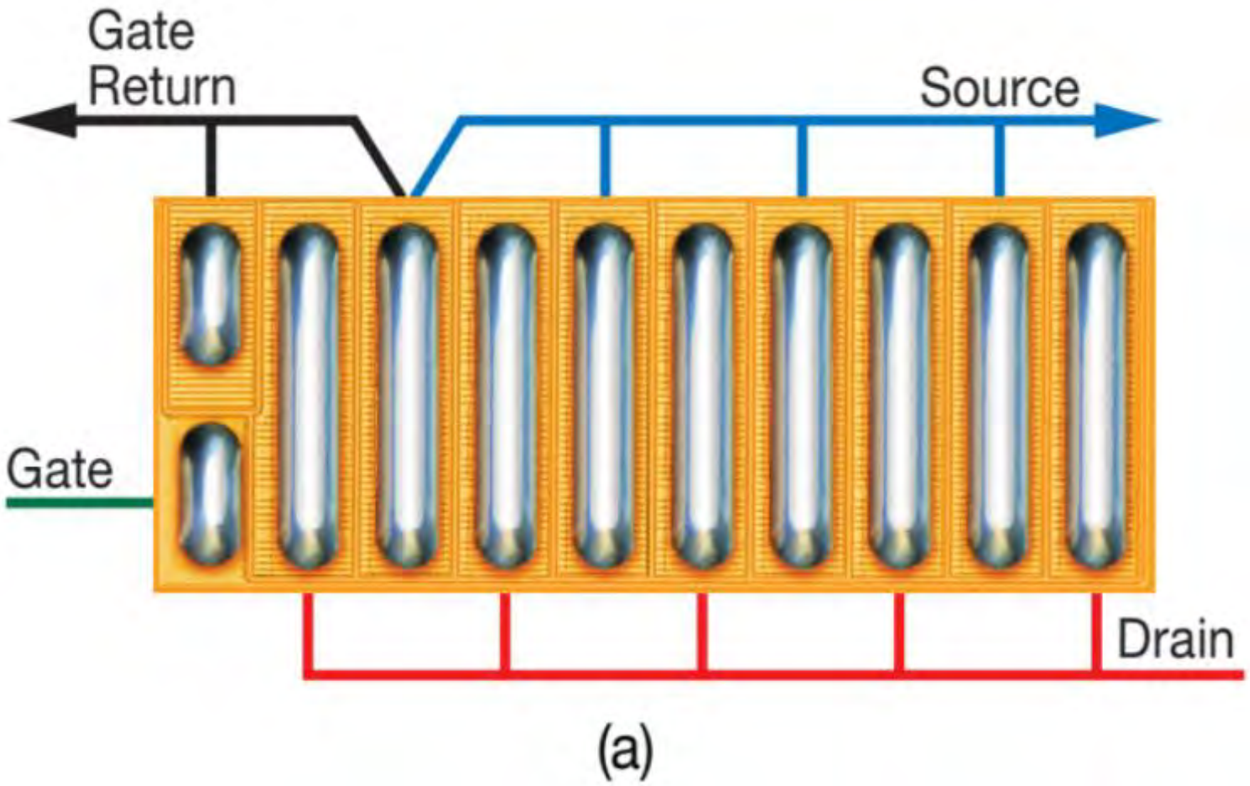
GaN設計の基本：レイアウト

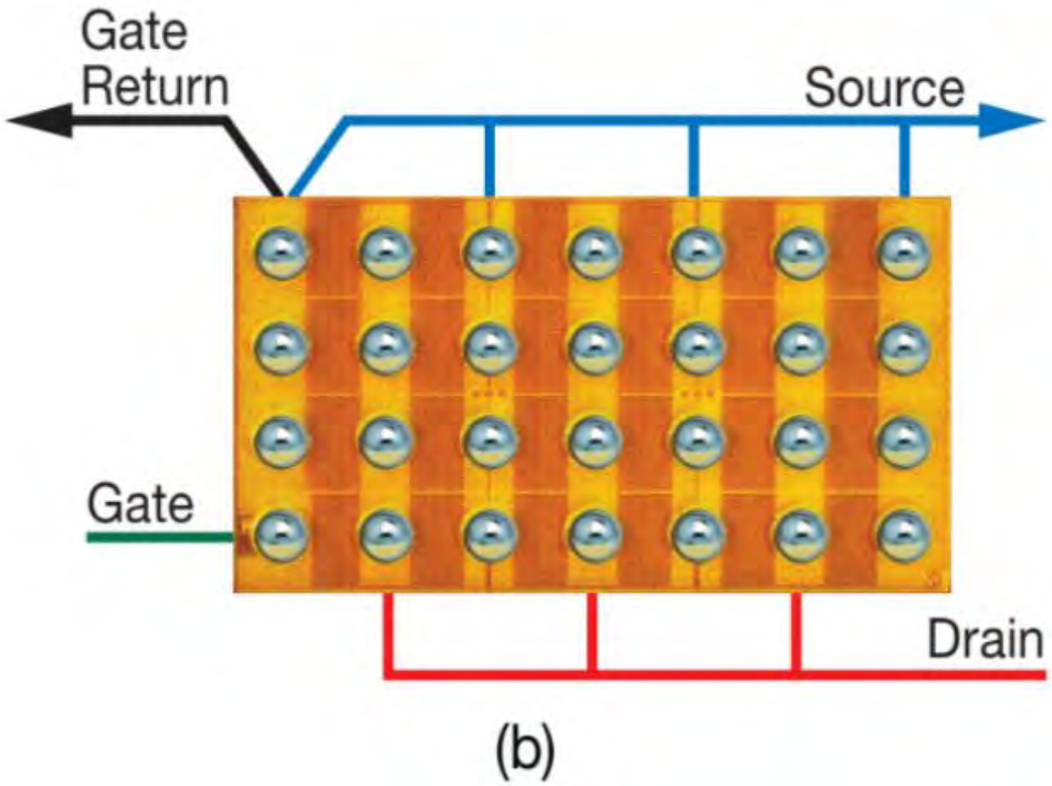
- Common source inductance (CSI)
- High-frequency power loop inductance
- Gate drive loop inductance
- Optimal layout

寄生インダクタンス

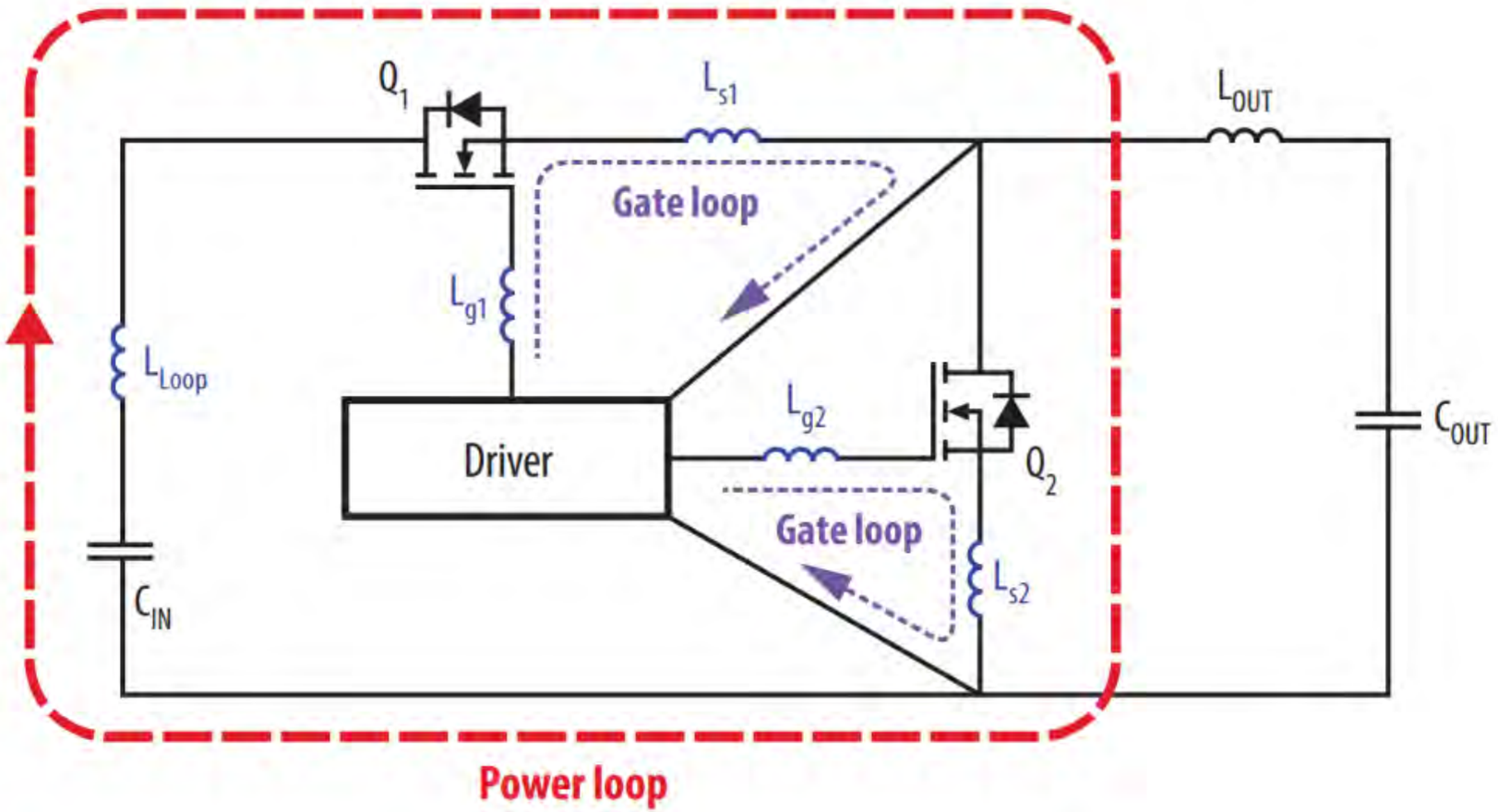


寄生インダクタンスの最小化

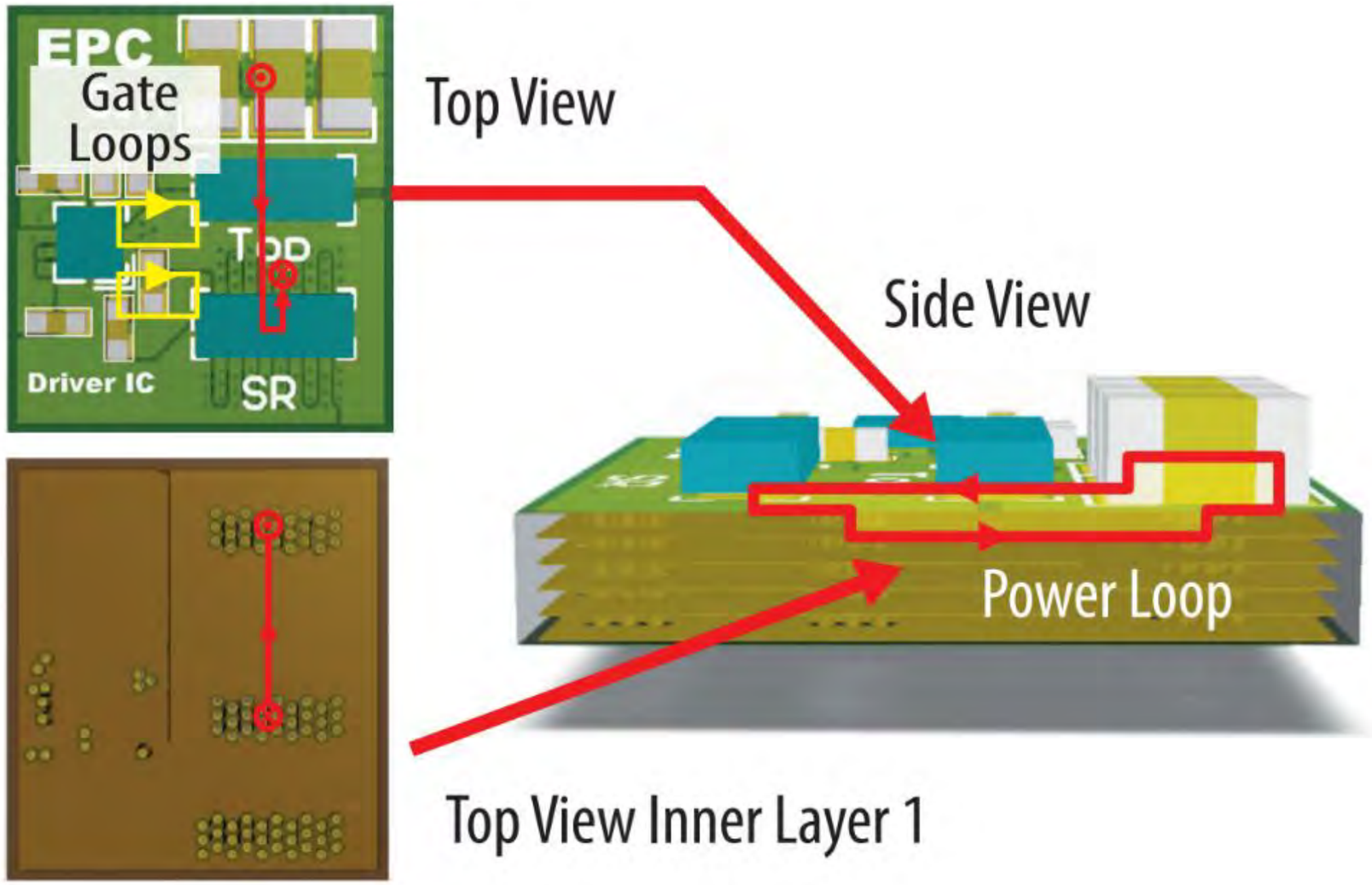




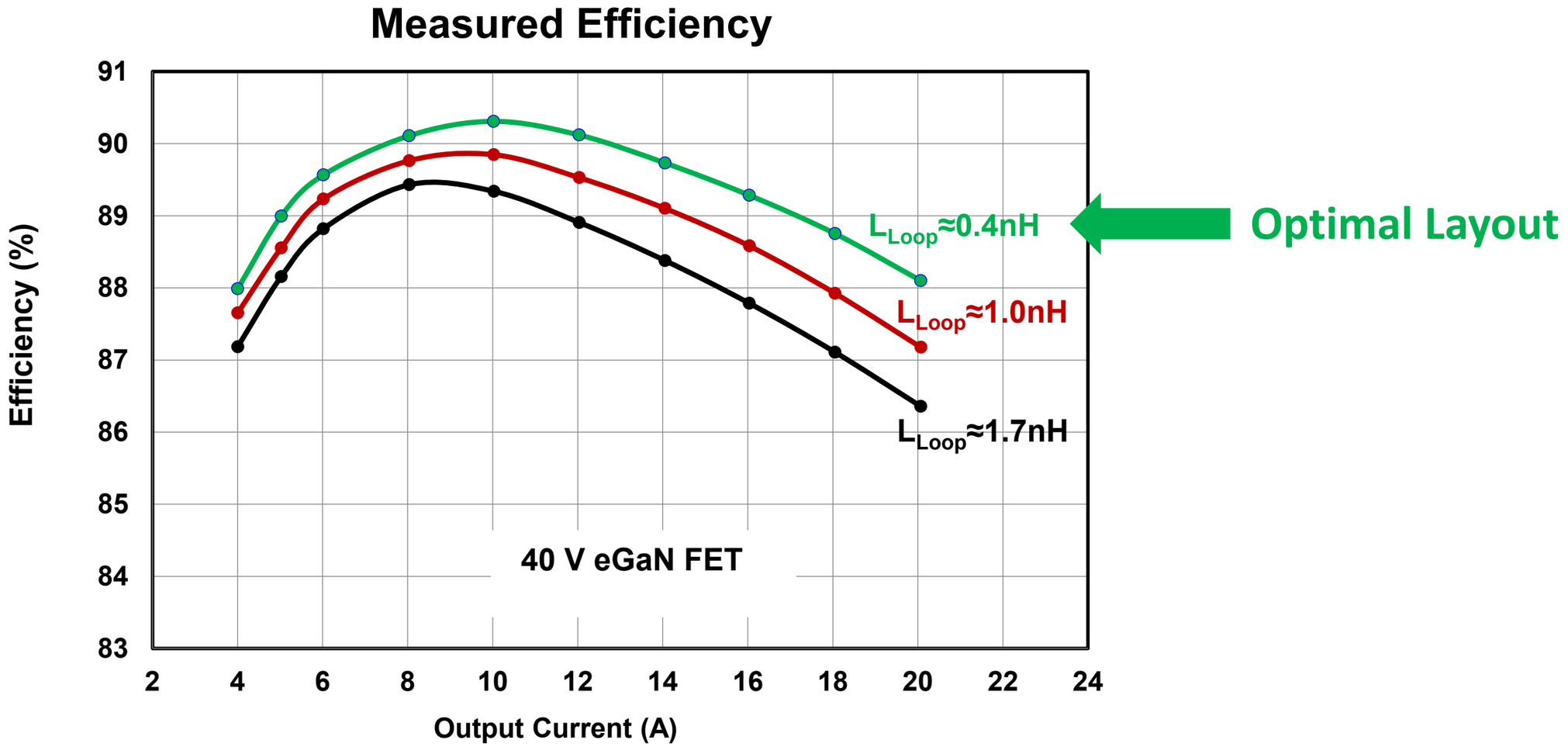
ゲート駆動のループ・インダクタンス



最適レイアウト


EPC
Gate
Loops
Driver IC
SR
Top View
Side View
Power Loop
Top View Inner Layer 1

最適レイアウト：効率



V_{IN}=12 V, V_{OUT}=1.2 V, f_{sw}=1 MHz, L=300 nH

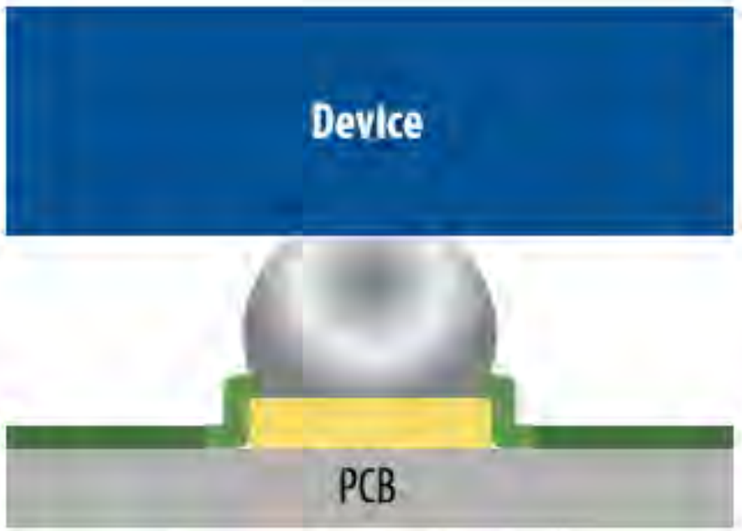
プリント回路基板設計の考慮事項

- Copper pad design
- Silkscreen design
- Vias

銅パッドの設計

Asymmetrical solder ball
(Sensitive to registration)
Non-solder mask defined

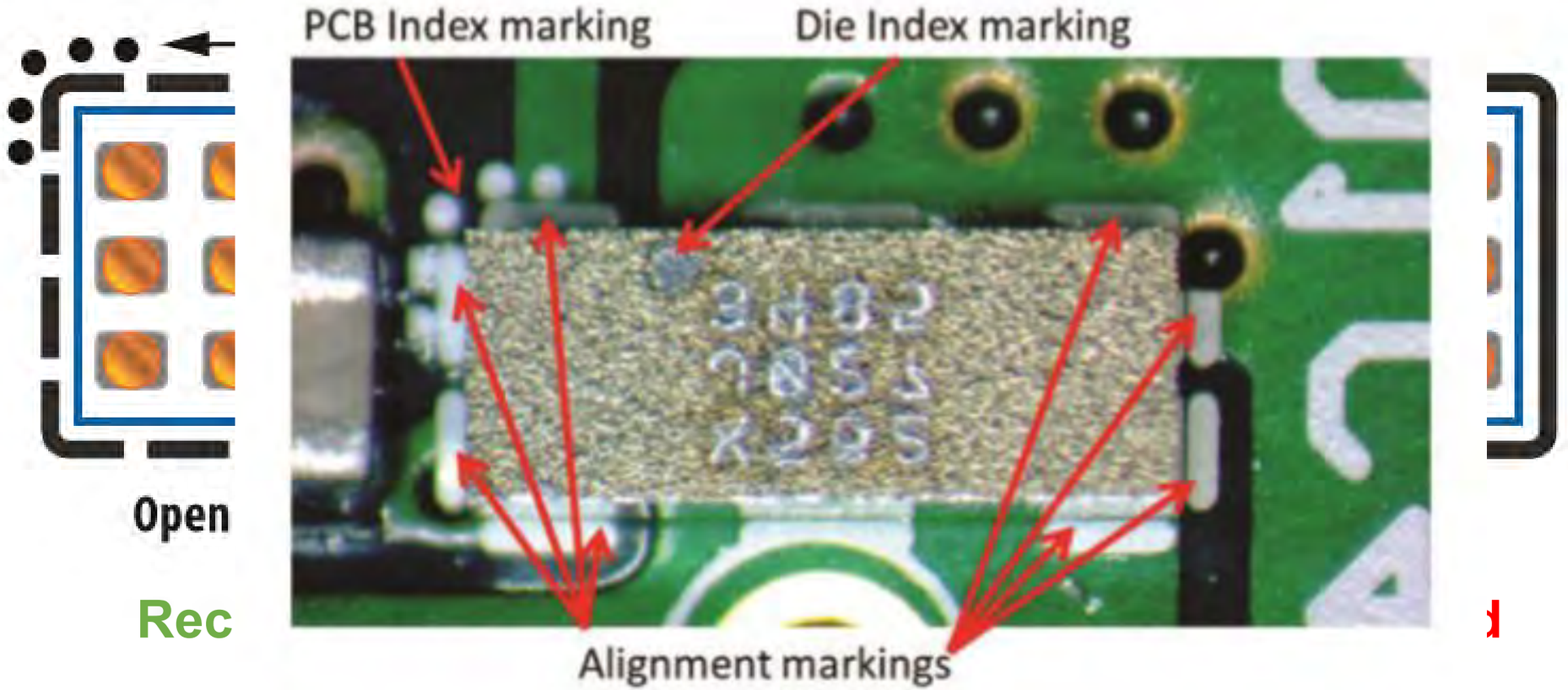
Not Recommended



Symmetrical solder ball
(Regardless of registration)
Solder mask defined

Recommended

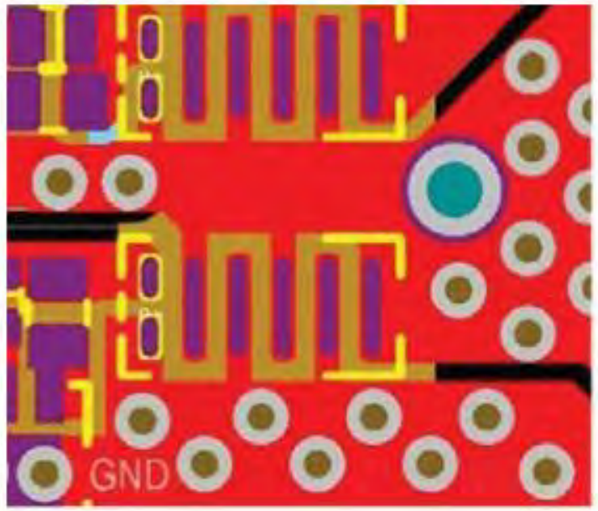
シルクスクリーンの設計

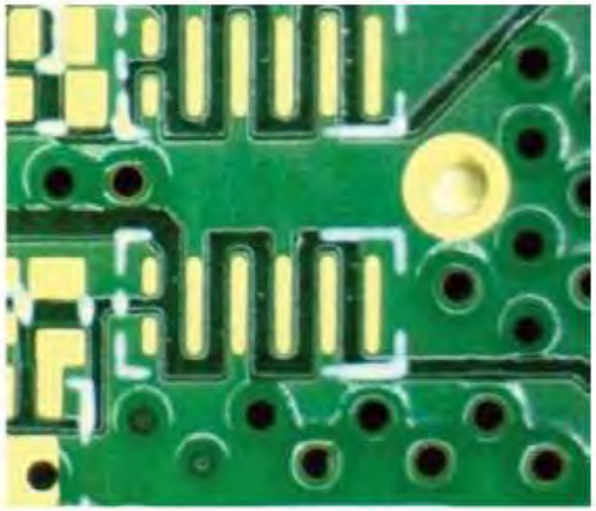


ビア

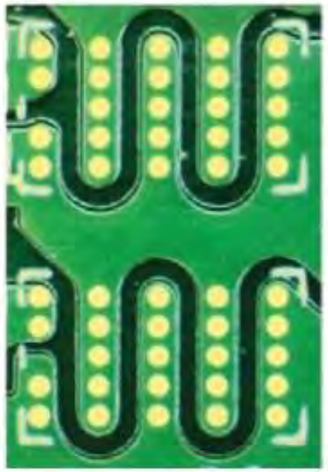
PCB Layout

PCB Photo



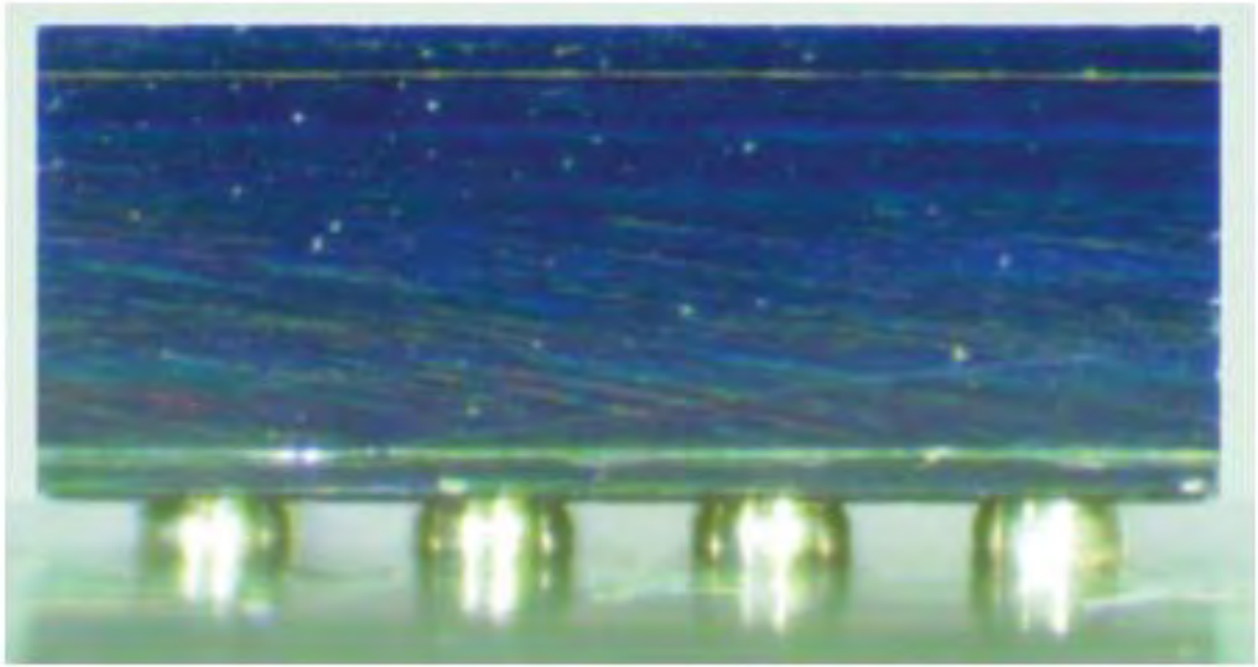


Vias next to pad design



Vias in pad design – vias are filled

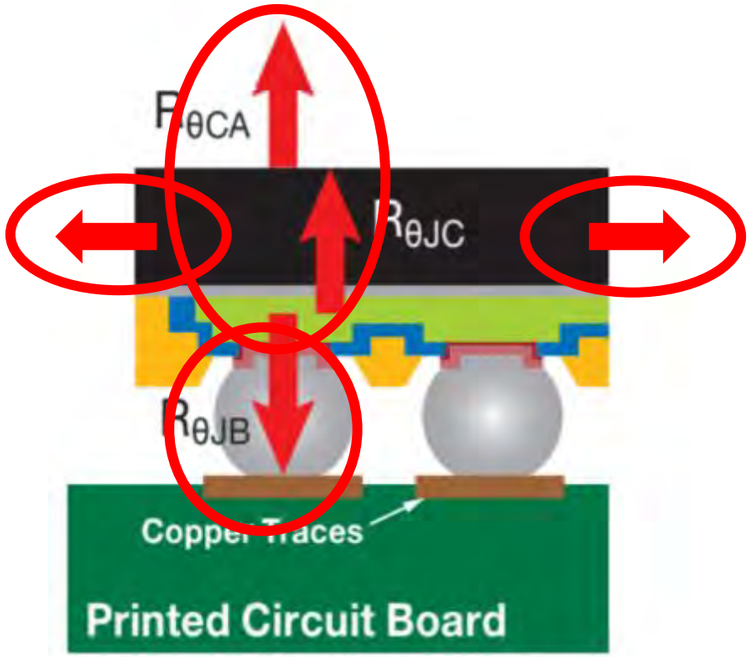
高い信頼性と高い歩留り



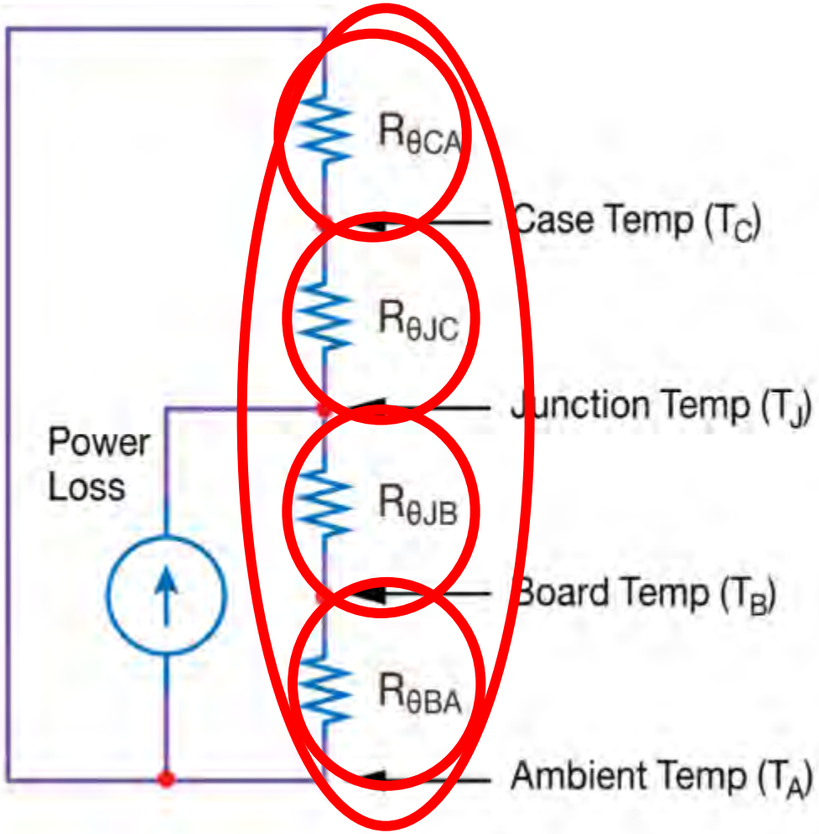
熱管理

- GaN thermal models
- Heatsinking techniques
- Simple thermal solution
- Performance

GaNの熱モデル

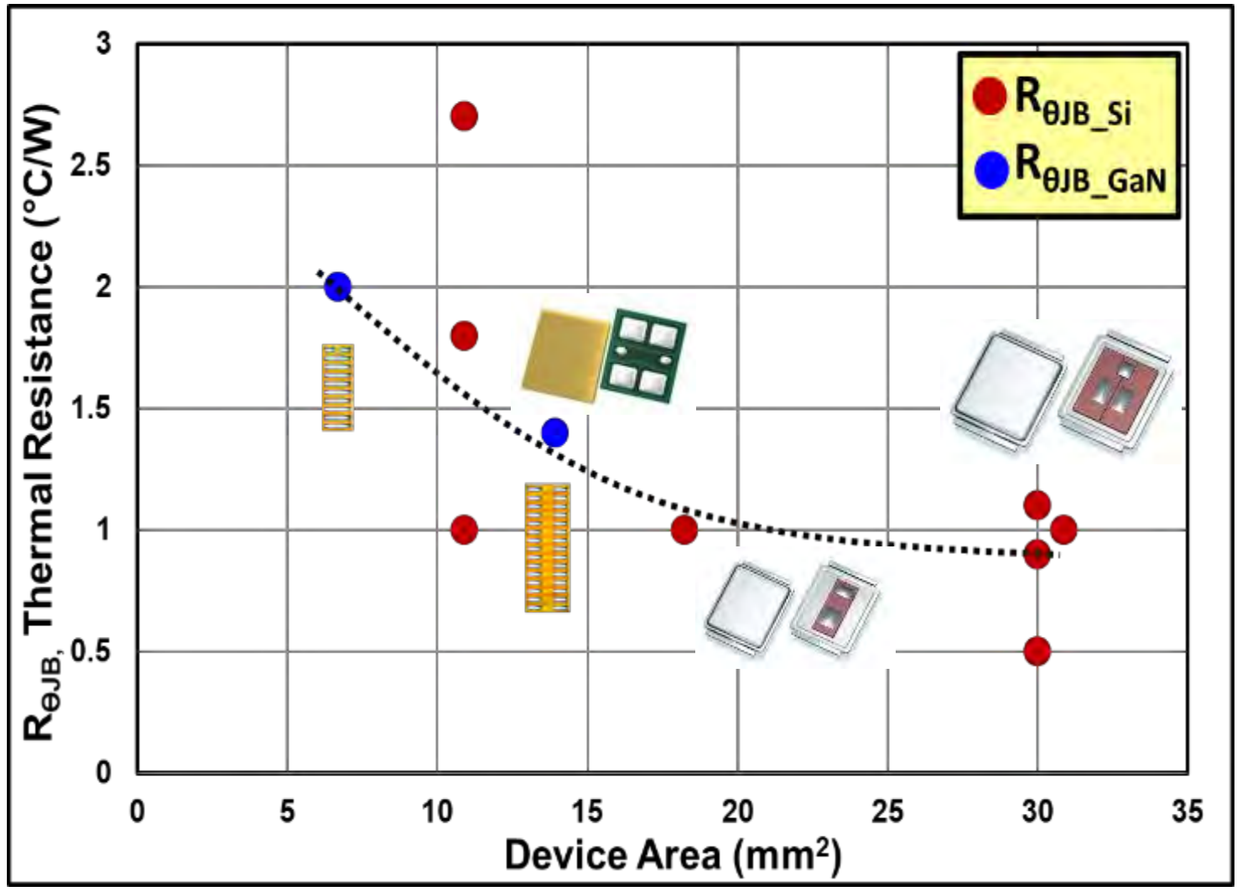


$R_{\Theta JA}$

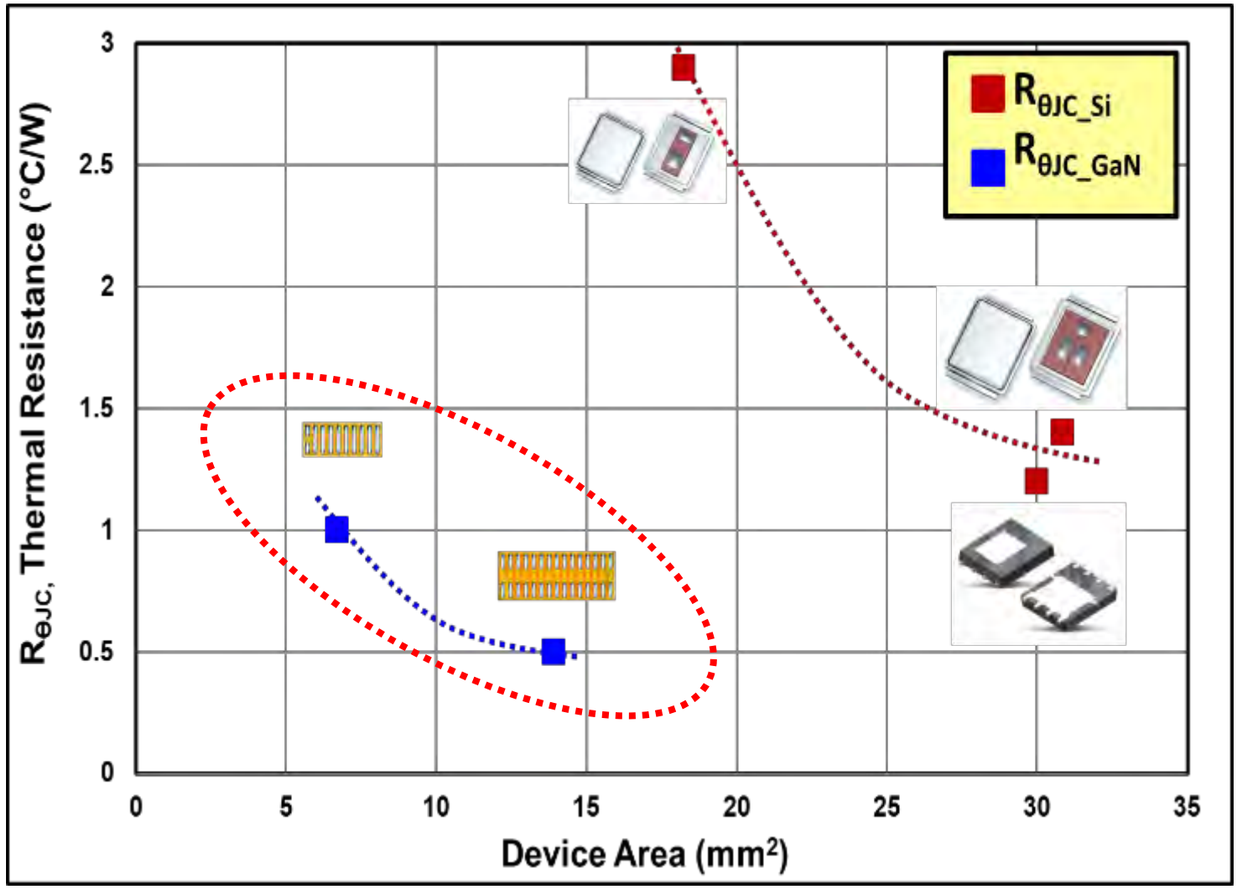


eGaN FETの両面冷却

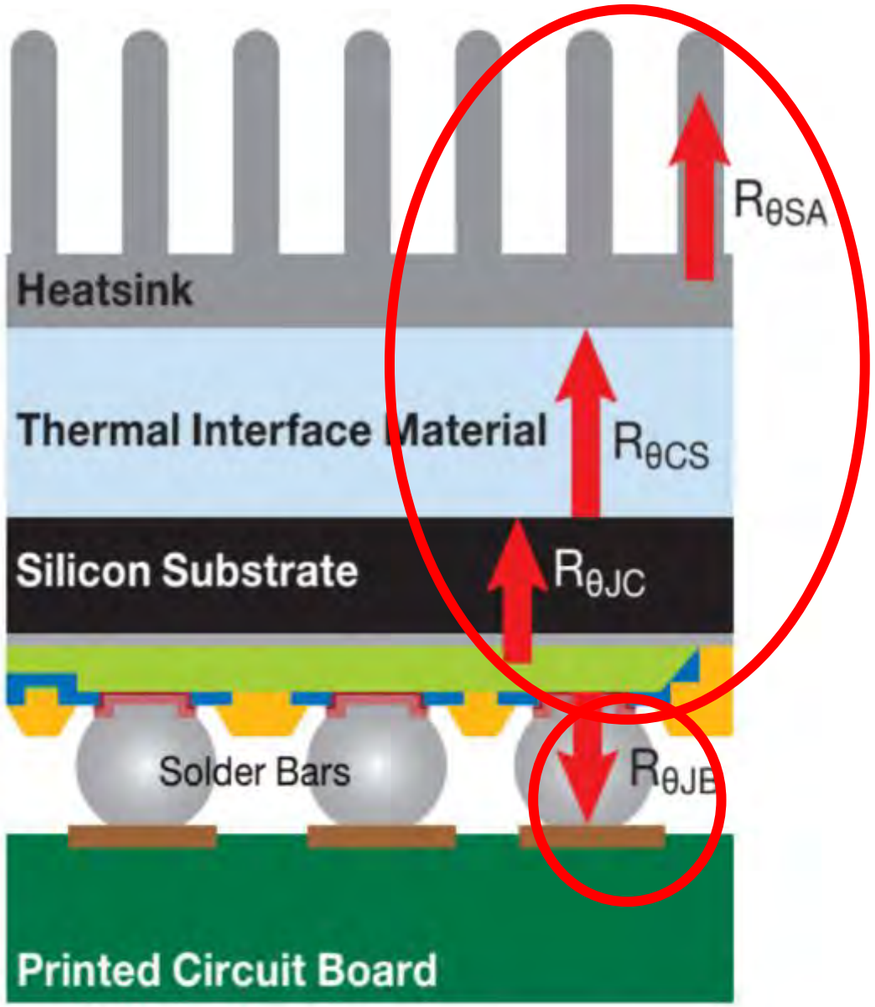
Heat transfer to PCB $R_{\Theta JB}$oard

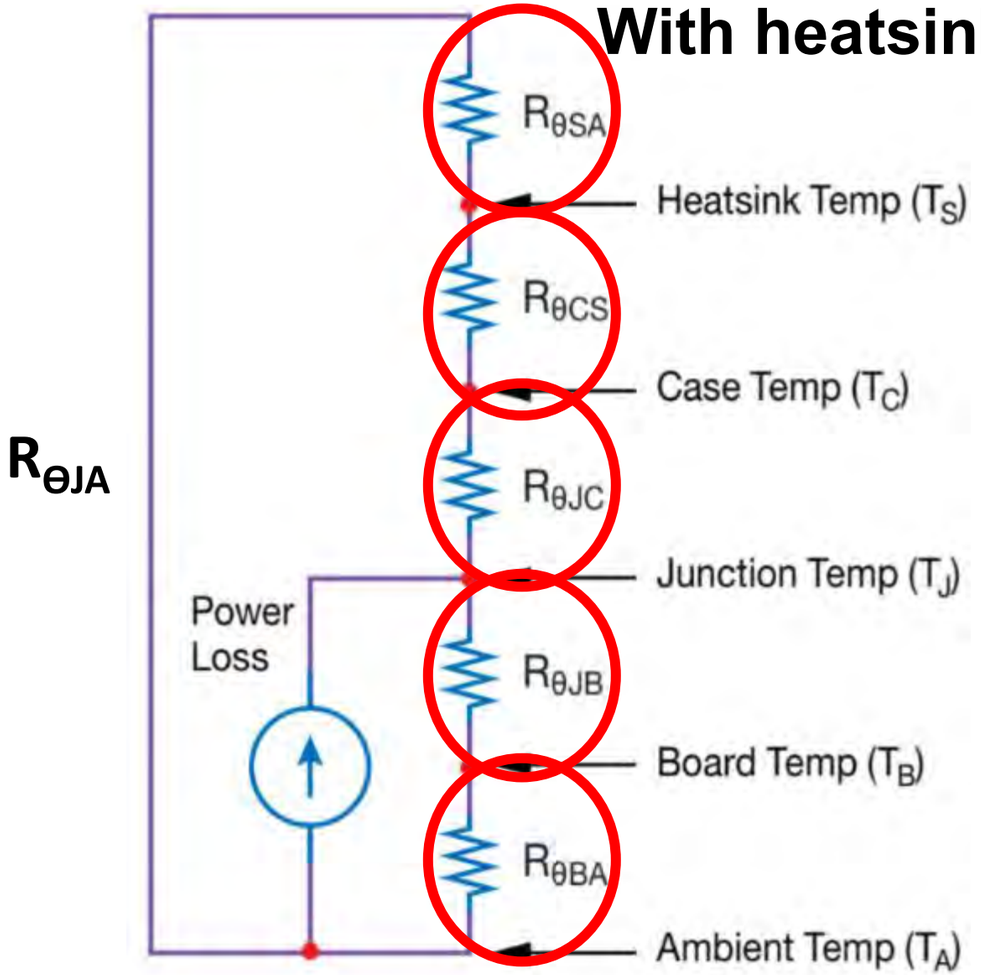


Heat transfer to top Si substrate $R_{\Theta JC}$ase

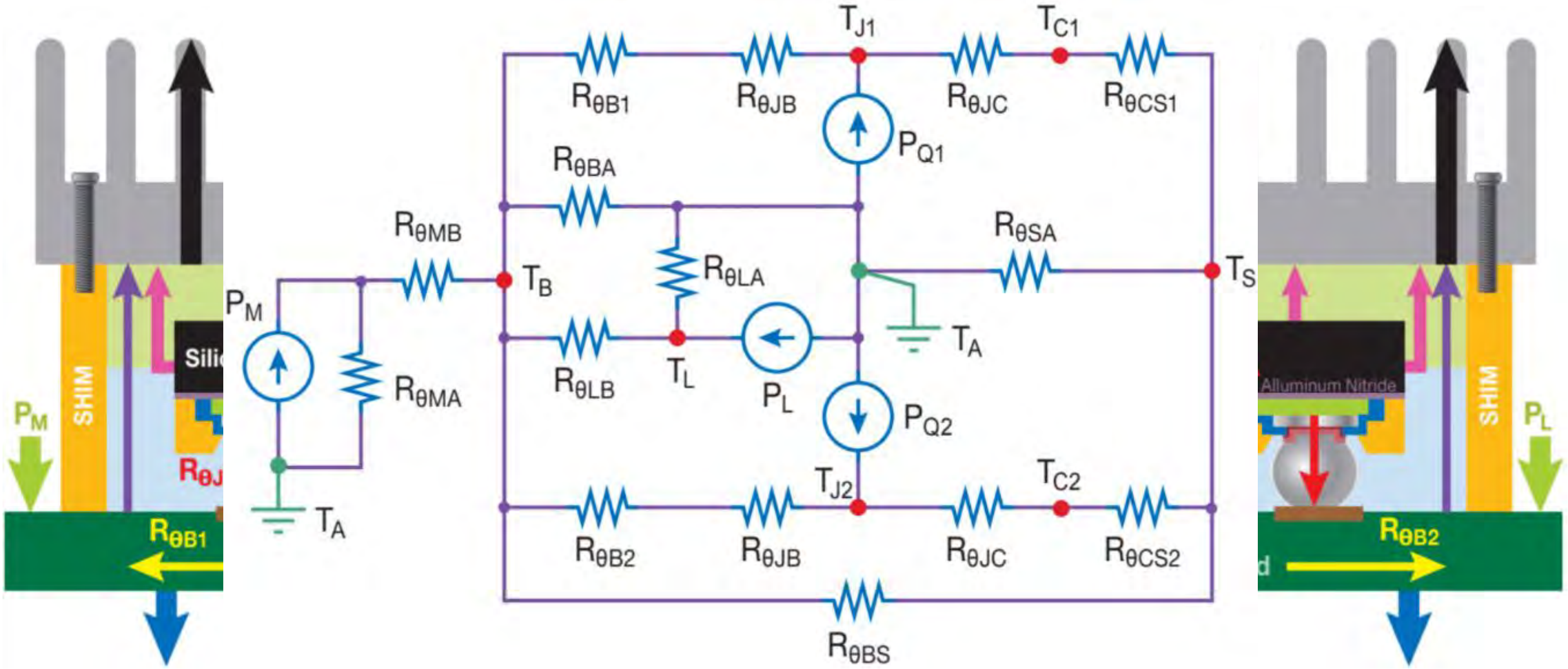


ヒートシンク装着時のGaNの熱モデル

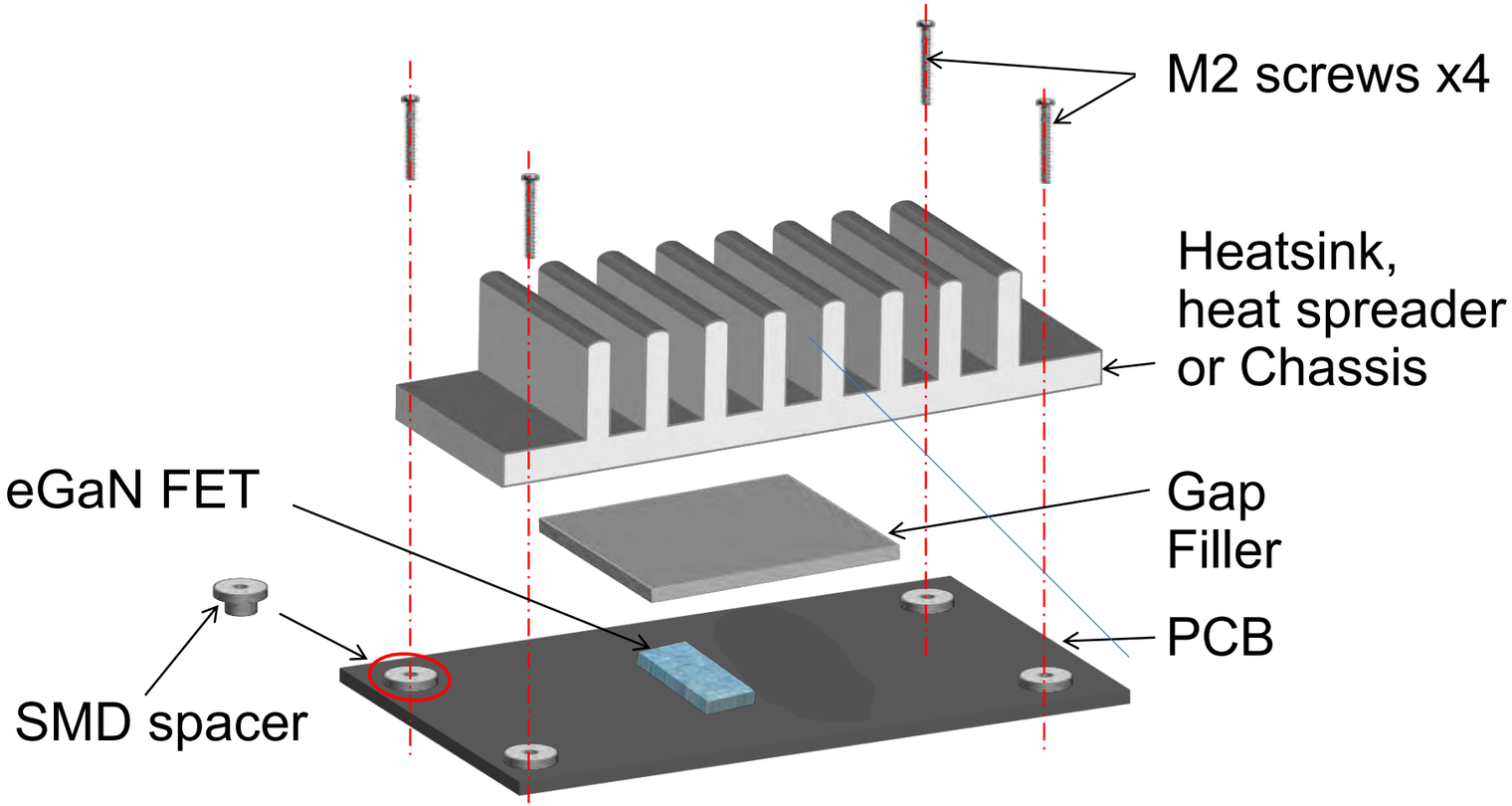




パワー段の熱モデル

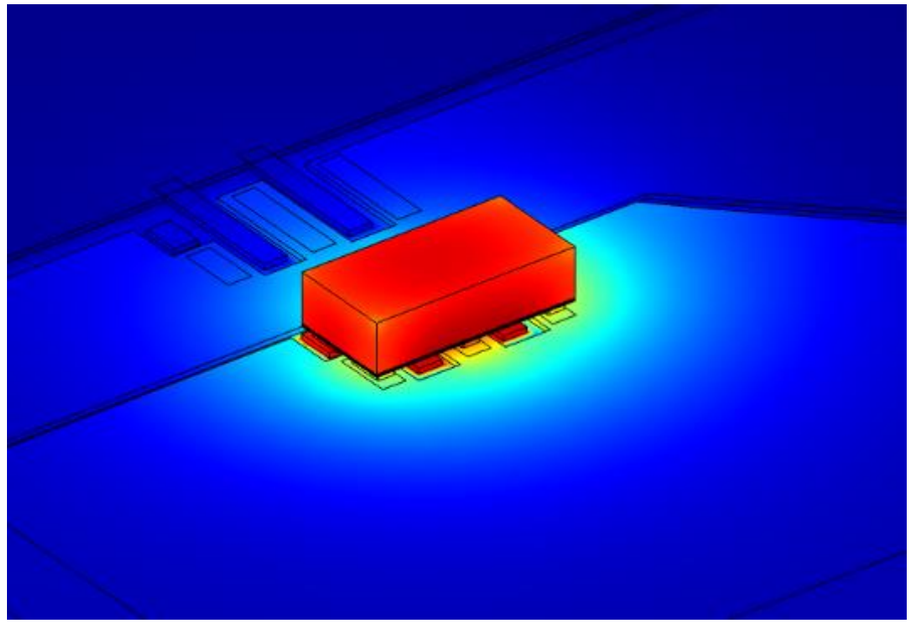

T_{J1}
T_{C1}
$R_{\theta B1}$
$R_{\theta JB}$
$R_{\theta JC}$
$R_{\theta CS1}$
P_{Q1}
$R_{\theta BA}$
$R_{\theta MB}$
$R_{\theta SA}$
$R_{\theta LA}$
T_B
T_S
P_M
T_A
$R_{\theta LB}$
T_L
P_L
$R_{\theta MA}$
P_{Q2}
T_{J2}
T_{C2}
$R_{\theta B2}$
$R_{\theta JB}$
$R_{\theta JC}$
$R_{\theta CS2}$
$R_{\theta BS}$
SHIM
Aluminum Nitride
$R_{\theta B1}$
$R_{\theta B2}$

熱システムの例



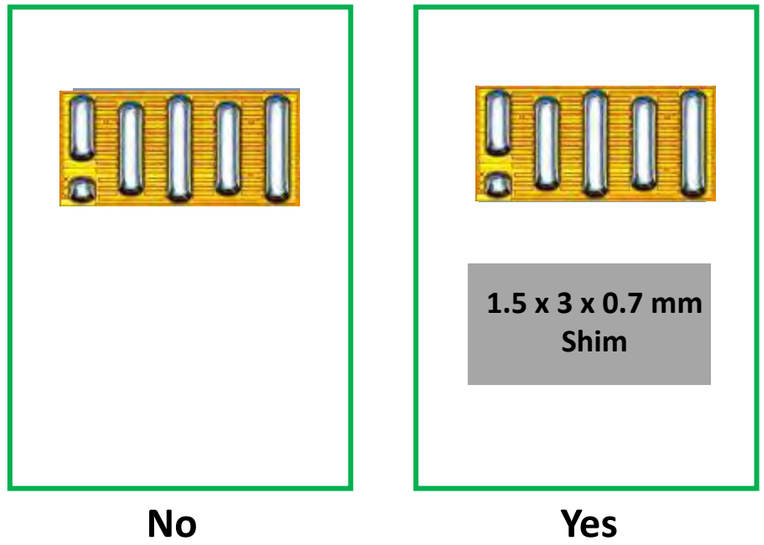
- Gap Filler is Bergquist 3500 S35 – 3.6 W/mK
- Gap filler thickness – 0.1 mm to 0.3 mm
- Copper – 2 oz

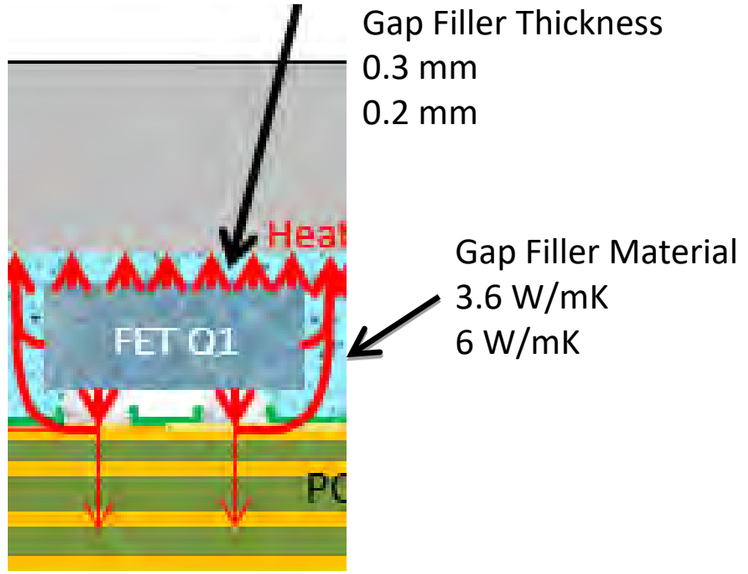
基準の例：4 mm^2



- 3.6 W/m K gap filler, 0.3 mm spacing to heat spreader
- 137.8 °C average T_J with heat spreader at 100 °C

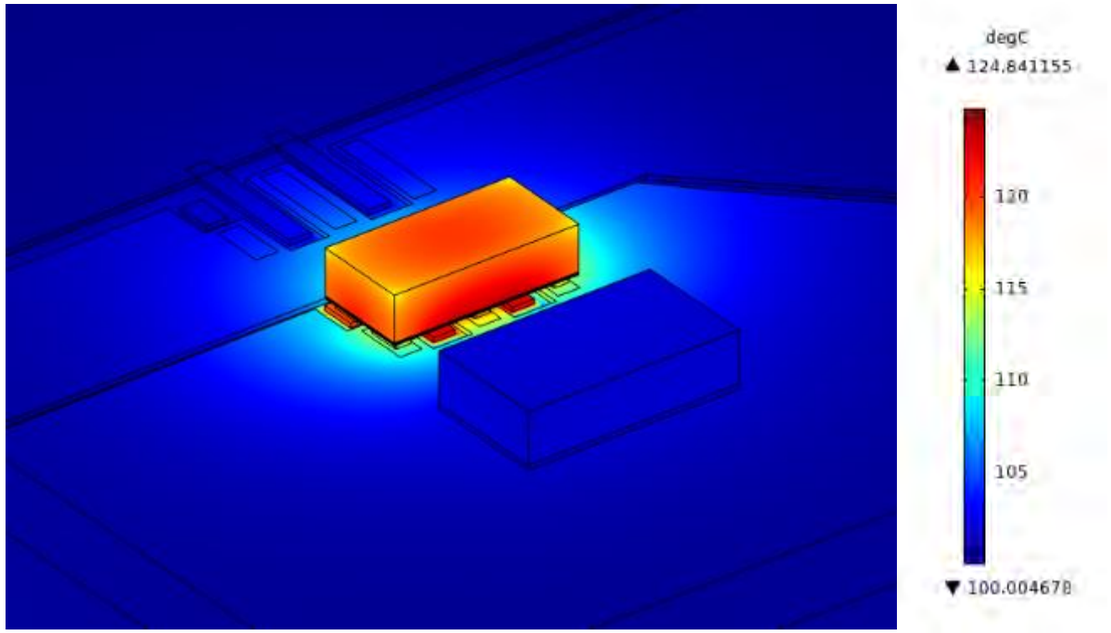
熱のオプション





Option	Shim	Thickness	Filler	$R_{th(JS)}$ (°C/W)	P_D (W @ dT_{JS} = 25 °C)
Baseline	No	0.3 mm max	3.6 W/mK	6.3	4.0
1	Yes	0.3 mm max	3.6 W/mK	6.1	4.1
2	No	0.2 mm max	3.6 W/mK	5.4	4.6
3	No	0.3 mm max	6 W/mK	4.6	5.4
4	**Yes**	**0.2 mm max**	**6 W/mK**	**3.9**	**6.4**

最高の熱特性： 4 mm²、3.9 ℃/W @ 6 W

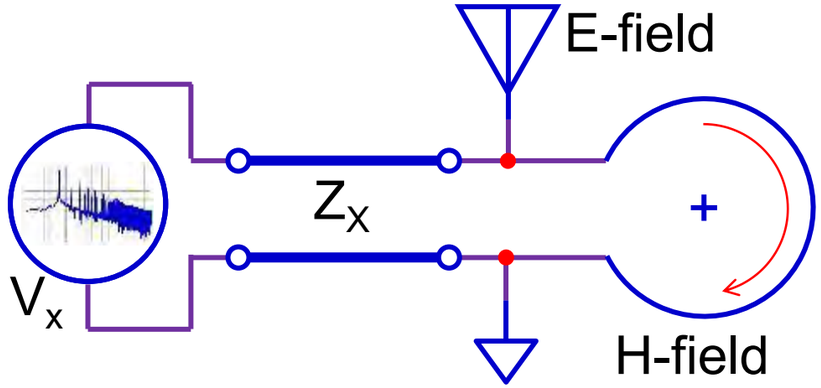


- 1.5 mm x 3 mm x 0.7 mm thermal shim, 6 W/mK gap filler, 0.2 mm spacing to heat spreader
- 123.4 °C average T_J with heat spreader at 100 °C

EMIの考慮事項

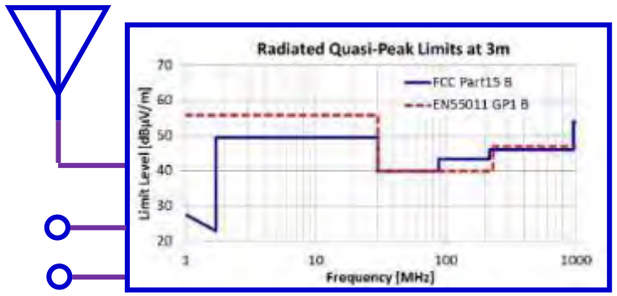
- EMI system overview
- Effect of layout
- Effect of rise/fall times
- Effect of reverse recovery

EMIシステムの概要



Source Transmission Radiator

Radiated
or
Conducted



Receiver

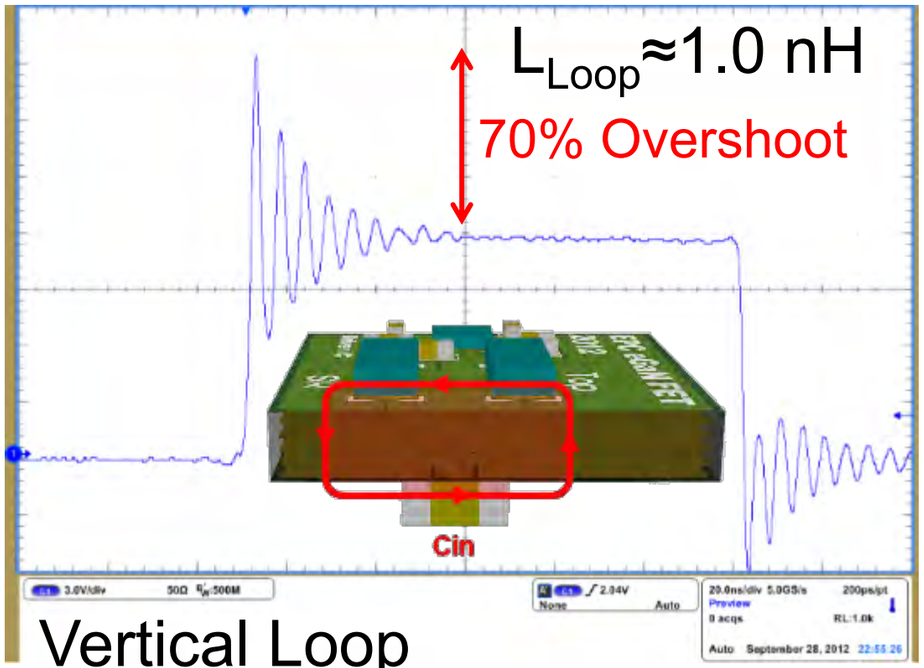
- Corrupted circuit
- Governed by EMI standards

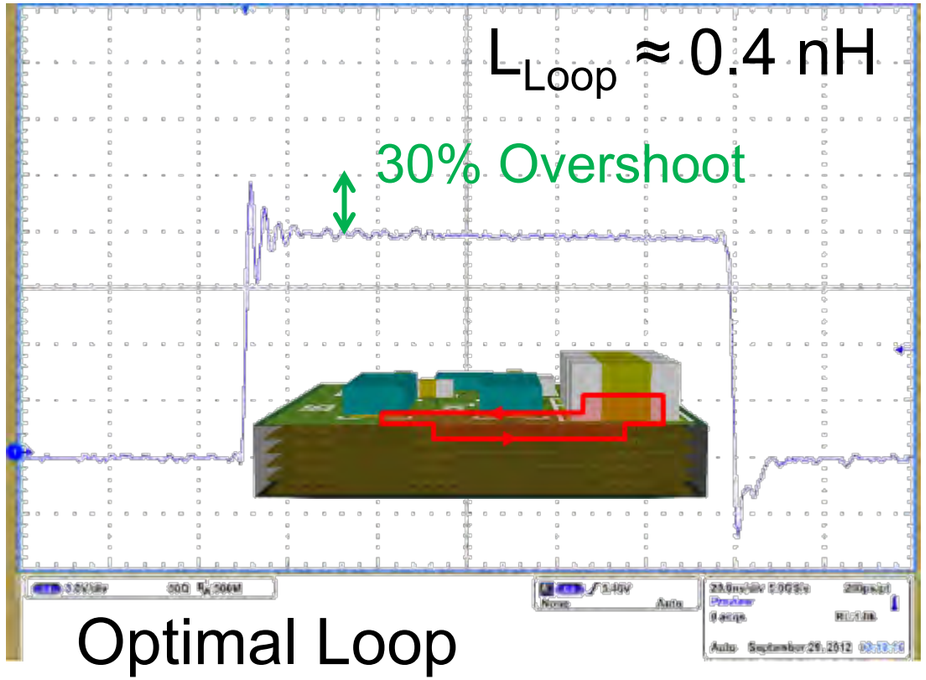
Decreasing cost to reduce EMI

オーバーシュートに対するレイアウトの影響

EMI energy ∝ to:

- V^2 of overshoot magnitude → E-field
- I^2 of current in power loop → H-field





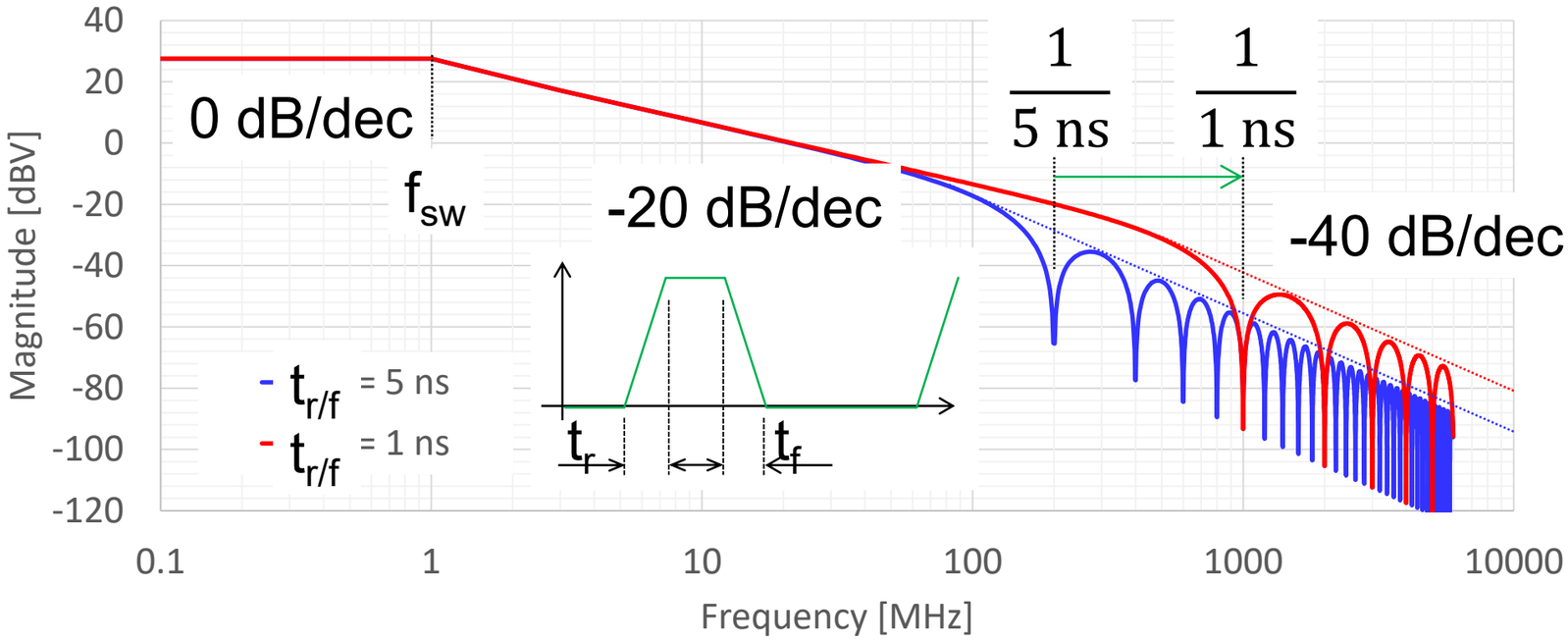
D. Reusch, J. Strydom, “Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter,” Applied Power Electronics Conference, APEC 2013, pp. 649–655, 16–21 March 2013.

立ち上がり／降下時間の影響

Buck Converter Switch-node:

- V_{IN} = 48 V, V_{OUT} = 12 V, f_{SW} = 1 MHz
- Overshoot ringing excluded
- Switch-node mainly radiates as E-field

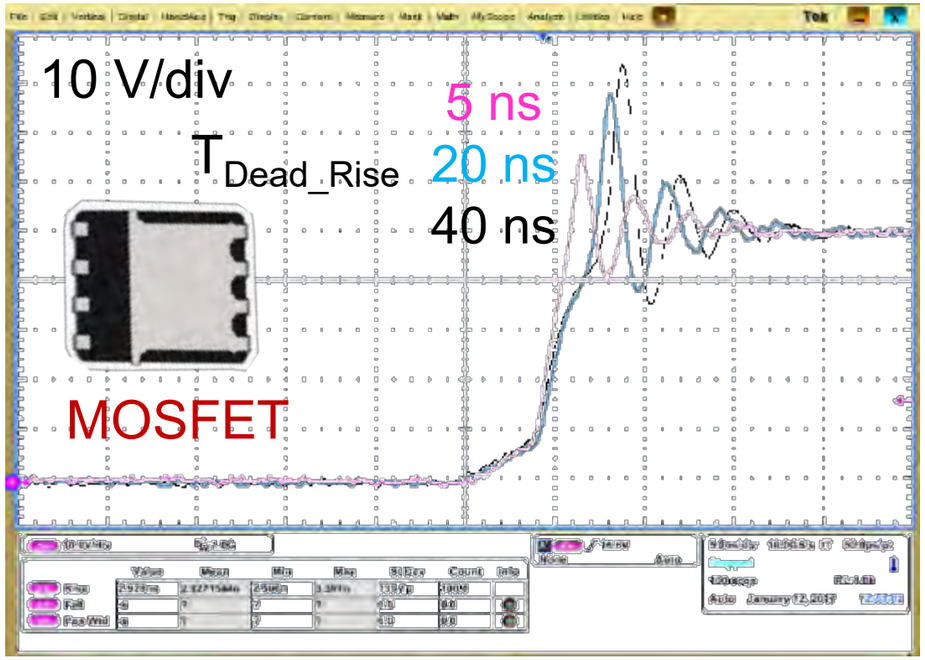
eGaN® FETs switch faster

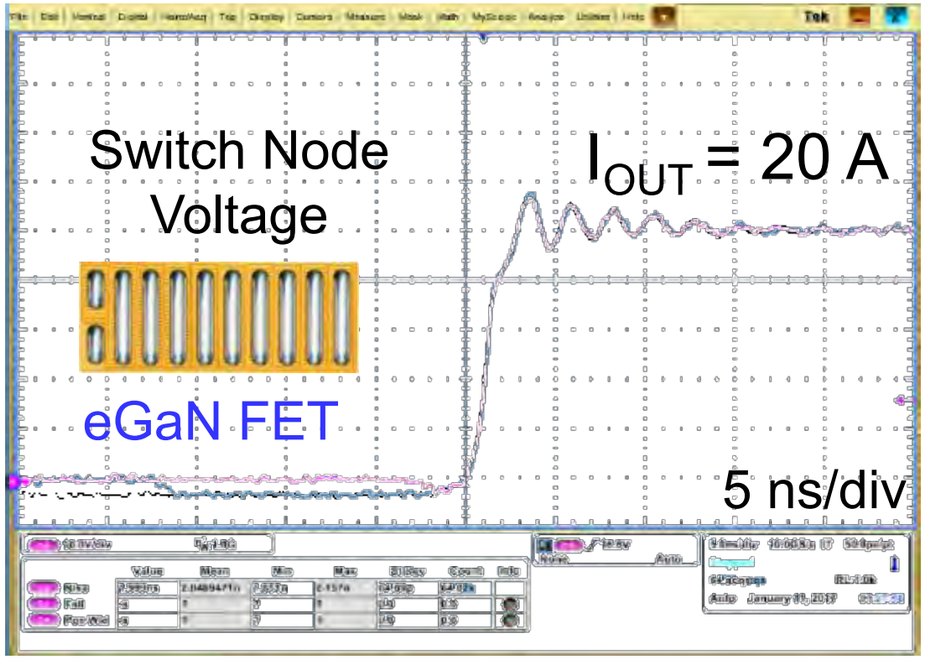


https://incompliancemag.com/article/spectra-of-digital-clock-signals/

逆回復（Q_{RR}）の影響

- Q_{RR} = shoot-through in power loop
- EMI proportional to I^2 of Q_{RR} current
- eGaN FETs have zero Q_{RR}





Glaser, J. S. & Reusch, D., “Comparison of deadtime effects on the performance of DC-DC converters with GaN FETs and silicon MOSFETs,” 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 2016.

eGaN FETはEMI互換

- Adopting simple layout techniques reduces EMI generation
- Shorter switching times only shift frequency content of EMI
- Have zero reverse recovery thus generate lower EMI

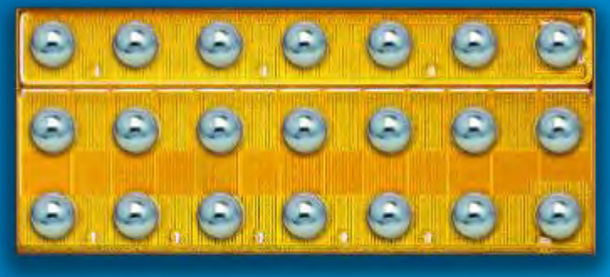
まとめ

- Gate Drive – Strong and growing ecosystem
- Layout – Increase efficiency
- PCB design – Reliable and high yielding
- Thermal management – Simple and inexpensive
- EMI – Better than MOSFETs!

EFFICIENT POWER CONVERSION

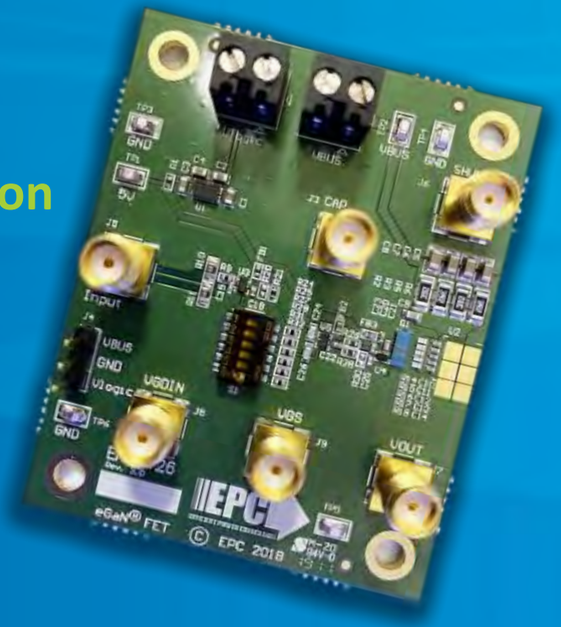
How To GaN Video Series

3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



epc-co.com