Welcome to the second installment of our How2GaN summer series. In this webinar, we will discuss gate drivers suitable for GaN FET converters.
A gate driver interfaces with the PWM signals from a controller to the gate of the GaN FETs and is a critical element for reliable operation of a GaN FET based converter. Factors that need to be considered include the drive capability and matching those to the driving requirements for the FETs. Does the driver have the necessary protection features that collectively ensure reliable and predictable operation under all conditions. Since GaN FETs switch fast, the driver also needs to fast and timing within the driver needs to match timing expected for the FETs. Finally, the driver need to meet the specific requirements for the GaN FETs. So let’s get into the details.
GaN FETs have a reverse conduction mechanism similar to a diode when the gate is held off but with a much higher forward voltage drop of around 2.5 V. This means when using a bootstrap circuit, it is possible to over-charge the bootstrap capacitor when the lower power FET is reverse conducting and employing standard drivers and techniques. GaN FET specific gate drivers are designed to overcome this problem by clamping the bootstrap voltage should the lower FET reverse conduct. In addition, the driver must also remain stable when the switch-node rings below 5 V which can occur following a fast transition into reverse conduction due to the parasitic inductance and capacitance in the circuit.
GaN FETs switch fast
• Applicable to half-bridge drivers
• Driver should be rated >100 kV/µs
• Higher voltage rated FETs switch faster
• Increasing gate resistances reduces dv/dt
  • Efficiency penalty

GaN FET drivers need to be capable of stable operation under much higher voltage transients the traditional MOSFETs, particularly half-bridge drivers. GaN FET drivers should be rated to handle at least 100 kV/us and you can see this from the graph that shows a transition of 73 kV/us. Most commercial GaN FET drivers can already meet this requirement, but it should be noted that higher voltage rated GaN FETs will switch even faster. The switching transient can be reduced by increasing the gate resistance to the FET but comes with an efficiency penalty.
GaN FETs have a low threshold voltage of between 0.7 V and 1.5V and mainly affects the off state. For optimal performance GaN FET drivers come with two drive connections, one for turn on and the other for turn off. This method ensure reliable turn off for the FETs. Traditional MOSFET techniques such as using a diode in the turn-off path is not recommended as the diode adds 0.5V to the turn-off path leaving little margin for error or tolerances and increases the turn off loop impedance thus slowing down the turn off transition.
GaN FET Gate Over-Voltage Management

Max. $V_{GS} = 6.0$ V
- Above limit affects reliability
- Drive gate with 5 V
- Damp ringing with resistor ($R_{on}$)
  - Gate loop inductance ($L_{Gon}$)
  - Common-Source inductance ($L_{CSI}$)
  - Gate Capacitance ($C_{GSon}$)

\[
R_{on} \geq \frac{4 \cdot (L_{Gon} + L_{CSI})}{C_{GSon}}
\]

GaN FETs have a maximum gate voltage rating of 6 V and exceeding that affects the reliability. The recommended drive voltage is 5 V so ringing over-shoot must be managed to prevent the gate voltage exceeding the maximum limit. This can be achieved with the addition of a gate turn-on resistor that provides damping to the inductance of the gate loop. The minimum value of the resistor can be determined using the equation that accounts for the gate capacitance, gate loop inductance and common-source inductance.
GaN FET Gate Under-Voltage Management

Prevents ringing-based turn-on when FET was turned off

- Damp ringing with resistor ($R_{off}$)
  - Gate loop inductance ($L_{Goff}$)
  - Common-Source inductance ($L_{CSI}$)
  - Gate Capacitance ($C_{GSoff}$)

Given that GaN FETs have a low threshold voltage, it is also important to manage the gate under-voltage which can occur at turn-off. The gate loop inductance can induce ringing such that when it rings back up it can exceed the threshold voltage thus turning the FET back on leading to a shoot-through condition. This can be prevented with the addition of a gate turn-off resistor that provides damping to the inductance of the gate loop. The minimum value of the resistor can be determined using the equation that accounts for the gate capacitance, gate loop inductance and common-source inductance.

$$R_{off} \geq \sqrt{\frac{4 \cdot (L_{Goff} + L_{CSI})}{C_{GSoff}}}$$
Gate drivers incorporate protection features and the most prevalent is under-voltage lockout that is used to prevent turn on of the FET when the supply voltage is too low. A too low gate voltage can lead to excessive on-state resistance and hence excessive losses and even failure. The minimum recommended UVLO thresholds are 4 V to enable operation and 3.8V to disable operation. This hysteresis prevents oscillation between states. The UVLO settings apply to both upper and lower FETs in the case of half-bridge drivers.
A key characteristic of gate drivers is propagation delay which is defined as the time taken for the input signal to the gate driver to appear on the output drive stage. Since circuits can have different turn-on and turn-off delays it is important for reliable GaN FET operation that those propagation delays be matched to within 5 ns of each other and should further be less than 50 ns delay in total across the entire rated operating temperature range for the driver. Most GaN FET gate drivers can easily achieve this requirement.
Controllers can generate PWM signals that may become very short, and this can lead to problems for the gate driver and power stage. First, a too short pulse width can lead to incomplete transitions within the gate driver and power circuit. In addition, a too short pulse width can prevent the bootstrap circuit from being properly charged. Protection against minimum pulse width is rarely incorporated into a gate driver so designers must ensure that minimum pulse width protection is built into their controllers.
Here we present an overview of GaN FET compatible gate drivers. Shown on the left are single low side drivers, and on the right half-bridge drivers of various voltage and qualification capabilities and footprints. There are even footprint compatible second source options available too now. All these products are commercially available and there are several more in development so keep and eye open for announcements.
Adapting MOSFET Drivers for GaN FETs

- Driver MUST use an external bootstrap diode (D_BTST)
- Ensure UVLO & operating voltage match GaN FET gate
- Add measures to prevent bootstrap over-charging
  - Add 5.2 V Zener clamp (D_Cmp)
  - Add series current limit resistor (R_Ilim)
  - Schottky anti-parallel diode (D_AP) (where applicable), mostly low voltage

There are still situations where designers want to use a controller IC with an integrated MOSFET based gate driver. It is possible to adapt these drivers to work with GaN FETs as long as certain criteria can be met. The most important is that the bootstrap diode should be external and that the UVLO setting match those required for GaN FETs. When modifying a MOSFET based half-bridge gate driver we recommend adding a 5.2 V Zener clamp diode across the bootstrap capacitor, a current limiting resistor in series with the bootstrap diode and if applicable an anti-parallel diode across the lower FET. These measures collectively work to limit bootstrap over-voltage as explained at the beginning on this section.
Up to now we have relied on a diode, either internal to the gate driver or external, for the bootstrap supply. Gate driver internal diodes have reverse recovery due to process limitations which can induce losses in the upper FET of a buck converter. The bootstrap diode can be replaced by a GaN FET to make a synchronous FET bootstrap supply. A GaN FET thus replaces the bootstrap diode function and comes with the added benefit of regulation for the bootstrap capacitor because it can conduct current in both directions. The synchronous bootstrap FET circuit works best at higher frequencies and/or can be used to eliminate reverse recovery induced switch-node voltage transition distortion.
Sync-Boot Design Considerations

- **Timing:**
  - Turn on - Delay
  - Turn off – Immediate

- **Off state margin** – prevents Sync boot FET conductor power current

- **Drain resistance** – to prevent over-voltage

- **Tiny FET** such as EPC2038 (100 V, 3.3 Ω)

A synchronous bootstrap solution has a few design features that need to be considered. First is timing. The synchronous bootstrap should always be turned on after the main lower FET is turned on and turned off at the same as the main lower FET. This is necessary to prevent the synchronous bootstrap FET from conducting any power current. The reverse voltage of GaN FETs can be programmed higher using a negative voltage on the gate. This allows the reverse conduction voltage of the synchronous bootstrap FET to become higher than the low side main FET thus always preventing inadvertent diode mode conduction. It is also recommended to add some damping resistance to the drain of the synchronous bootstrap FET to prevent over-voltage ringing during high dv/dt transitions. Lastly, the smallest possible FET for the synchronous bootstrap function should be chosen, such as the EPC2038.
Here are the step to retro fit a synchronous bootstrap power supply to the gate driver. First we add the synchronous bootstrap FET where the source is connected to the 5V supply and drain to the bootstrap capacitor circuit. Next, we need a voltage shift of the lower FET gate signal for which we use a capacitor $C_{ENH}$ and diode $D_{ENH}$ is used to charge this capacitor whenever the low FET gate is held low. Now we need to reduce the main supply to the gate driver slightly to prevent the internal diode for ever forward biasing using $D_{4V7}$. Next, we add our turn-off and on timing circuit of $R_{on}$, $R_{off}$ and $D_{off}$. Finally, we need some damping for the drain circuit inductance using $R_{damp}$. This concludes our section on gate drivers. I will now hand over to John Glaser who will cover dead-time effects, $C_{oss}$, reverse recovery and provide us with thermal solutions for cooling the GaN FETs.

Now let’s look at a block diagram review of what we covered so far. The 3 blocks are: PWM Controller, gate driver, and power FETs.

(pagen down) Often the controller and gate driver are combined in one IC. We discussed adapting for GaN FETs.

(pagen down) Another way to partition the blocks is to combine the gate driver and the power FETs, into a Power Stage. This has many advantages. Let’s look at a GaN example in detail.
Introducing the 80 V rated EPC2152 GaN ePower stage that represents the next evolution for GaN FETs; a monolithic integration of the power FETs with complete half bridge gate driver.

There are many benefits to monolithic integration of the power stage such as:

(Build 1) It virtually eliminates common source inductance (CSI), and reduces the power loop and gate loop inductances,

(Build 2) The gate drivers are matched to the FETs and can be designed to optimize switching speed against EMI generation, voltage spikes and efficiency resulting in the shortest practical transition times,

It improves thermal power dissipation distribution allowing optimized FET scaling that yield higher efficiencies. This feature is more useful for high step-down ratio converters,

Integration improves dv/dt immunity that covers all 8 types of switch-node transitions which is important for motor drives,

(Build 3) It simplifies PCB layout and reduces assembly component count for the converter solution.
The IC includes 12 V tolerant CMOS and TTL compatible input buffers, a logic interface with Power-On-Reset (POR), Under-Voltage-Lockout (UVLO) functions, a high voltage, high dv/dt capable control signal level-shifter, a synchronous bootstrap supply that ensures proper high side voltage for the high side gate driver and measures just 3.9 by 2.6 mm.
Additional Resources

- Website List of Ecosystem ICs: https://epc-co.com/epc/Products/eGaNDriversandControllers.aspx
- App Note: The Growing Ecosystem for eGaN® FET Power Conversion
- App Note: eGaN® FET Drivers and Layout Considerations
- Video: How to GaN 04 – Design Basics: Gate Drive
- Reliability: Reliability Report - Phase 12
For more information, please visit us at epc-co.com or submit an inquiry to Ask a GaN Expert
Next Webinars

- August 11, 2021
  Understanding the Impact of Dead-time, $Q_{RR}$, and $C_{OSS}$
- August 25, 2021
  Thermal Management of GaN FETs