National Taiwan University

How to use eGaN Correctly

Peter Cheng
Manager, Asia FAE

Efficient Power Conversion Corporation

2012 Nov.16
Agenda

• What is the Ideal Switcher?
• eGaN FETs Features & Benefits
• eGaN FETs Drivers
• Layout, Layout, Layout !
• Design Example
The Ideal Power Switch

- Block Infinite Voltage
- Carry Infinite Current
- Switch In Zero Time
- Zero Drive Power
- Normally Off
eGaN FETs
Key Features & Benefits

• Enhancement-Mode devices
• Rds(on) per unit area is much smaller
• Much faster switching (tr/tf) time
• Very low Qg and capacitance
• Provide much higher light load efficiency
• No parasitic PN junction body (Qrr=0)
eGaN Characteristics

Note:
All curves here use EPC2001 (100V, 7mΩ)

Figure 2: Transfer Characteristics

- No Negative Temp Coef region like MOSFETs

Figure 4: $R_{DS(on)}$ vs $V_G$ for Various Temperature

- Fully enhanced at 4V
- $V_{TH}$ relatively stable with temperature

Figure 6: Gate Charge

- Very low $Q_G$

Figure 8: Normalized On Resistance Vs Temperature

- $R_{DS(on)}$ rise lower than MOSFET for similar temp rise.

Figure 9: Normalized Threshold Voltage vs. Temperature

- Compared with MOSFET
The slow rise time is due to the load inductance versus load resistance.
eGaN® FETs are Easy to Use

It’s just like a MOSFET except for TWO things

(1) The hyper high frequency capability makes circuits using eGaN® FET very sensitive to layout

(2) eGaN® FET are more sensitive to gate rupture than power MOSFETs
Gate Drive Constraints

- $V_{GS} = 6V$ max, but **4.5V needed** to fully enhance
- High frequency layout required
  - switching time 2-5ns range
- Fast switching causes opportunity for false turn on. $dv/dt$ immunity decreases as device voltage rating increases. A gate drive with a low resistance turn-off (pull-down) is needed.
- The diode $V_f$ is higher than silicon and therefore the gate drive needs to help minimize diode conduction.
- Zero reverse recovery allows very short pulse widths
Minimize Common Source Inductance (CSI)
Switching Interval

- Assumes turn-on / off symmetrical
- Neglects RMS loss effect of $C_{OSS} \frac{dv}{dt}$ current
- Neglects $di/dt$ effect of $C_{OSS} \frac{dv}{dt}$ current
- Neglects miller effect of $di/dt$ across $L_{loop}$
- Neglects gate inductance
Effect on Common source inductance

\[
di/dt = dV_{GS}/dt \times g_m
\]

\[
dV_{GS}/dt = I_G / C_{ISS}
\]

\[
I_G \sim \Delta V / (L_{CSI} \cdot g_M / C_{ISS} + R_G)
\]

5x longer!
Recommended Land Pattern is Defined in the Datasheet
PCB Top View

Relative Sizes (Cu trace, Solder mask, Bump, Stencil)

- Cu trace
- Solder Stencil – 100 μm thick
- Solder Mask
- Solder Bump
Relative Dimensions (Cu trace, solder mask, Bump, stencil)

No Stencil Bench Mount - Tacky flux part number: Kester TSF-6502
Drivers
LM5113 bootstrap voltage regulation, synchronous buck converter evaluation board. Input 48V, output 10V; switching frequency at 800 KHz.

LLP-10 (4mm x 4mm)

μSMD-12 (1.8mm x 1.9mm)
LM5113 layout reference

TI driver layout recommendation
4 external components placement!
Close to driver IC
Example: Buck Converter

- Hard switching:
  - Rise time ~2.5 ns
  - Peak dV/dt ~ 30 V/ns

- Inductor current waveform:
  - Inverted: 8 A load

- Soft switching:
  - Fall time ~4 ns
  - Switching time is load dependent

Drive Circuit

- Q1
- Va
- L1
- VO
- V1
- Q2
- RL
- C
- RC
- R
Ideal Hard Switching

\[ P_{TR} \approx \frac{V_{IN} \times I_{OFF} \times Q_{GD}}{2 \times I_G} \]

\[ P_{TF} \approx \frac{V_{IN} \times I_{OFF} \times Q_{GS2}}{2 \times I_G} \]
Buck Converter Parasitics

$L_S$: Common Source Inductance

$L_{Loop}$: High Frequency Power Loop Inductance

$V_{IN} = 12$ V, $V_{OUT} = 1.2$ V, $F_S = 1$ MHz, $I_{OUT} = 20$ A
Lloop & CSI impact on turn on

Impact of high frequency loop inductance, $L_{\text{Loop}}$, on turn on. Ideal waveforms: Solid line. Waveforms with parasitic influence: Dashed line.

Impact of common source inductance, $L_s$, on turn on. Ideal waveforms: Solid line. Waveforms with parasitic influence: Dashed line.
Lloop & CSI impact on turn off

Impact of high frequency loop inductance, \( L_{\text{Loop}} \), on turn off. Ideal waveforms: Solid line. Waveforms with parasitic influence: Dashed line

Impact of common source inductance, \( L_s \), on turn off. Ideal waveforms: Solid line. Waveforms with parasitic influence: Dashed line
Packaging Evolution

Device Loss Breakdown

- **Power Loss (W)**
  - **So-8**: 18% Package, 82% Die
  - **LFPAK**: 27% Package, 73% Die
  - **DirectFET**: 47% Package, 53% Die
  - **LGA eGaN**: 53% Package, 47% Die

- **V\text{IN} = 12V**
- **V\text{OUT} = 1.2V**
- **I\text{OUT} = 20A**
- **F\text{S} = 1MHz**

- **Efficiency (%) vs Switching Frequency (MHz)**
  - **So-8**: High efficiency at low switching frequencies, drops at higher frequencies.
  - **LFPAK**: Improved efficiency compared to So-8, especially at higher frequencies.
  - **DirectFET**: Further improvements, maintaining high efficiency across a wide range of frequencies.
  - **LGA eGaN**: Highest efficiency, maintaining performance across all shown frequencies.

EPC - The Leader in eGaN® FETs

National Taiwan University 2012
www.epc-co.com
Experimental Efficiency

\[ V_{IN} = 12 \text{ V}, \quad V_{OUT} = 1.2 \text{ V}, \quad F_s = 1 \text{ MHz}, \quad L = 150 \text{ nH} \]
Peak Voltage Comparison

$V_{IN} = 12\, V$, $V_{OUT} = 1.2\, V$, $F_S = 1\, MHz$, $L = 150\, nH$
Experimental Waveforms

\[ V_{IN}=12 \text{ V}, \quad V_{OUT}=1.2 \text{ V}, \quad F_{S}=1 \text{ MHz}, \quad L=300 \text{ nH} \]
Experimental Waveforms

$V_{\text{IN}} = 24\ V, \ V_{\text{OUT}} = 1.2\ V, \ F_S = 1\ MHz, \ L = 300\ nH$
Optimal Layout Efficiency

\[ V_{\text{OUT}} = 1.2 \text{ V}, \, F_s = 1 \text{ MHz}, \, L = 300 \text{ nH} \]


Si MOSFET: Top: BSZ097N04 SR: BSZ04N04
Optimal Layout Power Loss

$V_{OUT} = 1.2$ V, $F_S = 1$ MHz, $L = 300$ nH

Si MOSFET: Top: BSZ097N04 SR: BSZ04N04
Summary

eGaN FETs can improve high frequency hard switching converter performance:

• Lower Switching Charge ($Q_{GD} + Q_{GS2}$)
• Lower Gate Charge ($Q_G$)
• Improved Packaging
• Improved Layout Capability
What Other Advances are Needed?

• High speed digital controller ICs and integrated controller/driver ICs.
  – Application specific controllers to reduce time-to-market
  – Dynamic deadtime control with ~1ns resolution
  – Synchronous PFCs
  – Envelope Tracking Controllers

• Note: Improvements in magnetics would be helpful…
The end of the road for silicon.....

is the beginning of the eGaN FET journey!