Designing Manufacturable and Reliable Printed Circuit Boards Employing Chip Scale eGaN® FETs

Michael de Rooij, Efficient Power Conversion, U.S.A., Michael.derooij@epc-co.com
Alana Nakata, Efficient Power Conversion, U.S.A., Alana.nakata@epc-co.com

The Power Point Presentation will be available after the conference.

Abstract

eGaN FETs, which are available in non-traditional chip scale packages (CSP) as land grid array (LGA) and/or ball grid array (BGA) formats, have repeatedly demonstrated higher power density and higher efficiency performance than equivalent MOSFETs across various applications [1, 2]. Those improvements are contingent upon proper layout practices documented extensively in [1, 3] that minimize unwanted parasitic elements. Over the seven years since eGaN FETs were first launched into the market there have been a total of 127 device failures out of a total of more than 17 billion hours in actual use in the field, 75 of which were a result of poor assembly technique or poor printed circuit board (PCB) design practices [4]. Designers are becoming more familiar with the PCB design rules that affect manufacturability. eGan FETs and are less forgiving compared to MOSFETs due to their relatively smaller sizes. This paper will cover the various guidelines for PCB design that maximize the performance of eGaN FETs and reliability yet still rely on existing PCB manufacturing capabilities.

1. Introduction

eGaN FETs have consistently demonstrated superior electrical performance over their MOSFET counterparts in switching power electronic circuits [1] and represent a shift in how those circuits are designed. Their high switching speed means careful attention to many critical design aspects of the power and drive circuits, such as common source inductance (CSI), power loop inductance [3], and gate loop inductance is required. Most of these aspects are reasonably well understood and many designers have embraced them into their designs.

Extensive testing has also proven that eGaN FETs are reliable [4] when designed into application circuits correctly. Since they were first launched into the market seven years ago there have been a total of 127 device failures out of a total of more than 17 billion hours in actual use in the field, 75 of which were a result of poor assembly technique or poor printed circuit board (PCB) design practices [4]. PCB design is also the highest requested design support for eGaN FETs and hence will be discussed in detail in this paper.

PCB design is no longer simply a connection of conductors with insulating layers anymore but requires a deep understanding of the complexities and challenges that need to be overcome to build a PCB and assemble that ensures the reliability of the components attached to them. These challenges will only increase over time with the ever present market demand for smaller and more energy dense converters.

eGaN FETs are available in non-traditional chip scale packages (CSP) as land grid array (LGA) and/or ball grid array (BGA) formats as shown in figure 1. Their small feature sizes require careful attention to the design in order to avoid PCB and assembly related problems such as dendrite formation; poor solder adhesion, and more.

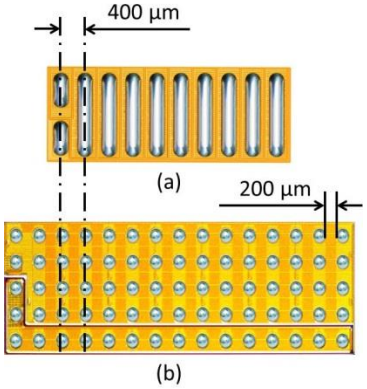

Fig. 1. eGaN FETs are a small feature land grid array (LGA) (a) and/or ball grid array (BGA) (b) formats.

To better understand the importance of these issues some examples will be given in the next section.

2. Issues related to poor PCB design and assembly practices

There are many issues that can be present if proper PCB design is not followed. These issues can be exacerbated by poor assembly techniques. This section presents the many issues while explaining their origins.

2.1. Electrical Dendrites

Electrical dendrites are considered ionic contamination that are formed when the flux is exposed to an electric voltage and forms conductive crystals [5]. The higher the voltage the faster dendrites can form. Electrical dendrites can quickly lead to failures because during their formation they can generate a lot of heat in addition to the short circuit created. Figure 2 shows an example of dendrite formation around a solder bar of an eGaN FET.

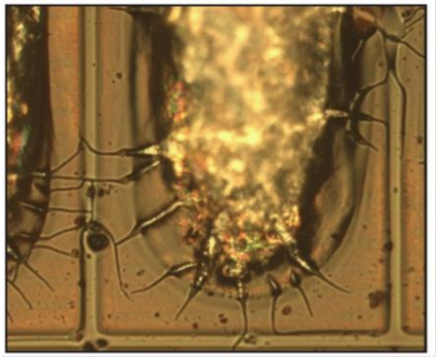

Fig. 2. eGaN FET showing electrical dendrite formation after exposure to residual flux.

2.2. Thermal dendrites

Thermal dendrites are a relatively new concept and are not to be confused with electrical dendrites although they may appear similar. It is surmised that thermal dendrites are caused by flux cracks formed during furnace cool down. Solder, which has not cooled as much can then diffuse into the flux cracks. These solder filaments can significantly reduce the electrical distance between bumps and can breakdown during operation. Flux cracks can remain after the assembly process even if using no-clean flux. Figure 3 illustrates what a flux crack looks like on a PCB formed in the absence of a die.

Thermal dendrites are slightly different from traditional thermal dendrites seen in metal melts where the presence of a nucleation source can lead to “arms” growing from the particles in a super-cooled liquid forming dendrites [8, 9, 10]

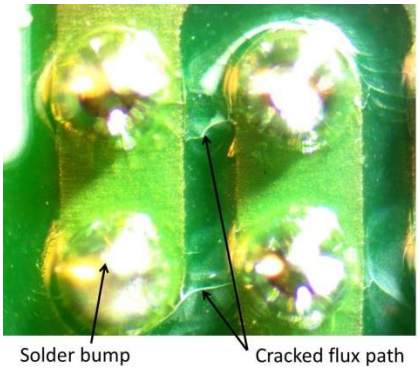

Fig. 3. Example of thermal dendrite formation path in cracked residual flux without a die present.

Examples of thermal dendrites are shown in Figure 4.

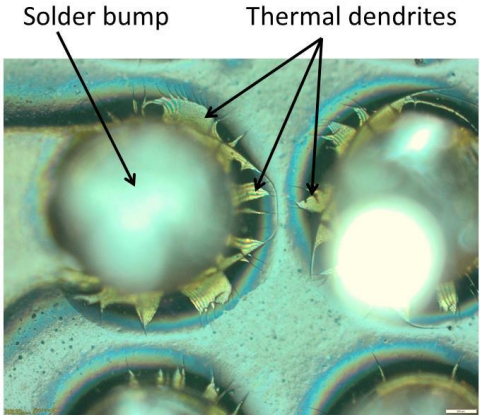

Fig. 4. eGaN FET showing thermal dendrite formation in cracked residual flux.

2.3. Poor solder adhesion

Contaminated solder pads can lead to poor solder adhesion, voiding and large un-wetted areas. Most contamination arises from a poor PCB fabrication process where soldermask residue is left on the pads such as from contaminated cleaning liquids.

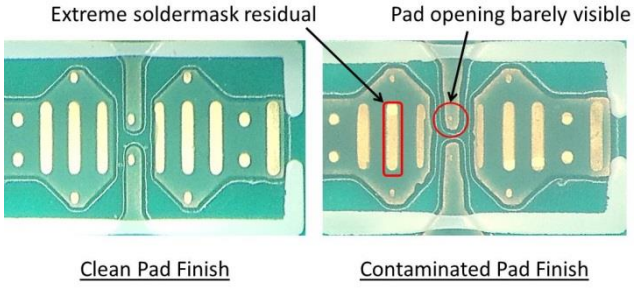

Fig. 5. Examples of a contaminated pad versus clean pad.

Figure 5 shows an example of a clean pad finish (left) alongside an extreme contaminated pad finish (right). Poor solder adhesion can lead to open circuits and in high current capable devices will lead to excessive current densities as currents are forced into undefined directions that will ultimately cause the device to fail. Figure 6 shows an example of a solder wetting issue.

Fig. 6. Example of poor solder wetting.

2.4. Solder bump cracking

Solder bumps mainly crack due to thermally induced mechanical stresses. If the solder solidifies under stress during the assembly process, this can lead to accelerated failure as the solidified stresses are added to those induced by thermal expansion and contraction.

A well-known industry analytical model [6] for strain on solder joints during thermal cycling is:

$$\varepsilon = \frac{(\Delta\alpha \cdot \Delta T \cdot DNP)}{h} \quad (1)$$

where:

ε = Strain on solder joint

Δα = Difference in coefficient of thermal expansion between die and PCB [$°C^{-1}$]

ΔT = Cyclic temperature swing [°C]

DNP = Distance from neutral point (stress centroid based on die size & solder bump/bar locations) [m]

h = Solder joint standoff height [m]

Equation 1 suggests a very tall solder bump height to reduce the thermally induced stress to near zero; which is not practical. The right balance between thermally induced stresses and reliability is typically determined by the manufacturer of the devices and given in their datasheets. In the case of eGaN FETs a solder mask defined pad further reduces the stresses induced during the reflow process and will be presented in section 3.

An example of solder bump cracking is shown in figure 7.

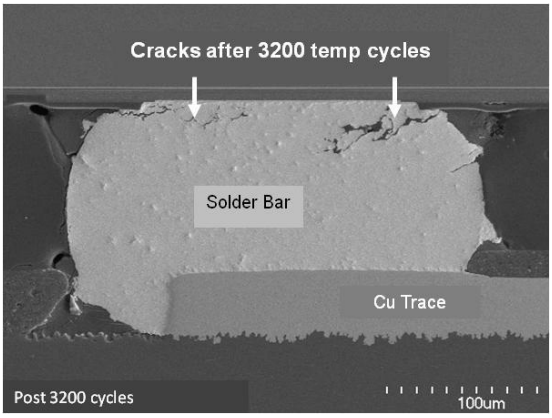

Fig. 7. Cross section x-ray of an eGaN FET solder bump showing bump cracking.

2.5. Solder voids

Solder voids are open volumes within the solder as shown in figure 8.

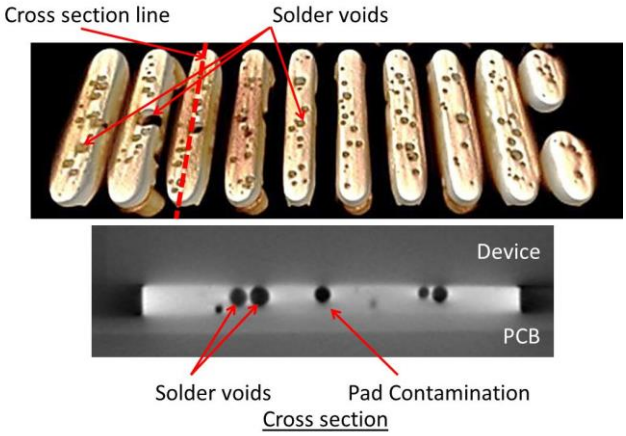

Fig. 8. 3D-X-ray (top) of an eGaN FET showing excessive solder bump voids. Contaminant on the pad to solder interface leads to voids formation (bottom)

Solder voids can have various causes including poor solder adhesion to the pad, outgassing from contaminated pads during reflow, insufficient device standoff height [7] and incorrect solder profile.

The voids reduce the contact area between the device and PCB pad and induce uneven mechanical and thermally induced stresses within the solder bump. Over time these voids can grow and lead to failure.

1.5. Die tilt

Die tilt can be caused by several reasons such as poor solder adhesion, uneven solder paste dispensing, excessive vibration during reflow, non-optimized temperature profile and oversized

solder mask and / or oversized solder stencil apertures. Die tilt is detrimental to device reliability and the thermal mechanical stress and not consistent across the die. It may also be an indication of short or open circuit bumps. Figure 9 shows an example of a tilted eGaN FET.

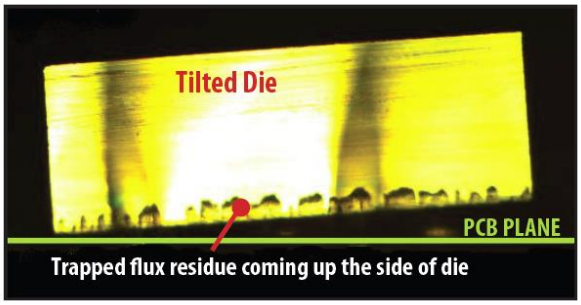

Fig. 9. Side view of an eGaN FET with severe die tilt after soldering.

3. Printed circuit board design considerations for eGaN FETs

Power designers may not be as familiar with fine pitch devices as their digital circuit counterparts. This section will cover the many design aspects designers need to be aware of when designing a footprint for eGaN FETs.

The quality of the solder bump interfacing the eGaN FET to the PCB is crucial for a reliable electrical, thermal and mechanical connection. The factors that define this quality include its symmetry, volume, height, and finish. These factors may be overlooked by a designer primarily focused on layout, and thus the device manufacturer must take on the responsibility for providing clear and simple guidelines in their datasheets. Those guidelines include the recommended footprint (copper dimension and soldermask opening) and solder paste stencil designs.

3.1. Soldermask defined pads

For eGaN FETs and integrated circuits a soldermask defined (SMD) footprint for the LGA and BGA bumps is recommended as shown in figure 10 (right). Figure 10 (left) shows a non-soldermask defined (NSMD) footprint pad that is typically used for PCB deigns. In our investigations of failures at customers' assembly facilities we have found instances where PCB manufacturers modified Gerber files to accommodate their internal manufacturing design guidelines developed for much larger packages. A design review prior to final board release would highlight this problem prior to incurring scrap or rework expenses in assembly. Figure 11 shows how the SMD pad works to reduce mechanical stress by ensuring a symmetrical bump after soldering. In contrast, using a NSMD footprint can result in an asymmetrical solder bump as 100% perfect registration between the copper and mask layers in not likely. In the case of the SMD footprint, immunity is ensured within the manufacturing tolerances of the PCB.

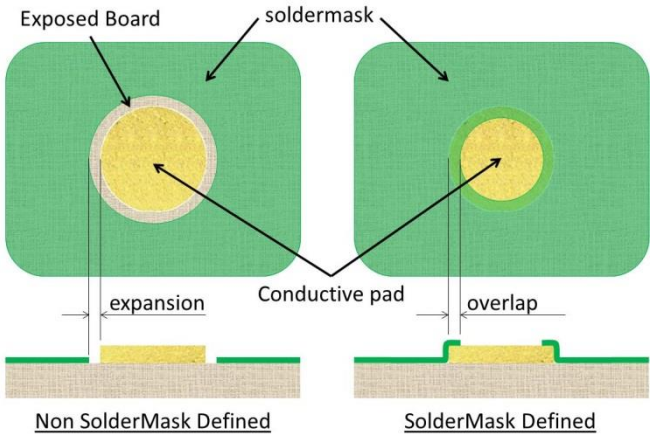

Fig. 10. Soldermask defined (SMD) versus non-soldermask defined (NSMD) pad.

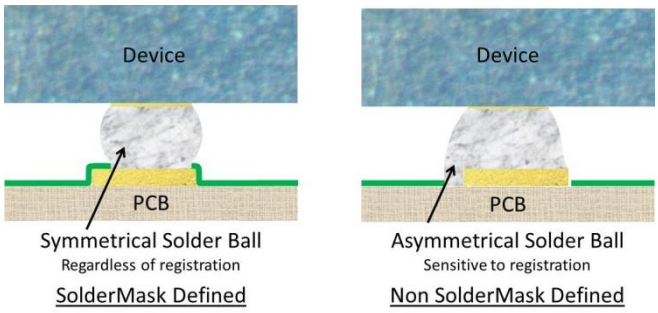

Fig. 11. Effect of copper to soldermask layer registration on the solder ball symmetry.

3.2. Soldermask quality

Not all soldermasks are the same and it is important to know what to look for when specifying the soldermask to yield a high quality PCB with the thickness and consistency being the most important. If the soldermask is too thick it will make it difficult to properly dispense the solder paste as the distance the paste needs to be pressed into becomes larger. If the consistency of the soldermask is not uniform it can lead to bumps that further prevent the stencil from be seated properly against the board. Solder mask defects or excessive soldermask openings can result in reduced bump height and lead to

cracking and/or die tilt. The resultant deformed bumps will cool with mechanical stress that can accelerate thermally induced failures.

Suitable soldermasks for PCBs employing eGaN FETs fall under IPC-SM-840 class T such as Taiyu 4000HFX L.P.I, PSR-2000/LF02/CA-25 or equivalents. It is important to specifically state in the PCB fabrication files that the soldermask should not be enlarged or modified by the PCB manufacturer.

Laser Direct Imaging (LDI) should be used to register the solder mask to a tolerance of at least 2 mils with respect to the copper layers. Finally, the solder mask should not be clipped. This places greater emphasis on the designer to ensure that the layout software has the correct design rules setup.

3.3. Solder bump volume

The height of the solder bump between the boards and the device is also critical for mechanical stress and has been determined to yield a balance between reliability, electrical and thermal performance. If the bump height is too low then the device will experience high thermally-induced mechanical stresses that will result in solder ball or under bump metal fatigue, while devices seated too high will experience higher electrical and thermal stresses (due to reduced heatsinking effects from the PCB) [4]. The optimal height is different for each device. For LGA and BGA devices additional options such as various solder types must also be part of the design decisions. Figure 12 shows how different solder types can yield different stencil designs.

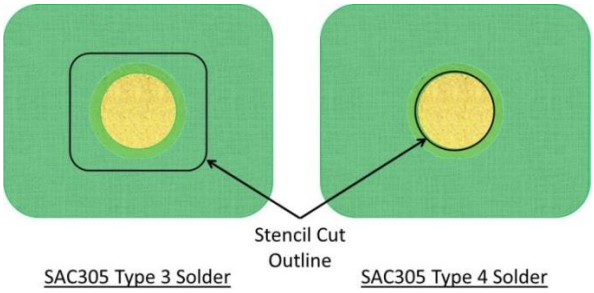

Fig. 12. Impact of solder type on stencil design.

3.4. Solder pad finish

Many designers opt to use a hot air solder leveling finish (HASL) for their boards which deposits solder on the pads. This solder deposit yields small amounts of solder on the pads that add to the amount of solder that will be dispensed via the stencil and will be included in the bump solder volume, ultimately affecting the finished bump volume and hence its quality. In addition, the HASL process is imprecise and typically yields uneven solder on the pads of varying quantities as can be seen in figure 13 (right). This can lead to die tilt and/or open solder joints. It is therefore recommended to use an electroless nickel immersion gold (ENIG) pad finish that yields a very uniform and flat pad as shown in figure 13 (left).

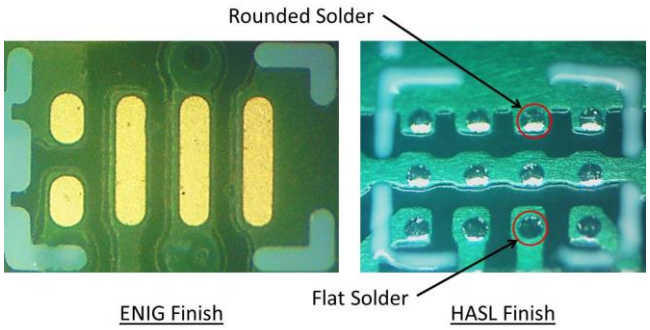

Fig. 13. ENIG finish versus HASL finish showing uneven solder heights.

For the ENIG finish a typical nickel (Ni) thickness of 150 µinches and gold (Au) thickness of 3 - 5 µinches in accordance with IPC-4552 is recommended.

3.5. Silkscreen

While silkscreen has traditionally played a minor role in PCBs, it can be a part of the reliability function because it does not have zero thickness and as a result and impede the flow of flux during reflow process.

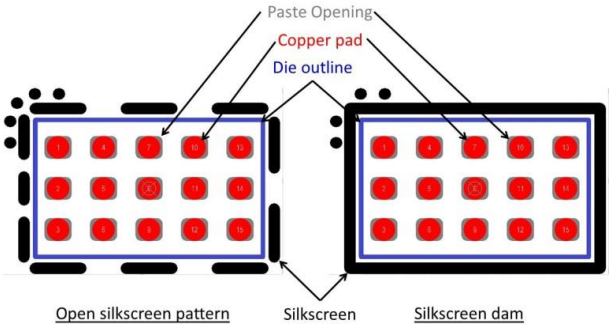

Fig. 14. Device land pattern with open device outline silkscreen (left) and dammed closed silkscreen device outline (right).

If the flux flow is impeded then it can lead to die tilt and flux residue. The silkscreen is also used to register the die into place during the assembly process and many designers will tend to design a

fully enclosed silkscreen pattern outlining the device as shown in figure 14 (right). This can lead to damming when the flux cannot flow out from under the die during reflow and is particularly acute with thick silkscreen. Flux damming can result in uncured flux being present under the die and can lead to thermal dendrite formation.

Device damming can be prevented by simply opening the silkscreen walls at various locations as shown in figure 14 (left).

3.6. Vias

Vias form an integral part of the PCB design for eGaN FETs due to their small size and electrical performance requirements [3]. Via dimensions are at the discretion of the designer who needs to be aware of several limitations depending on how the via is used.

The basic via is simply a vertical connection between the layers of the PCB and is made up of a hole with annular ring of copper. Manufacturing restrictions limits holes sizes to a minimum of 6 mils and minimum annular ring dimension of 5 mils. Designers may already recognize that this already exceeds the dimensions of some eGaN FETs bump spacing and a compromise in one direction may be made. Vias should always be tented (covered with soldermask) to prevent solder from wicking into the hole during the reflow process and to prevent voltage clearance issues due to exposed copper in proximity to the die.

In some cases it may be necessary to place a via under a device pad. In this case the via must be filled and capped to prevent the solder required for optimal bump height from draining into the hole during reflow. Capping is required to prevent the filler from outgassing under the solder bump. This via should be tented in the layout design software so that the pad soldermask opening, should it overlap the via, will determine which part of the via to cover or expose. The finished via must essentially have the same height as the remainder of the pad. This will ensure proper solder paste dispensing.

Some designs may require many vias that are used to distribute the current and increase the total current transferred to another layer. Despite the vias being connected to the same electrical node manufacturing restrictions require at least 10 mill wall to wall spacing for vias that will prevent weaknesses in the board and ensure a uniform board thickness finish. Tented vias near or within the device can lead to high spots that cause the stencil to sit up higher and can lead to solder over deposit during manufacturing. When using vias close to or within the device make sure the PCB manufacturer is aware of your stencil seating concerns.

3.7. Layer registration

The many layers that make up the PCB need to be aligned (registered) with each other. This ensures a proper functional board and is specified by providing a registration tolerance. Layers of the same type are typically specified differently from layers of different types. Layers typically registered with each other are copper to copper, copper to soldermask, copper to hole, and copper to silkscreen (not typically specified but is helpful for die placement).

Most layers can be specified with a registration tolerance of 2 mils with respect to a copper layer except holes which should use 3 mils minimum.

3.8. Layer stackup

A stackup defines the thickness of each of the layers that make up the PCB. PCB's for eGaN FETs typically use copper thicknesses between 1 and 2 oz (35 & 70 µm) depending on the design and how much current density is required. The insulating layers are typically make using materials such as FR4 or FR370-HR. Substrates with a higher glass transition (T_g of at least 180°C) ratings are preferred for higher reliability. The thicknesses of the insulating layers are driven by the balance between manufacturability and electrical properties. The optimal layout [optimal] for 100 V devices specifies a 5 mil core thickness between layers 1 and 2. Due to symmetry requirements, this will also force layers 3 and 4 to also be 5 mils thick with the prepreg layer being adjusted to meet the final board thickness (typically 1.5 mm or 62 mils). For higher voltage devices and to ensure proper creepage requirements a min core thickness of 12 mils is recommended. The prepreg layer will then adjust to approximately 25 mils. Figure 15 shows a typical PCB stackup.

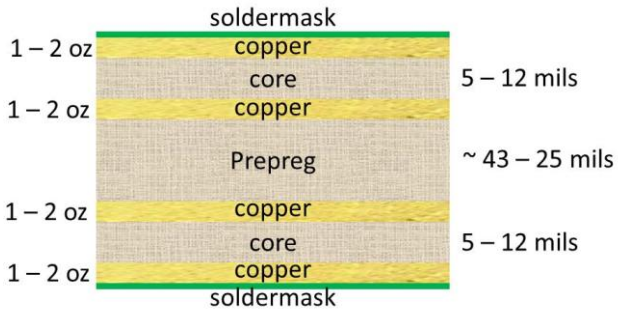

Fig. 15. PCB stackup for a typical PCB suitable for eGaN FETs.

3.9. Board flatness

A lesser known PCB specification is board flatness. It is still an important specification because a board the bows too much can prevent the stencil from being properly seated on the board and will lead to potential pads not being properly dispensed with solder paste. An array with maximum horizontal or vertical dimension of 200 mm (8000 mils) should be specified with a flatness to be within 40 mm per meter (7.5 mil per inch).

3.10. Fiducials

Fiducials are used for component registration during placement process of assembly. Due to the fine pitch of eGaN FETs it is typically required to add fiducials to the PCB. There are two types of fiducials; a global and a local. Global fiducials are used to align a PCB array and local fiducial are used on a single board. Most designs will require local fiducials to accommodate eGaN FETs. A typical board should have at least 3 fiducials with at least 2 aligned vertically and 2 aligned horizontally. Fiducials should be placed as close as possible to the board edge and as far apart from each other. This improves the registration over longer distances. If the eGaN FETs are located more to one side of the board, then the fiducials should be located in their proximity. A 40 mil diameter fiducial should be sufficient for most assemblers.

3.11. Board or array size limits

PCBs and PCB arrays using eGaN FETs should also be limited in size. Larger boards are more difficult to register for precise assembly of the eGaN FETs with their small feature size. Boards and arrays should be limited to 200 mm on each side. For arrays it is recommended to rotate the boards in an attempt to locate all of the eGaN FETs of the various boards as close to each other as possible. Allowing larger boards to be used as the registration location can still be located as close as possible to the eGaN FETs.

4. Assembly related considerations for eGaN FETs

The discussion up to this point has focused on the PCB design and its manufacturability. In this section the assembly process that goes hand in hand with the PCB will be presented.

4.1. Solder paste choice

EPC currently uses Kester NXG1 Type 3 SAC305 and Kester NP505-HR SAC305 Type 4 solder pastes for soldering eGaN FETs. Both pastes are no-clean flux with 88.5% metal.

It is recommended to clean the flux from the board even if no-clean flux is used in order to prevent the formation of thermal and electrical dendrites. EPC uses Kyzen Aquanox A4625 chemical in a Nu/Clean AQUABATCH XL standard system manufactured by Technical Devices Company to remove the no clean flux.

If a no-clean flux is used and it is not rinsed off, then a post reflow bake for a minimum of 60 minutes. at 150°C is recommended, with 4 hours preferred. This ensures that the no-clean flux is properly cured and helps prevents dendrite formation.

If a water rinseable flux is used, the eGaN FET needs to be rinsed on all four sides to ensure proper flux removal. A tilted device can obstruct the flow of the rinse and cause flux to remain trapped under the die. For this reason, using a no rinse solder flux with low ionic content and then rinsing the no rinse flux is recommended.

4.2. Stencil design

A laser-cut stainless steel stencil of 100µm thickness is recommended. A smooth wall laser-cut stencil is more likely to release the desired dispense volume. Type 3 solder paste requires a larger opening than Type 4 solder and recommendations are available for both for each die configuration. In the case that a stamped stencil must be used, it may be necessary to enlarge the opening slightly to compensate for proper solder release volume.

4.3. Reflow profile

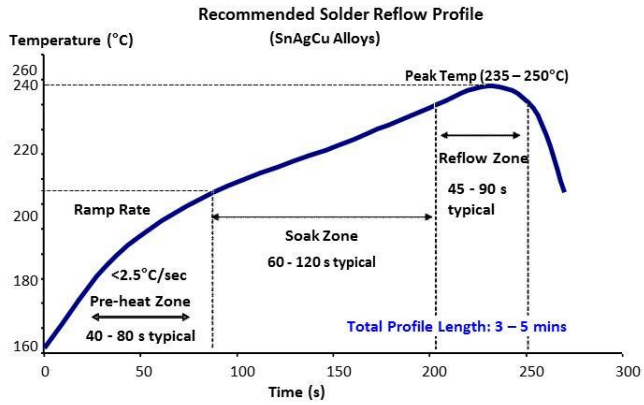

Fig. 16. Recommended solder reflow profile.

Figure 16 shows the recommended reflow profiles for eGaN FETs based on the solder paste manufacturer recommendations for the pastes referenced in section 4.1. Furnace cooling profiles can be adjusted to try and attenuate the flux

cracking, but this adds complication to the assembly process. The vendor recommended reflow profiles should be followed for the paste being used.

5. Conclusions

Reliability and quality control are inter-related. Understanding how to design PCB's for eGaN FETs aids in ensuring that the boards will yield reliable solder joints and reliable operation. This is more critical due to the small size and high current densities of eGaN FETs. Quality follows many steps described in this paper from solder mask defined pads that ensure low stress bumps to ensuring contamination free pads and proper solder profiles. Failure to follow the prescribed steps can lead back to the issues such as electrical and thermal dendrites, poor solder adhesion, solder voiding, bump cracking and die tilt that were presented in this paper.

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