The eGaN® FET Journey Continues

Using eGaN® FETs for Envelope Tracking Buck Converters

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Agenda

• Overview of Envelope Tracking
• Why eGaN® FETs for Envelope Tracking
• Maximizing Device Performance
• Experimental Results
• Current Limitations
• Summary
• Q & A
Overview of Envelope Tracking
Why Envelope Tracking?

Source: Cisco VNI Mobile Data Traffic Forecast

66% Compound annual growth rate (CAGR)

Reference: Nujira.com website

3G (W-CDMA)
3.5 dB PAPR (~2:1)

3.5G (HSUPA)
6.5 dB PAPR (~5:1)

4G (LTE / OFDM)
8.5 dB PAPR (~7:1)

Same average
Effect of PAPR

- Fixed supply
- Peak efficiency up to 65%
- Average efficiency only 25%
- Increasing PAPR

PAPR = 0dB
Peak efficiency up to 65%

Average Power vs. Peak Power

Output Probability
Effect of Envelope Tracking

Average efficiency ~50% (incl. ET)

Only 1/3 the losses

60 ~100MHz BW ET for 4G LTE
Improvement in switching device performance buys:

• Improves overall ET efficiency
• Increases Switcher stage bandwidth
• Simplifies Linear stage design / Removes it entirely?
• Increase system BW which increases RFPA fidelity

Why eGaN FETs for Envelope Tracking
Idealized Switching

\[ P_{TCR} \propto \frac{V_{IN} \cdot I_{ON} \cdot Q_{GS2}}{2 \cdot I_G} \]

\[ P_{TVF} \propto \frac{V_{IN} \cdot I_{ON} \cdot Q_{GD}}{2 \cdot I_G} \]
Hard-Switching Figure of Merit

\[ FOM_{HS} = (Q_{GD} + Q_{GS2}) \cdot R_{DS(on)} \cdot (pC \cdot \Omega) \]

- EPC Gen 4
- EPC Gen 2
- Vendor A
- Vendor B
- Vendor C
- Vendor D
- Vendor E

Vendor Comparison:
- Vendor A: 3.5x
- Vendor B: 6.1x
- Vendor C: 8.5x

Conditions:
- Drain-to-Source Voltage: \( V_{DS} = 0.5 \cdot V_{DSS} \)
- Drain Current: \( I_{DS} = 20 \text{ A} \)

www.epc-co.com EPC - The Leader in eGaN® FETs

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## High Frequency eGaN FETs

<table>
<thead>
<tr>
<th>EPC Part No.</th>
<th>BV (V)</th>
<th>Max. $R_{DS(ON)}$ (mΩ) ($V_{GS} = 5V, I_D = 0.5 A$)</th>
<th>Min. Peak Id (A) (Pulsed, 25 °C, $T_{pulse} = 300 μs$)</th>
<th>Typical Charge (pC) $(V_{DS} = 20 V; V_{GS} = 0 V)$</th>
<th>Typical Capacitance (pF)</th>
<th>$Q_G$</th>
<th>$Q_{GD}$</th>
<th>$Q_{GS}$</th>
<th>$Q_{OSS}$</th>
<th>$Q_{RR}$</th>
<th>$C_{ISS}$</th>
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### Hard Switching FOM

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<th>230mΩ</th>
<th>90mΩ</th>
<th>200mΩ</th>
<th>71mΩ</th>
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<tr>
<td>Q(_{\text{GS2}})</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Q(_{\text{GD}})</td>
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<td>100 V eGaN FET</td>
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<tr>
<td>65 V eGaN FET</td>
<td>Q(_{\text{GS2}})</td>
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<tr>
<td>30 V BGA MOSFETS</td>
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</table>

**Diagram:**
- **Q\(_{\text{GS2}}\)** in blue for 30 V BGA MOSFETS
- **Q\(_{\text{GD}}\)** in red for 100 V eGaN FET
- **Q\(_{\text{GD}}\)** in red for Si8808DB
dv/dt Turn-on Immunity

![Diagram showing Gate Charge vs. V_G - Gate Voltage and Q_G - Gate Charge]

- $Q_{GS1} > Q_{GD}$
- Id = 1A
- Vd = 20V
- 20V, 40V
- EPC8004 eGaN FET
Maximizing Device Performance
Common Source Inductance

\[ P_{TCR} \propto \frac{V_{IN} \cdot I_{ON} \cdot Q_{GS2}}{2 \cdot \bar{I}_G} \]

\[ P_{TVF} \propto \frac{V_{IN} \cdot I_{ON} \cdot Q_{GD}}{2 \cdot I_G} \]
Packaging Evolution

Device Loss Breakdown

- **Power Loss (W)**
  - **SO-8**: 18% Package, 73% Die
  - **LFPAK**: 27% Package, 47% Die
  - **DirectFET**: 53% Package
  - **LGA**: 47% Package

- **V_{IN}** = 12V
- **V_{OUT}** = 1.2V
- **I_{OUT}** = 20A
- **F_S** = 1MHz

Efficiency (%)

- **SO-8**
- **LFPAK**
- **DirectFET**
- **LGA**

Switching Frequency (MHz)

- **0.5**
- **1**
- **1.5**
- **2**
- **2.5**
- **3**
- **3.5**
Converter Parasitics

$L_S$: Common Source Inductance

$L_{Loop}$: High Frequency Power Loop Inductance

$V_{IN}=12$ V, $V_{OUT}=1.2$ V, $f_{sw}=1$ MHz, $I_{OUT}=20$ A
Low Parasitic Layout

Top Layer

Vias to next layer

To BUS caps

Supply

Switch node

Gate Current orthogonal to drain current

Top Gate

Bottom Gate

Vias to next layer

Ground
Low Parasitic Layout

First Inner Layer

To gate drive

Optimum gate loop return

Optimum power loop return

Source

Drain

Sub

Sub

S

S

Source
EPC8000 Series Improvements

- Reduce active area for lower power / higher frequency operation
- Minimize Hard Switching Figure of Merit
- Complete dv/dt turn-on immunity
- Separate gate and power loops
- Minimize power loop inductance
- Minimize gate loop inductance
Experimental Results
ET Prototype Board

2X, SO-8 footprint

Bus caps
EPC80XX
LM5113
EPC80XX
20 $V_{BUS}$, 10 MHz, 4 A Switching

No measurable overshoot

Rise time ~500 ps
Fall time ~400 ps

10 ns/div and 5 V/div, 1 GHz 100:1, 1 pF TM probe
Near 90% @ >4:1 step down ratio
42 $V_{IN}$ at 1 $A_{OUT}$

- No measurable overshoot
- $dv/dt$ interval
- $75V/ns$ slew rate
- $di/dt$ interval
- Rise time $\sim 1.0$ ns
- Total switching time $\sim 1.2$ ns

2 ns/div and 10 V/div, 1 GHz 100:1, 1pF TM probe

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42 \text{V}_\text{IN}, 20 \text{V}_\text{OUT}, 10 \text{MHz}

![Graph showing efficiency, power loss, and losses components for EPC8005 at different output powers.](image-url)
Current Limitations
Parasitic Losses

- Reverse recovery charge
- Bootstrap diode
- Switch-node rising edge
- Level Shift
- IC capacitance
- Half-bridge driver
No-load Switching

10 MHz switching, no load, large dead-time

10 V/div, 100 mA/div, 10 ns/div

Expected commutation based on eGaN FET $C_{OSS}$

Initially slow rising edge

Actual voltage commutation slopes are different, even though currents are the same
Loss Breakdown

10 MHz switching, no load, large dead-time  
10 V/div, 100 mA/div, 10 ns/div

- Inductor current
- Switch-node voltage
- Bootstrap Q

Actual commutation based on total $C_{OSS}$ – including IC capacitance
Conduction Switching

42 $V_{\text{IN}}$, 20 $V_{\text{OUT}}$, 10 MHz

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Efficiency

Power Loss (W)

Output power (W)

Conduction

Switching

$C_{\text{OSS}}$

Gate driver and Magnetics

$C_{\text{OSS}}$ Gate Driver

$Q_{\text{RR}}$ Bootstrap diode

65%

70%

75%

80%

85%

90%
eGaN FET Limited Efficiency

Calculated efficiency improvement

Reduction in $C_{\text{driver}}$ and $Q_{\text{BootRR}}$ losses

Efficiency vs. Output power (W) graph showing calculated efficiency improvement and reduction in driver and BootRR losses.
Summary

- New devices enable higher switching frequencies
- Switching 42 V, 40 W at 10 MHz at 89% possible.
- Driver parasitics limit performance – light load losses can be cut in half, and full load losses can be reduced by 25%
Thank you!

Questions?
The end of the road for silicon.....
is the beginning of the eGaN FET journey!