WSC: GaN-based Power Supplies and Power Supply Modulators for Efficient Powering of RF PAs

M.A. de Rooij, J.T. Strydom, S. Colino
Agenda

- Background to eGaN FETs
- EPC8000 Series Parts
- Envelope Tracking
- Experimental Results
- Limiting Factors
- Summary
Why Gallium Nitride?
eGaN FETs are LGA

Land Grid Array
Solder bump under die
Flip Chip Assembly
Cross Section of an eGaN FET
Threshold vs. Temperature

Normalized Threshold Voltage vs. Junction Temperature (°C)

- eGaN FET
- MOSFET A

Temperature range: -50°C to 150°C

Normalized Threshold Voltage range: 0.6 to 1.2
eGaN® FETs vs. MOSFETs
Why Envelope Tracking?

66% Compound annual growth rate

Source: Cisco VNI Mobile Data Traffic Forecast

Exabytes per Month

2012 2013 2014 2015 2016 2017

Reference: Nujira.com website

Peak power
Average power

3.5G (HSUPA)
6.5 dB PAPR (~5:1)

3G (W-CDMA)
3.5 dB PAPR (~2:1)

4G (LTE / OFDM)
8.5 dB PAPR (~7:1)

Same average

Source: Cisco VNI Mobile
Data Traffic Forecast
Effect of PAPR

- PAPR = 0dB: Peak efficiency up to 65%
- Increasing PAPR:
  - Average efficiency only 25%
  - Output Probability
Effect of Envelope Tracking

Average efficiency
> 50 % (incl. ET)

Only 1/3 the losses

PA Efficiency (%)

Output Power (dBm)

Average Power

Output Probability

Envelope Tracking
RFPA Standards*

<table>
<thead>
<tr>
<th>Standard</th>
<th>Launched</th>
<th>Typ. Carrier BW (MHz)</th>
<th>Typ. Spectral Efficiency (bps/Hz)</th>
<th>Approx. PAPR(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2G cellular</td>
<td>1991</td>
<td>0.2</td>
<td>0.17</td>
<td>0.0</td>
</tr>
<tr>
<td>2.75G cellular</td>
<td>2003</td>
<td>0.2</td>
<td>0.33</td>
<td>3.5</td>
</tr>
<tr>
<td>3G cellular</td>
<td>2001</td>
<td>5</td>
<td>0.51</td>
<td>7.0</td>
</tr>
<tr>
<td>Digital TV</td>
<td>1997</td>
<td>8</td>
<td>0.55</td>
<td>8.0</td>
</tr>
<tr>
<td>DVB-T</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Wi-Fi</td>
<td>2003</td>
<td>20</td>
<td>0.90</td>
<td>9.0</td>
</tr>
<tr>
<td>WiMAX</td>
<td>2004</td>
<td>20</td>
<td>1.20</td>
<td>8.5</td>
</tr>
<tr>
<td>Wi-Fi</td>
<td>2007</td>
<td>20</td>
<td>2.40</td>
<td>9.0</td>
</tr>
<tr>
<td>3.5G cellular</td>
<td>2007</td>
<td>5</td>
<td>2.88</td>
<td>8.0</td>
</tr>
<tr>
<td>HSDPA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.9G cellular</td>
<td>2009</td>
<td>20</td>
<td>8.00</td>
<td>10.0</td>
</tr>
<tr>
<td>LTE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Up to 20 MHz Carrier bandwidth required
- Required ET supply BW about 5x higher than carrier BW

*Ref: www.open-et.org website
Envelope Tracking Supply

- ET power supply topologies vary
  - Open loop boost – full BW required
  - Closed loop linear-assisted Buck*

*B. Yousefzadeh, et. Al, Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers, ISCAS 2005
Initial Efficiency Results

10x potential bandwidth require 2.5x more phases and 2x losses

- EPC2001
- EPC2007

**Graph Details:**
- **Y-axis:** Efficiency (%)
- **X-axis:** Output Power (W)
- **Legend:**
  - 4 MHz Efficiency
  - 1 MHz Efficiency
  - 4 MHz Losses
  - 1 MHz Losses

**Additional Notes:**
- 90% - 98% Efficiency range
- 0 - 350 W Output Power range
- Power loss (W) scale from 0 to 16
Loss Breakdown

1 MHz EPC9002
Future die size optimization possible

4 MHz EPC9006
Lower Voltage ET Results*


24 $V_{\text{IN}}$ to 12 $V_{\text{OUT}}$ Buck

20 pp to 30 pp improvement!
Higher Frequency Lower Power Devices

- Improve Device Bandwidth
- Reduce device size
- Minimize $Q_{GD}$ / HS-FOM
- Complete dv/dt immunity
- Minimize gate loop inductance
- Minimize power loop inductance
- Separate gate and power loops
# Ultra High Frequency eGaN® FETs

<table>
<thead>
<tr>
<th>EPC Part No.</th>
<th>BV (V)</th>
<th>Max. ( R_{DS(ON)} ) (mΩ)</th>
<th>Min. Peak Id (A) (Pulsed, 25 °C, ( T_{pulse} = 300 \mu s ))</th>
<th>Typical Charge (pC)</th>
<th>Typical Capacitance (pF) (V(<em>{DS} = 20) V; V(</em>{GS} = 0) V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC8004</td>
<td>40</td>
<td>125</td>
<td>7.5</td>
<td>358</td>
<td>31</td>
</tr>
<tr>
<td>EPC8007</td>
<td>40</td>
<td>160</td>
<td>6</td>
<td>302</td>
<td>25</td>
</tr>
<tr>
<td>EPC8008</td>
<td>40</td>
<td>325</td>
<td>2.9</td>
<td>177</td>
<td>12</td>
</tr>
<tr>
<td>EPC8009</td>
<td>65</td>
<td>138</td>
<td>7.5</td>
<td>380</td>
<td>36</td>
</tr>
<tr>
<td>EPC8005</td>
<td>65</td>
<td>275</td>
<td>3.8</td>
<td>218</td>
<td>18</td>
</tr>
<tr>
<td>EPC8002</td>
<td>65</td>
<td>530</td>
<td>2</td>
<td>141</td>
<td>9.4</td>
</tr>
<tr>
<td>EPC8003</td>
<td>100</td>
<td>300</td>
<td>5</td>
<td>315</td>
<td>34</td>
</tr>
<tr>
<td>EPC8010</td>
<td>100</td>
<td>160</td>
<td>7.5</td>
<td>354</td>
<td>32</td>
</tr>
</tbody>
</table>

* Preliminary Data – Subject to Change without Notice

- Typical Charge (Q\(_G\), Q\(_{GD}\), Q\(_{GS}\), Q\(_{OSS}\), Q\(_{RR}\))
- Typical Capacitance (C\(_{ISS}\), C\(_{OSS}\), C\(_{RSS}\))

Dimensions: 2.05 mm x 0.85 mm
Small Signal Performance

Designed for switching Performance

Bias: 30 V, 500 mA

Gmax

Amplitude [dB]

Frequency [MHz]

S11 - Gate Reflection
S22 - Drain Reflection
EPC8009

Bias: 30 V, 500 mA

RFIC2014, Tampa Bay, 1-3 June, 2014
Large Signal Performance

**Graph:**
- **Y-axis:** Gain [dB]
- **X-axis:** Efficiency [%]
- **Output Power [dBm]:**
  - Linear scale from 26 to 42 dBm

**Graph Data:**
- **Efficiency:**
  - 1 dB Compression Point
  - EPC8009

**Description:**
- **500 MHz, Class A, Bias = 30 V, 500 mA**
Die Size - Gate Charge

- EPC8004 eGaN FET
- EPC2014
# Hard Switching FOM

<table>
<thead>
<tr>
<th></th>
<th>230mΩ</th>
<th>24mΩ</th>
<th>90mΩ</th>
<th>200mΩ</th>
<th>71mΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>65 V eGaN FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 V eGaN FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **EPC8005**
- **EPC2007**
- **CSD17381F4**
- **CSD17483F4**
- **Si8808DB**

**Q\(_{GS2}\)**

**Q\(_{GD}\)**

<table>
<thead>
<tr>
<th></th>
<th>30 V BGA MOSFETS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q(_{GS2})</td>
<td>Q(_{GD})</td>
</tr>
</tbody>
</table>

**Q\(_{GD}\)**
dv/dt Immunity

![Graph showing Gate Charge vs. qG - Gate Charge (pC)]

- EPC8004 eGaN FET
- QGD
- QGS1
Low Parasitic Layout

Top Layer

Vias to next layer

To BUS caps

Supply

Switch node

Gate Current orthogonal to drain current

Vias to next layer

Bottom Gate

Ground
Low Parasitic Layout

First InnerLayer

To gate drive

Optimum gate loop return

Optimum power loop return

Gate

Return

Drain

Source

Sub

To gate drive

Optimum gate loop return

Gate

Return

Drain

Source

Sub
ET Prototype Board

- EPC90
- V DEVELOPMENTBOARD
- eGaN® FET © EPC 2013
- J1 C4
- C1 C10
- U3 U2 Q1
- C1 C12 Q1
- J3 J5 J6
- UN SW
- P1 R12 R22
- P2 R4 R5
- R1 R2
- TP1 TP2
- HS1 GND
- C7

Components:
- Bus caps
- EPC8010
- LM5113
- SO-8 footprint
15 $V_{IN}$ to 3.3 $V_{OUT}$, 10 MHz

Efficiency

Output Power (W)

Power Loss (W)

EPC8007
20 $V_{IN}$ at 4 $A_{OUT}$

No measurable overshoot

Rise time $\approx 500$ ps
Fall time $\approx 400$ ps

10 ns/div and 5 V/div
42 $V_{IN}$ to 20 $V_{OUT}$, 10 MHz

Efficiency

Power Loss (W)

Output power (W)

EPC8005
42 $V_{IN}$ at 1 $A_{OUT}$

- No measurable overshoot
- $dv/dt$ interval
- $75V/\text{ns}$ slew rate
- $di/dt$ interval
- Rise time $\sim 1.0 \text{ ns}$
- Total switching time $\sim 1.2 \text{ ns}$

2 ns/div and 10 V/div, 1 GHz 100:1 1 pF TM probe
42 $V_{IN}$, 20 $V_{OUT}$, 10 MHz
Loss Investigation

5 MHz switching, no load, large dead-time

10V/div, 200mA/div, 10ns/div

Expected commutation based on eGaN FET $C_{OSS}$

Actual voltage commutation slopes are different, even though currents are the same
No-load Switching

10 MHz switching, no load, large dead-time

Expected commutation based on eGaN FET $C_{OSS}$

Initially slow rising edge

Actual voltage commutation slopes are different, even though currents are the same

Rise(2): 13.6ns  Fall(2): 7.1ns  Freq(2): No edges  Max(2): 42.8V
Parasitic Losses

Level Shift

Reverse recovery charge

Bootstrap diode

IC capacitance

Switch-node rising edge

V_{DD}

LM5113 half-bridge driver
Loss Breakdown

10 MHz switching, no load, large dead-time

10V/div, 100mA/div, 10ns/div

Bootstrap Q\textsubscript{RR}

Actual commutation based on total C\textsubscript{OSS} – including IC capacitance

Inductor current

Switch-node voltage

Rise(2): 13.6ns  Fall(2): 7.1ns  Freq(2): No edges  Max(2): 42.8V
42 $V_{IN}$, 20 $V_{OUT}$, 10 MHz

Efficiency vs. Output power (W)

- Conduction
- Switching
- Gate driver and Magnetics
- $C_{OSS}$ Driver
- $Q_{RR}$ Bootstrap diode

Unaccounted losses

Vin, 20 Vout, 10 MHz
eGaN FET Limited Efficiency

Calculated efficiency improvement

Reduction in $C_{\text{Driver}}$, $Q_{\text{BootRR}}$ and driver losses
**Point of Load Buck Converter**

- ~3V overshoot @ 15A out
- ~1.1ns rise time
- Inductor on back to maximize power density
- 28V to 3.3V / 15A @ 1MHz
EPC9107 Efficiency Results

V_{OUT} = 3.3 \, \text{V}, \, f_{SW} = 1 \, \text{MHz}, \, \text{GaN Switch/Synchronous Rect.: EPC2015, Driver LM5113}
Device Summary

- EPC8000 eGaN FETs proven up to 10 MHz
- New devices enable higher switching frequencies
- Switching 42V, 40W at 10MHz at 89% possible
- Driver parasitics limit performance
  - Doubles light load losses
- Gate driver improvements will allow further increase in switching frequency
• EPC8000 eGaN FETs enable High Frequency Power modulation.

• Superior FoM of eGaN FETs allow higher efficiency at higher frequencies.
  • Applicable to 42 V and 28 V DC to DC converters.
  • Enables very low duty cycle conversion

• eGaN FETs reduce energy cost.
The end of the road for silicon.....

is the beginning of the eGaN FET journey!