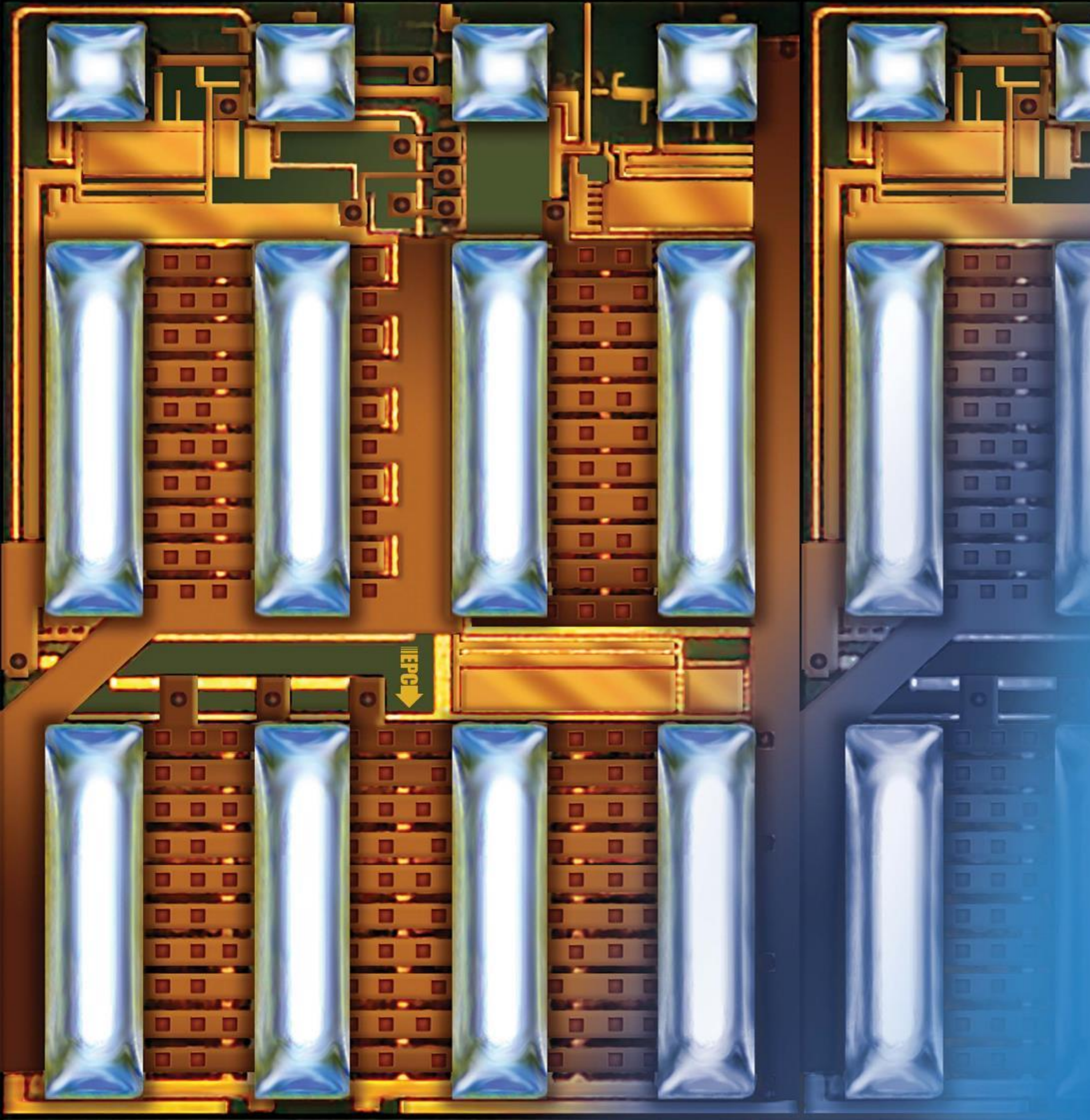


GaN Device Reliability

Shengke Zhang, Ph.D.

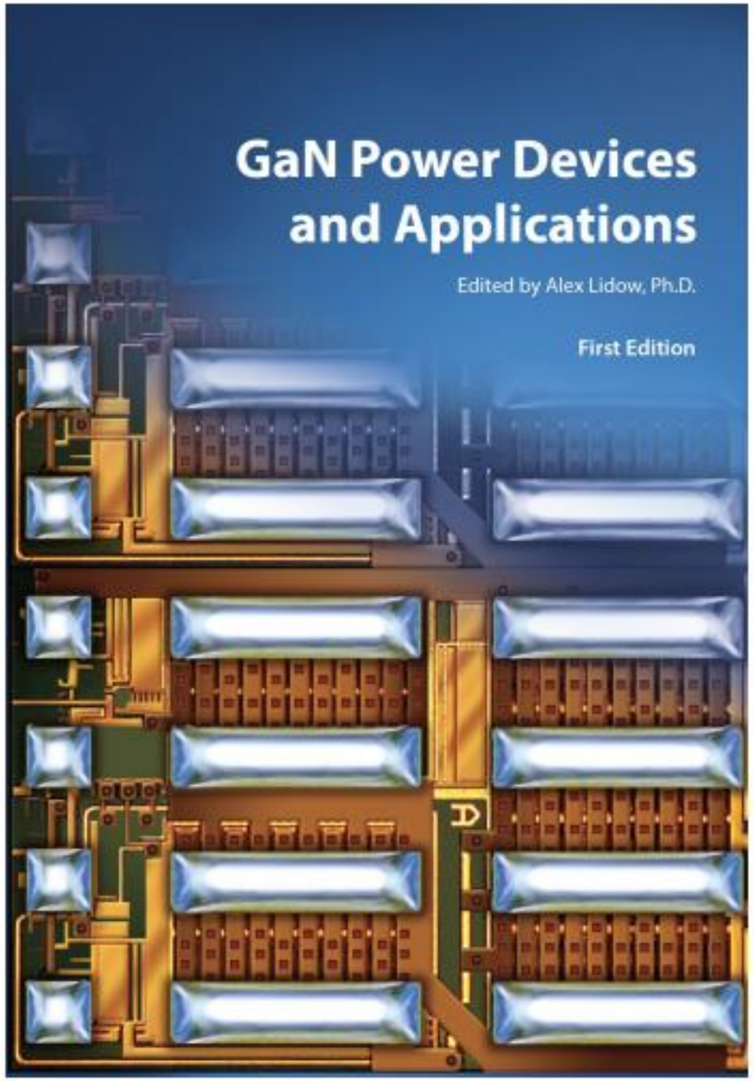
Presented by C.W. Ryu

EPC EFFICIENT POWER CONVERSION

Using Test-to-Fail Methodology to Predict Lifetime of eGaN® Devices in Various Applications

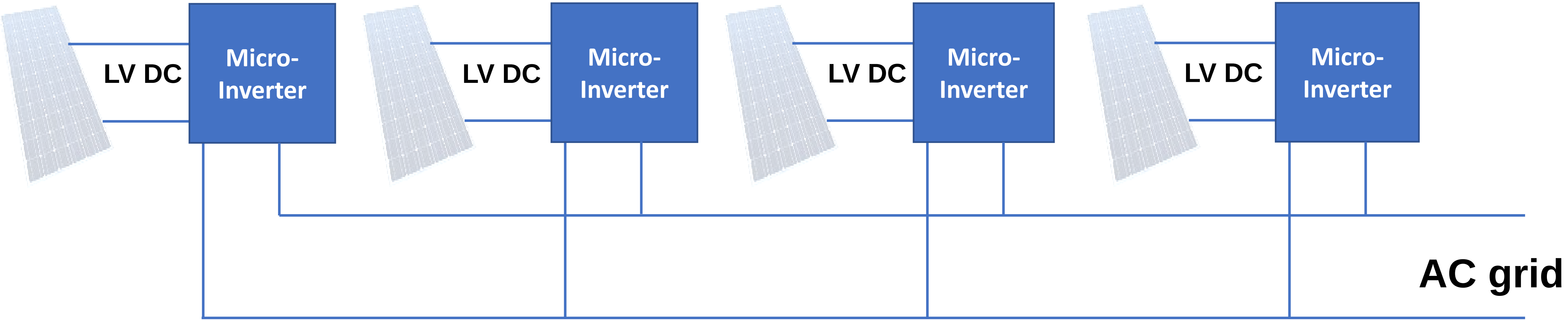
Why Test-to-fail?

Stressor	Device/ Package	Test Method	Instrinsic Failure Mechanism
Voltage	Device	HTGB	Dielectric failure (TDDB)
			Threshold Shift
		HTRB	Threshold Shift
			$R_{DS(on)}$ Shift
		ESD	Dielectric rupture
Current	Device	DC Current (EM)	Electromigration
			Thermomigration
Current + Voltage (Power)	Device	SOA	Thermal Runaway
		Short Circuit	Thermal Runaway
Voltage Rising/Falling	Device	Hard-switching reliability	$R_{DS(on)}$ Shift
Current Rising/Falling	Device	Pulsed Current (Lidar reliability)	None found
Temperature	Package	HTS	None found
Humidity	Package	MSL1	None found
		H3TRB	None found
		AC	None found
		Solderability	Solder corrosion
		uHAST	Dentrite Formation/Corrosion
Mechanical/ Thermo-mechanical	Package	TC	Solder Fatigue
		IOL	Solder Fatigue
		Bending force test	Delamination
		Bending Force Test	Solder Strength
		Bending Force Test	Piezoelectric Effects
		Die shear	Solder Strength
		Package force	Film Cracking



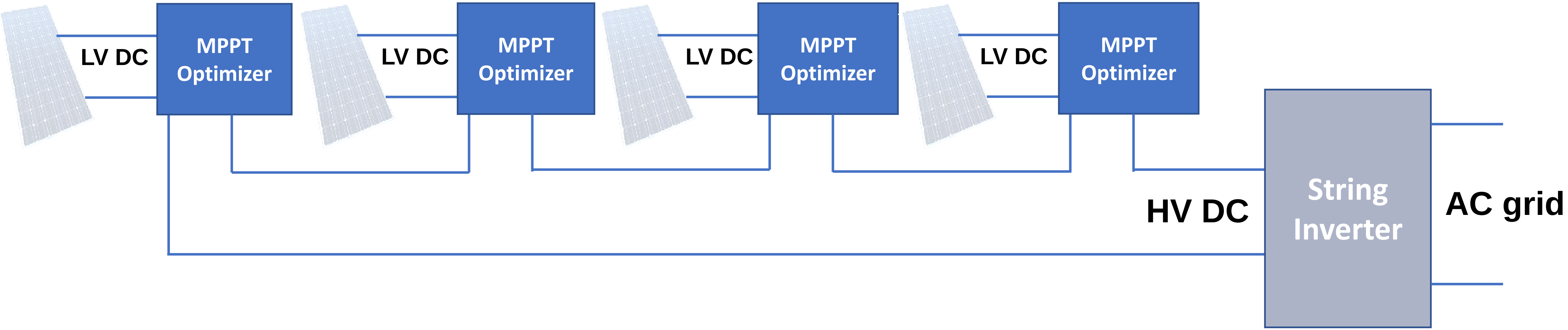
Solar

Popular Topology in Solar: **Micro-Inverter**



EPC's Low voltage eGaN solution (V_{DSMax} < 200V) is a good fit for this solar application

Popular Topology in Solar: **Power Optimizer**



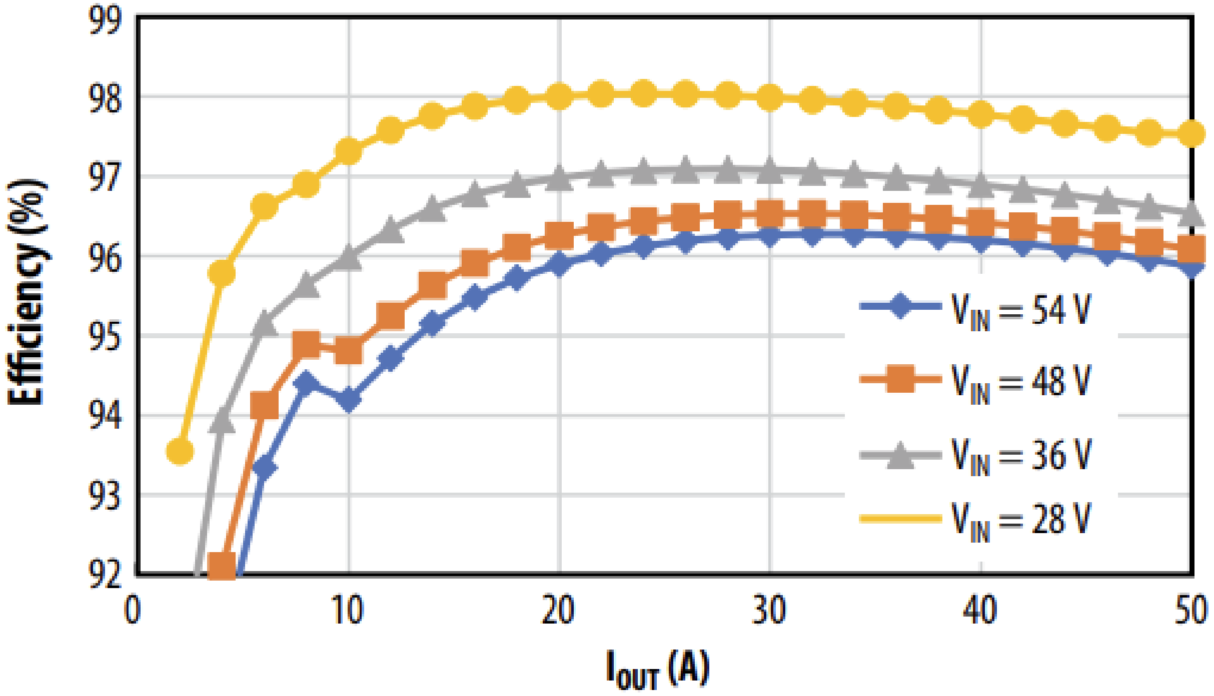
EPC's Low voltage eGaN solution (V_{DSMax} < 200V) is a good fit for this solar application

DC-DC

A Common 48 V–12 V Buck Converter

100 V rated eGaN devices offer superior efficiency

EPC9158: 48 V/54 V to 12 V, Buck Converter
using EPC2218 (100V rated eGaN transistor)



48 V, 1 kW LLC Resonant Converter

Low voltage eGaN devices ($V_{DS,Max \leq 100V}$) offer superior efficiency

EPC9149 board

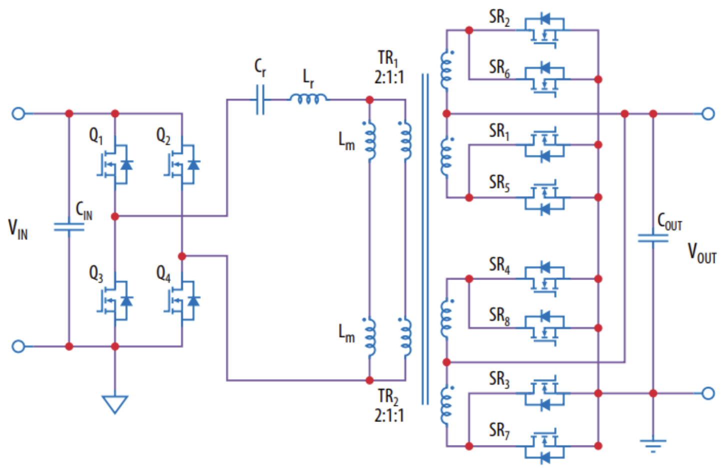
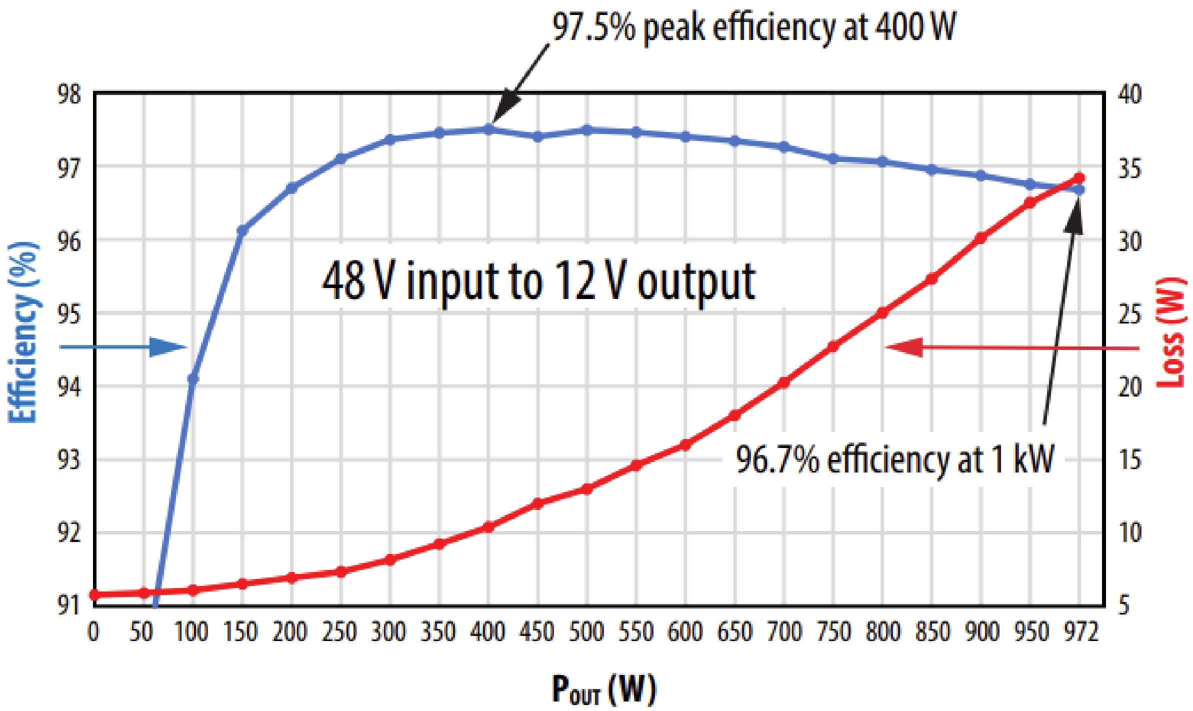


Figure 1. Power architecture schematic of the 48 V, 1 kW LLC resonant converter.

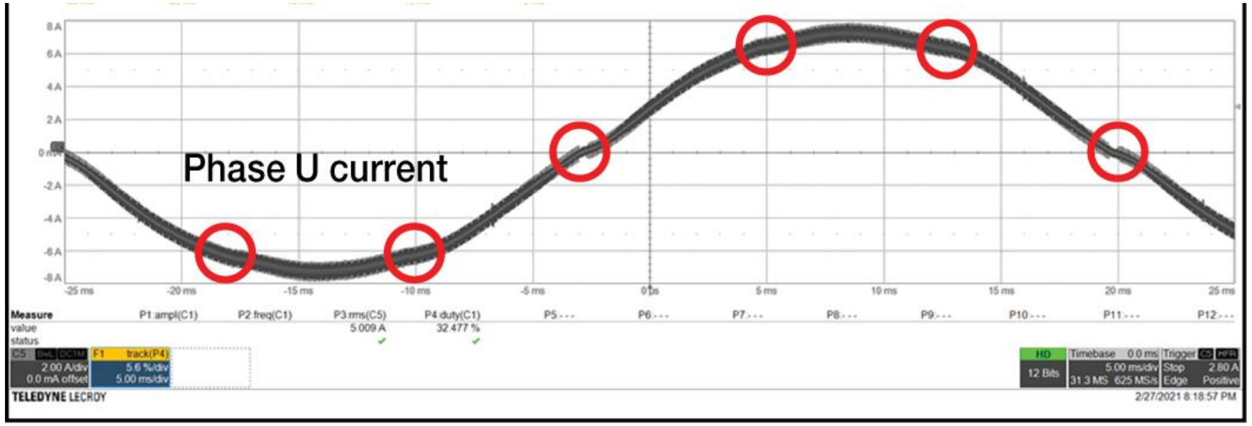


Motor Drives

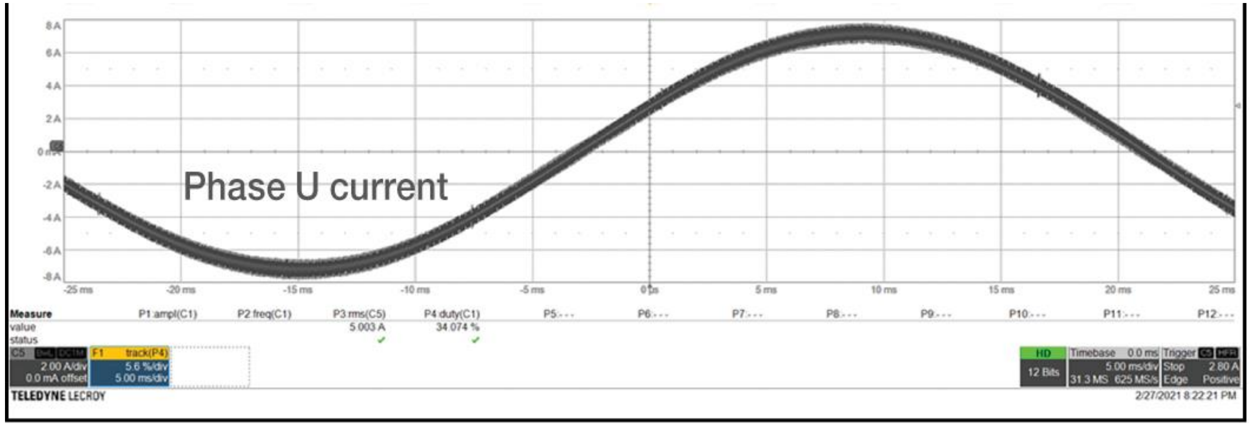
Benefits of GaN in Motor

Eliminating dead time leads to less distortion in phase current, less vibrations, and less acoustic noise.

Si: *500 ns dead time* at 20 kHz



GaN: *14 ns dead time* at 20 kHz

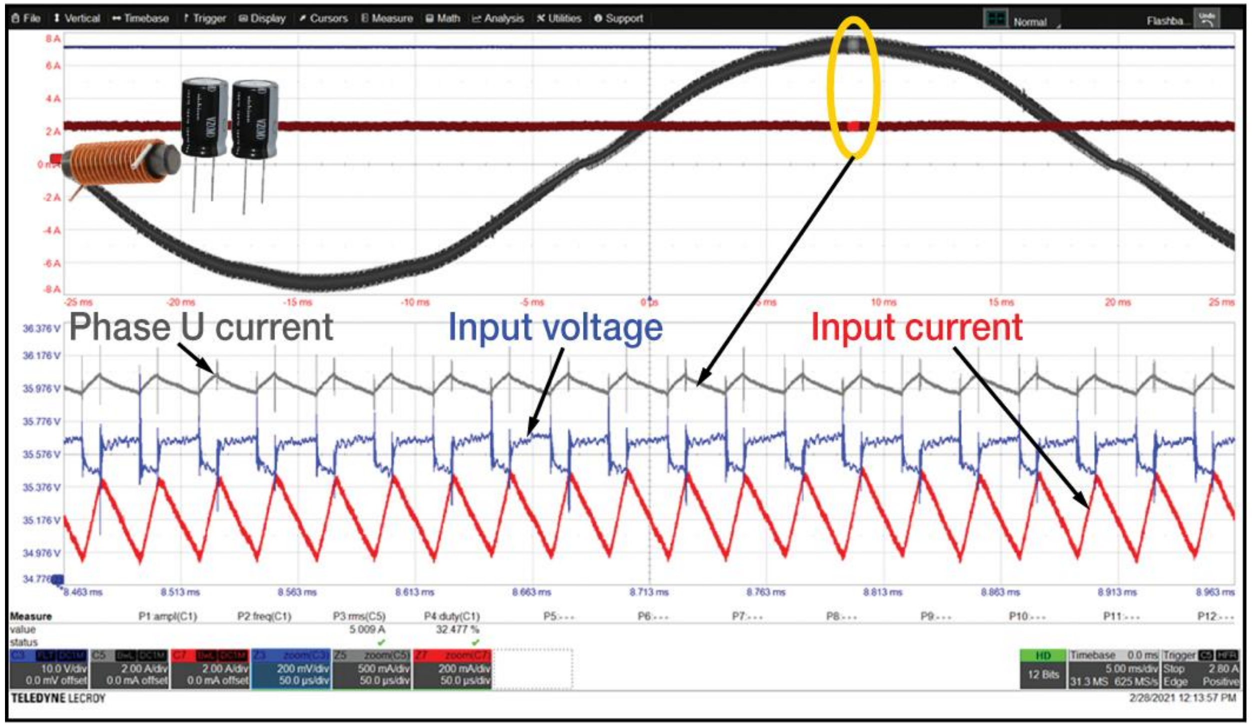


Benefits of GaN in Motor

Increasing PWM frequency reduces both the input current ripple (ΔV_{pp}) and input voltage ripple (ΔI_D) and smoother phase current.

Si: 500 ns dead time at 20 kHz

GaN: 14 ns dead time at 100 kHz



Benefits of GaN in Motor

Setup	Si Inverter 20kHz 500ns dead time 400 RPM 5 Arms	GaN inverter 100kHz 14ns dead time 400 RPM 5 Arms
Input Inductance	2.7 µH	None
Input capacitor	660 µF electrolytic	44 µF ceramic
Pin	121.3 W	113.3 W
Pout	119.6 W	111.3 W
$\eta_{inverter}$	98.5%	98.2%
Speed	42.25 rad/s	41.94 rad/s
Torque	1.876 N	1.940 N
Pmech	79.3 W	81.36 W
η_{motor}	66.3%	73.1%
η total efficiency	65.3%	71.8%

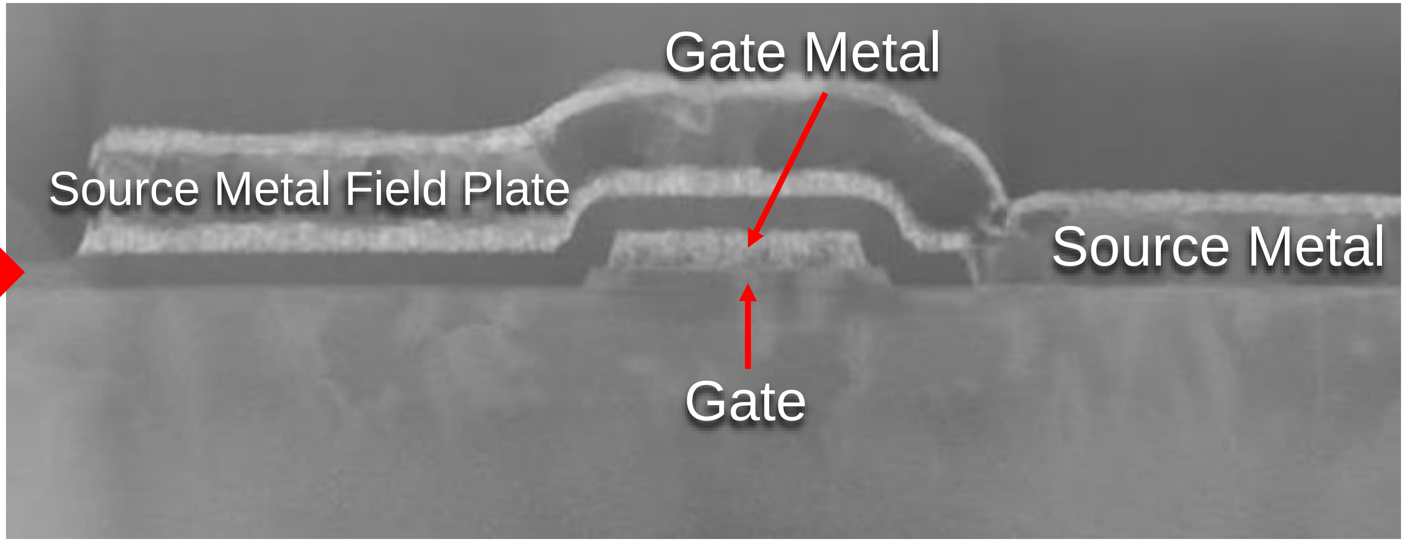
Main Stressors in Various Applications

- Gate Bias (Solar/DC-DC/Motor Drive)
- Drain Bias (Solar/DC-DC/Motor Drive)
- Temperature Cycling (Solar/DC-DC/Motor Drive)
- Short Circuit (Motor Drive)
- Mechanical Stress (Motor Drive)

Gate Bias

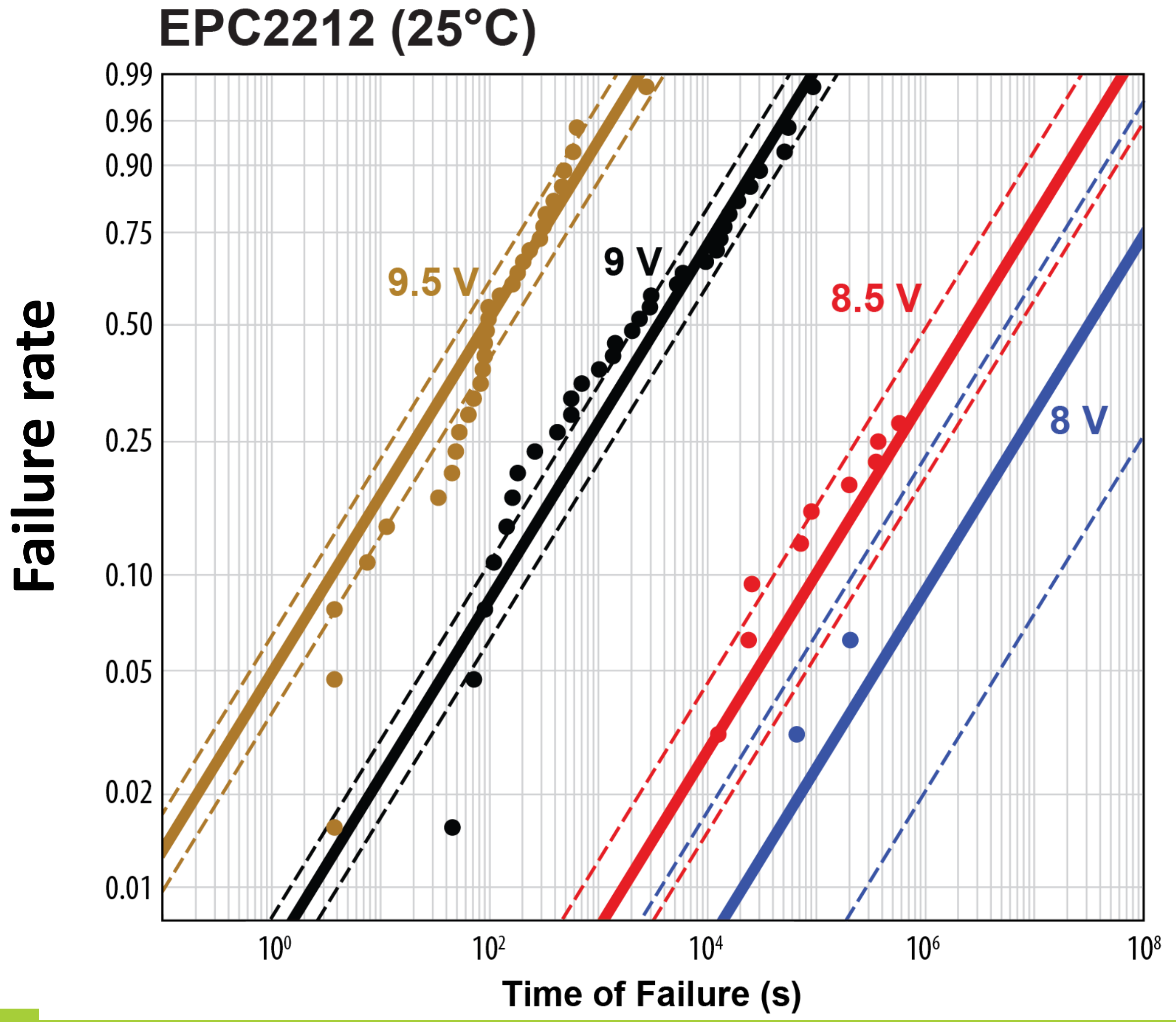
Gate-Source Voltage Stress

Si_3N_4

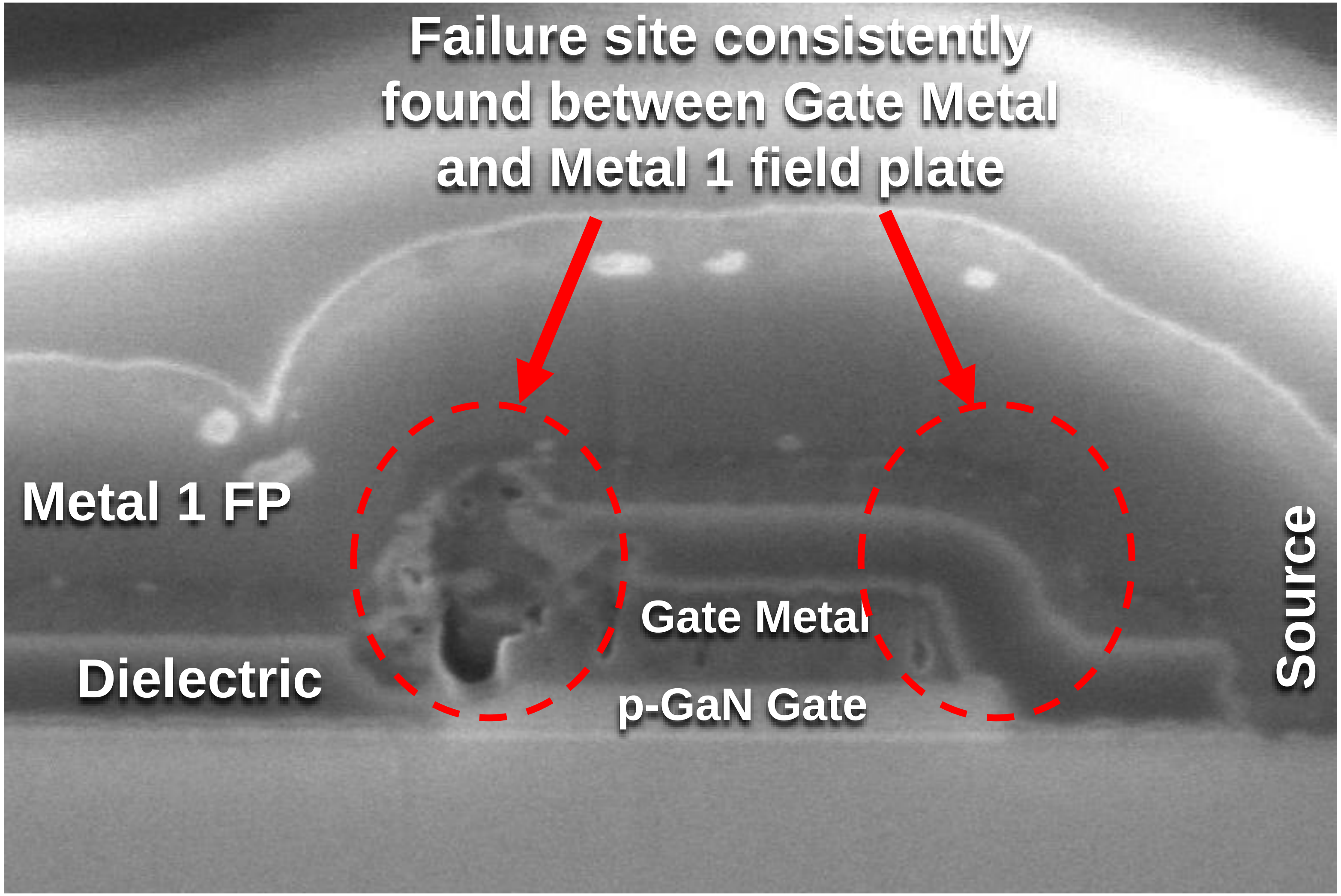


Weibull Analysis of Accelerated Gate Test

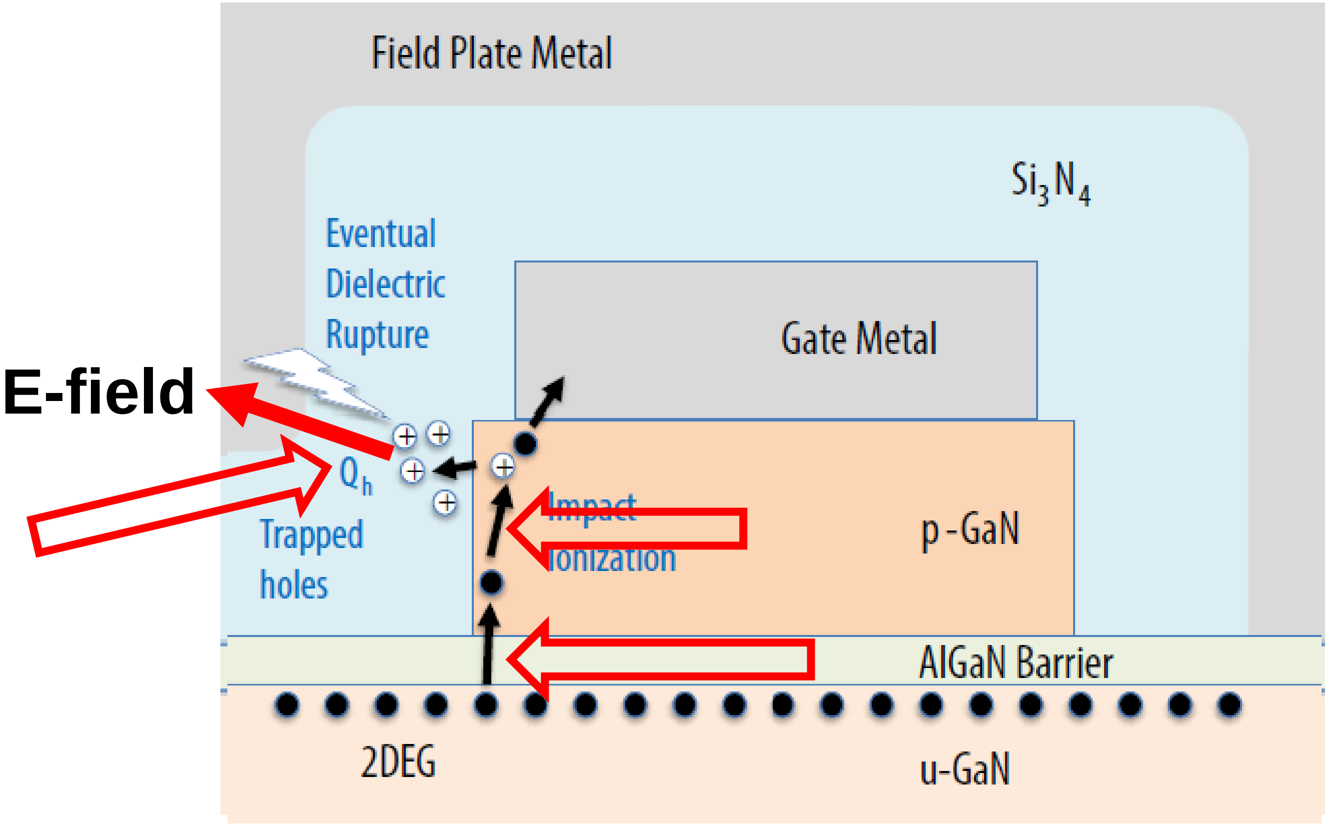
Data Sheet Maximum = 6V V_{GS}



Gate Failures Not in GaN



Gate Wear-out Mechanism: Impact Ionization

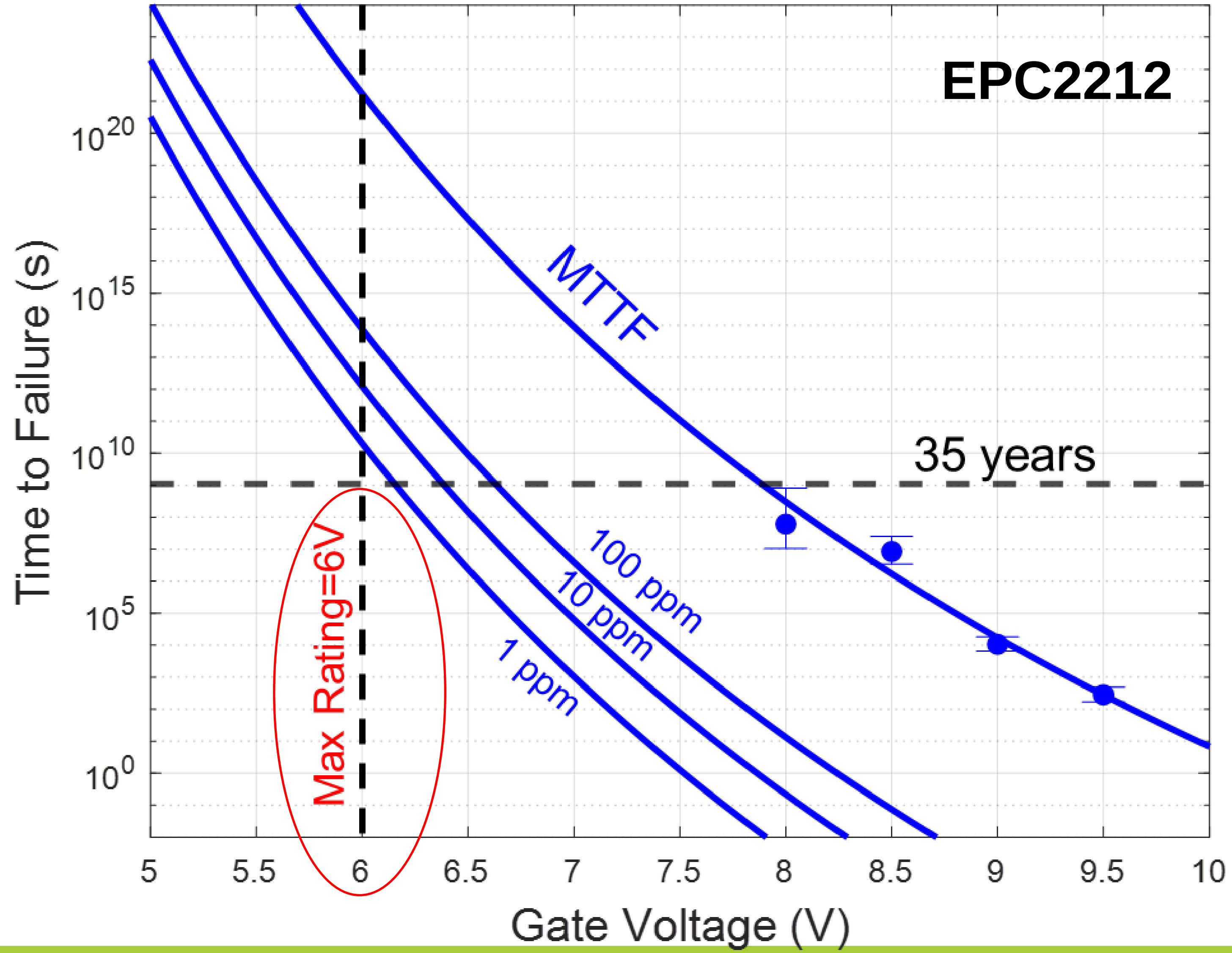


$$MTTF = \frac{Q_C}{G} = \frac{qQ_C}{\alpha_n J_n} = \frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V+V_0}\right)^m\right]$$

$m = 1.9$
$V_0 = 1.0\ V$
$B = 57.0\ V$
$A = 1.7\text{x}10^{-6}\ s$
$c = 6.5\text{x}10^{-3}\ K^{-1}$

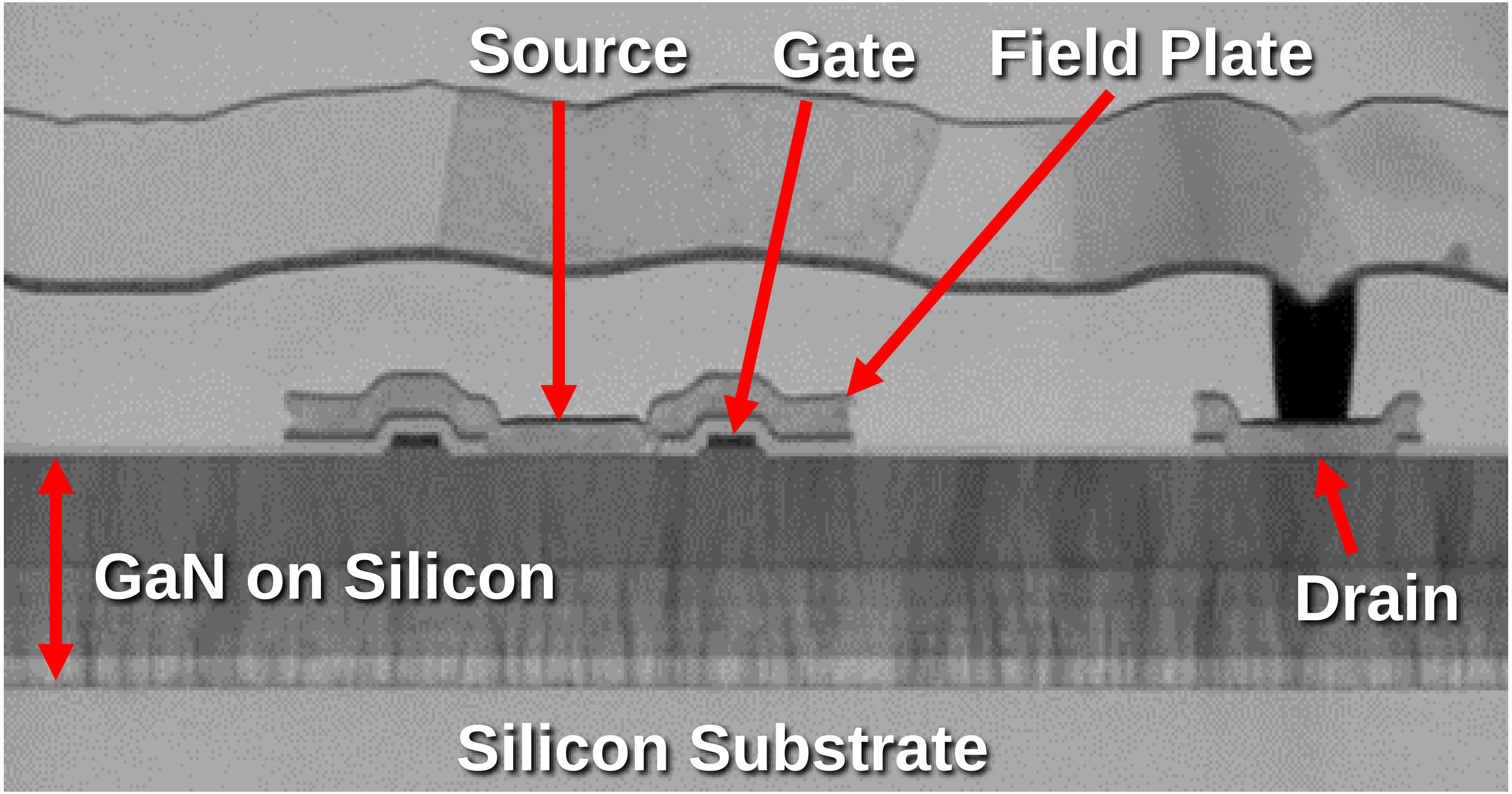
Gate Reliability and Lifetime Projection

<1ppm failure rate projected over more than 35 years of lifetime under continuous V_{GS}=6V DC gate bias (maximum rated V_{GS})

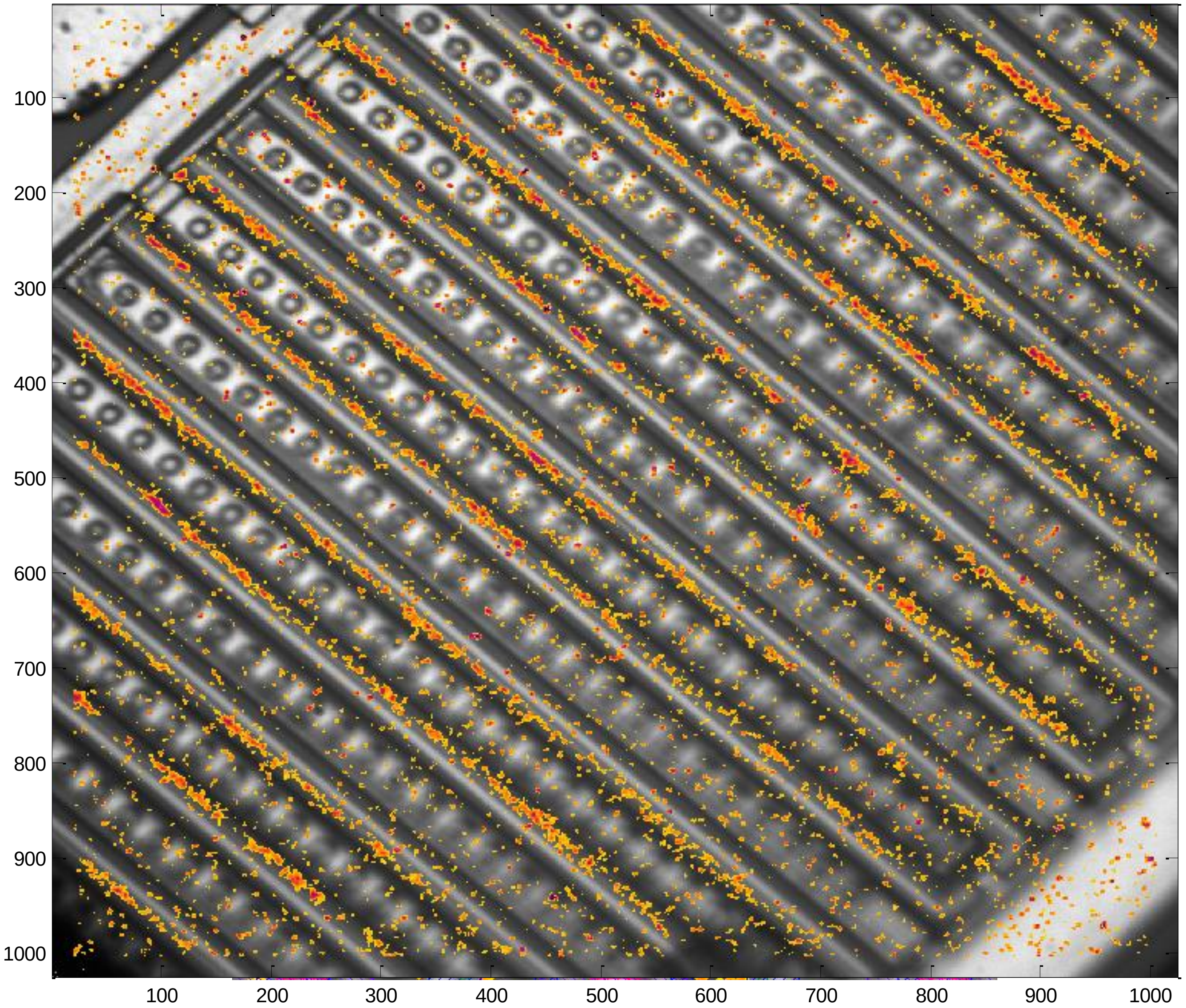


Drain Bias

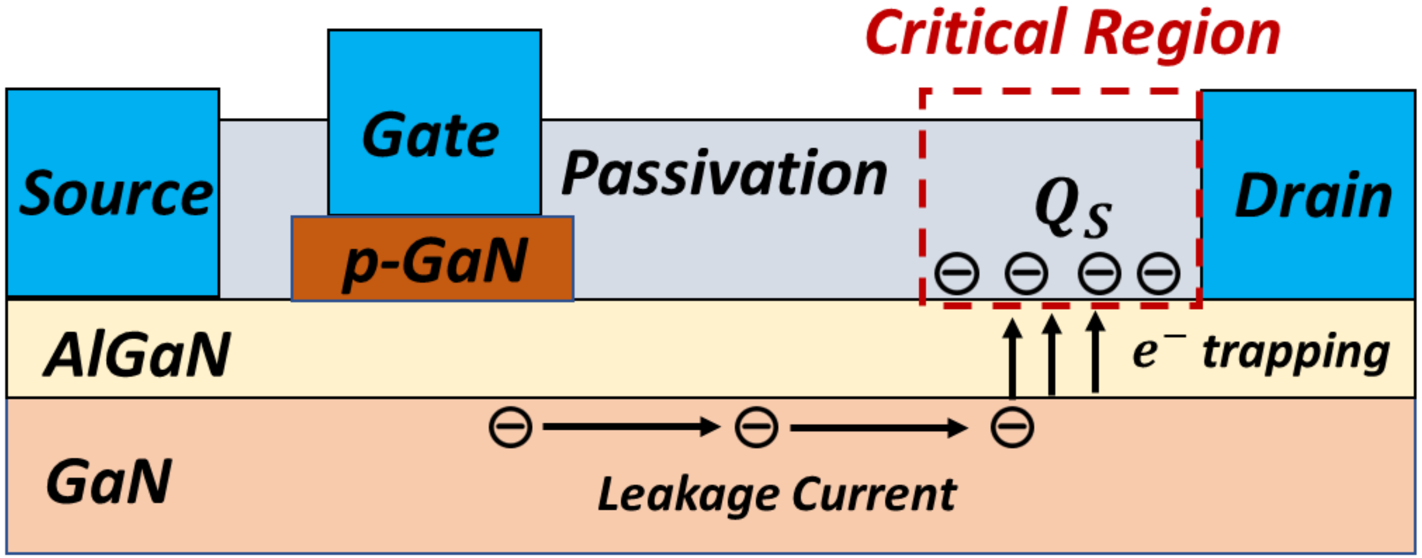
Drain-Source Voltage Stress

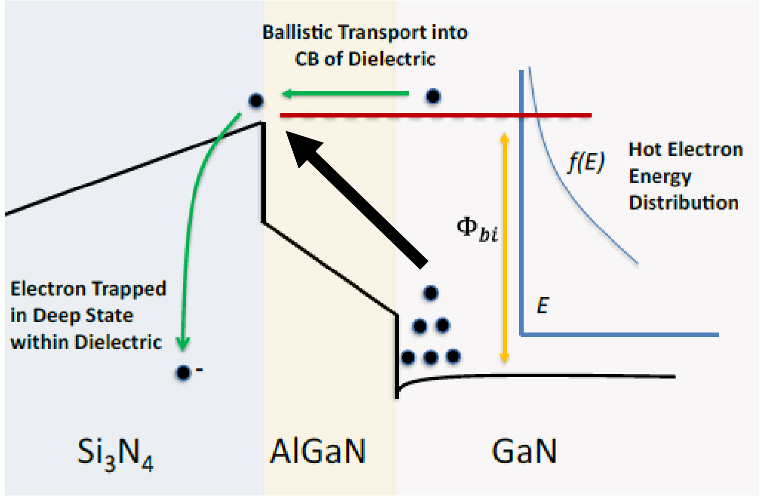


Physics of $R_{DS(on)}$ Shift – Hot Carrier Emission



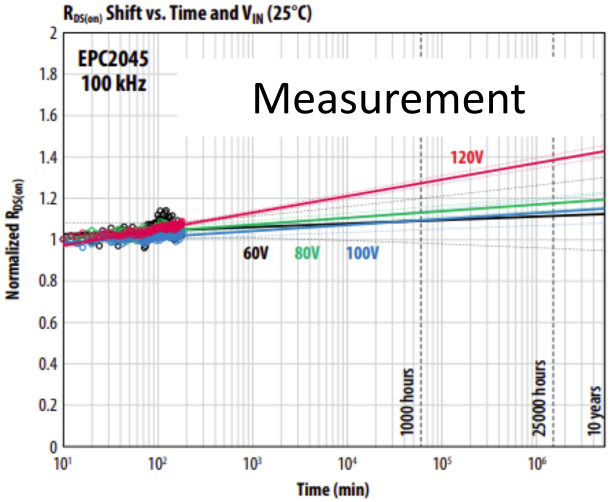
Hot Carrier Trapping Mechanism

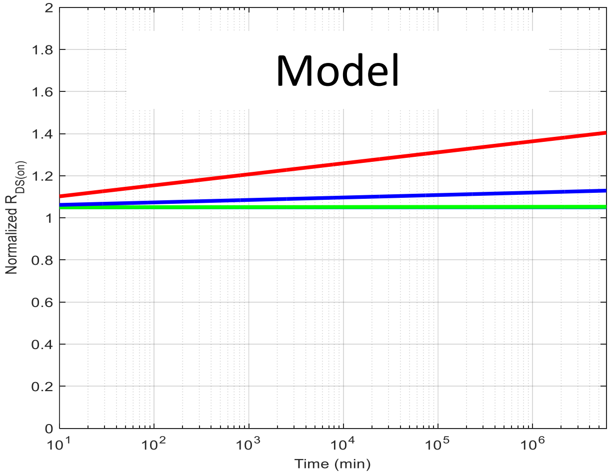


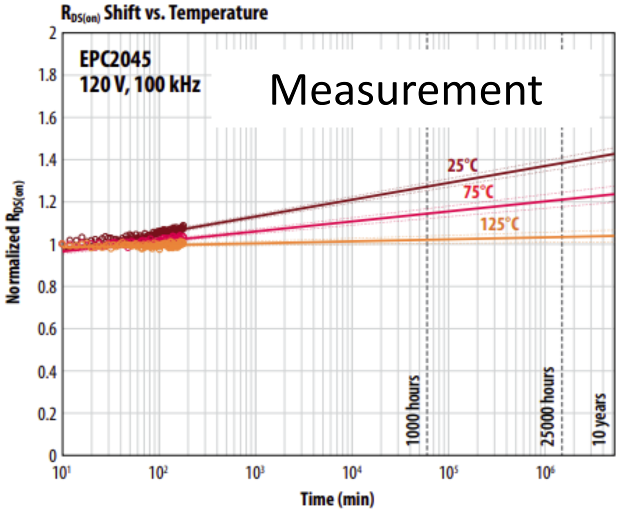


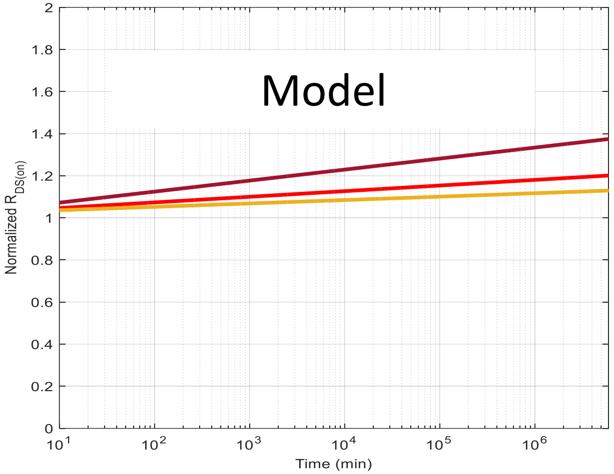
$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF \exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\sqrt{T}\log(t)$$

Model vs Measurement



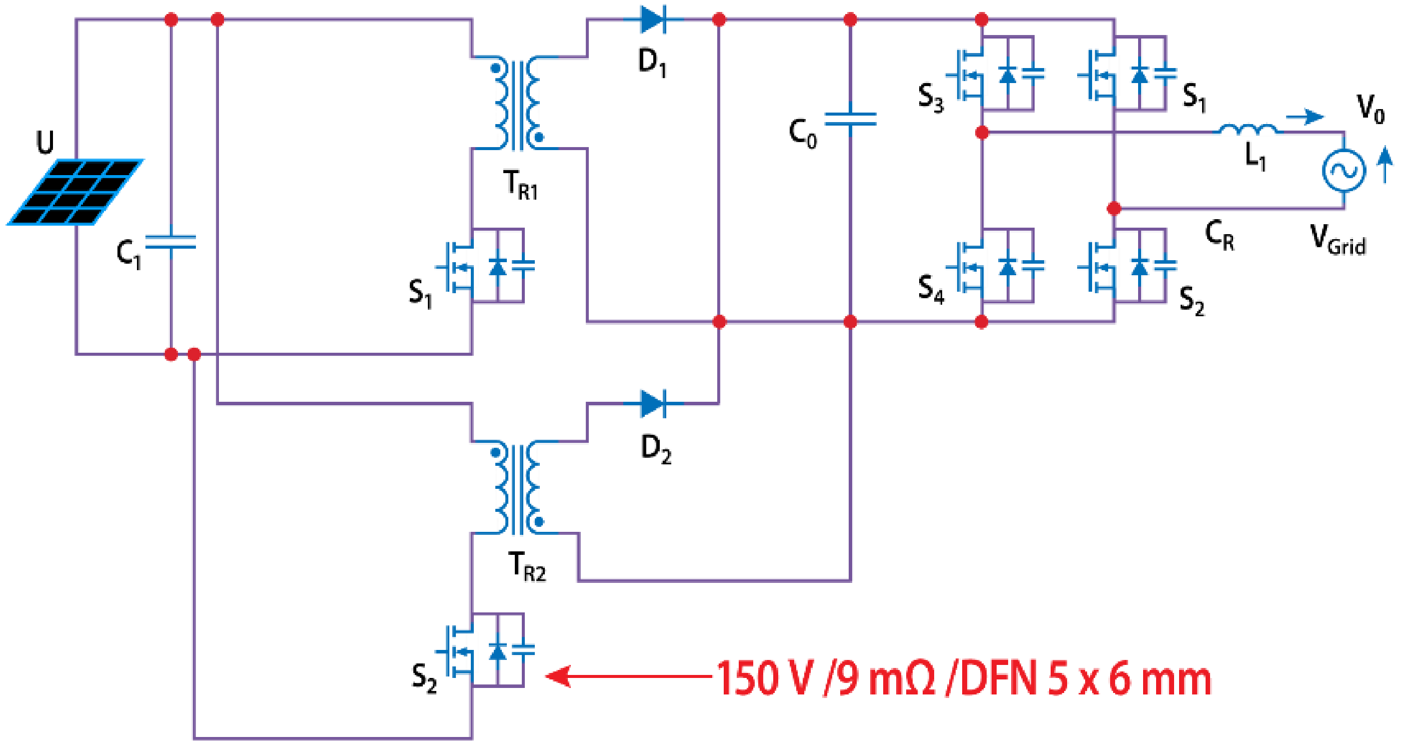






Apply the Model to Project Lifetime for Solar Mission Profile

Microinverter Flyback Topology

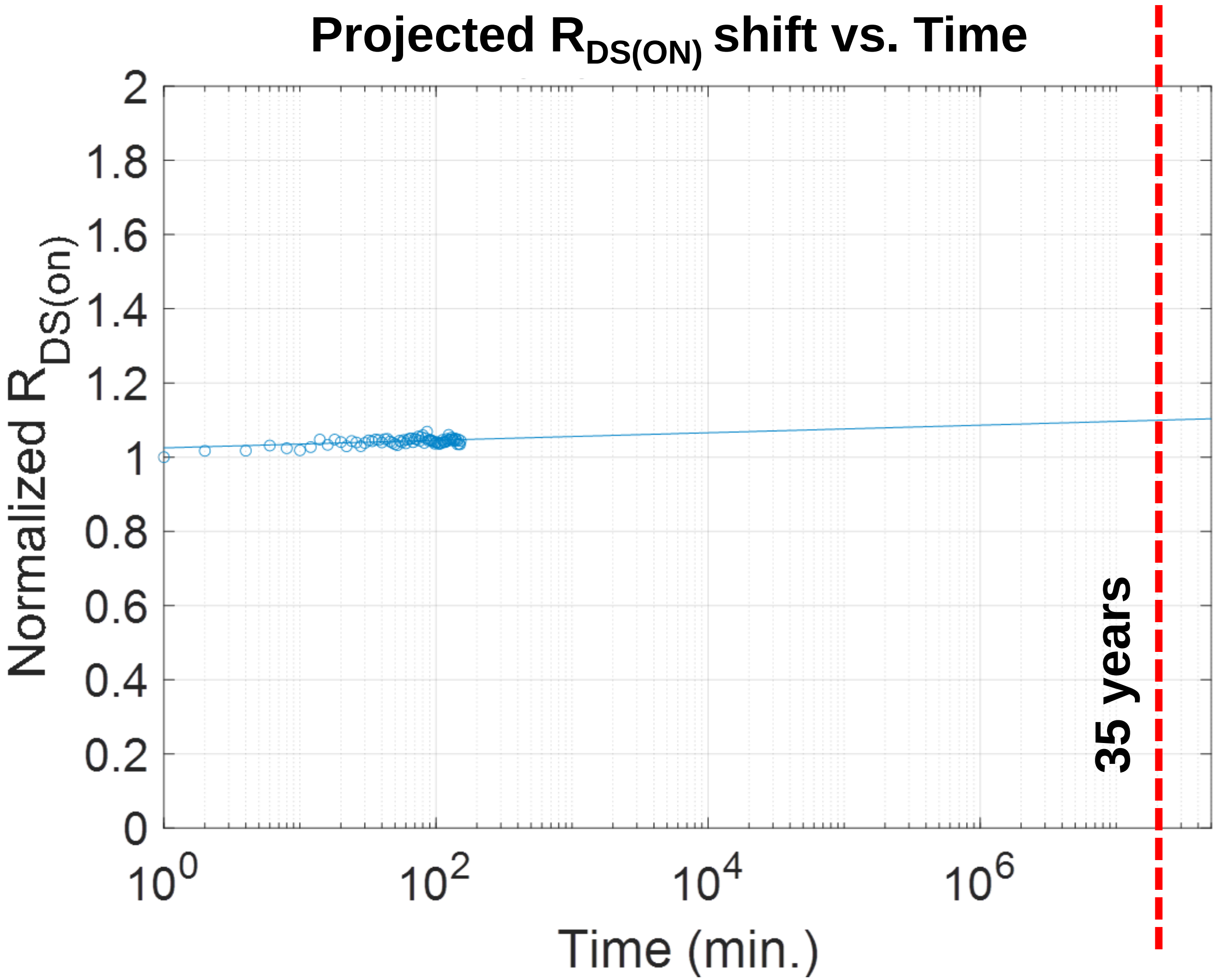


Part Number	Size (mm x mm)	V_{DS} (V)	$R_{DS(on)}$ max (mΩ)	Q_G Typ (nC)	Q_{RR} Typ (nC)
EPC2059	2.8 x 1.4	170	9	5.7	0
EPC2305*	3 x 5 QFN	150	3	21	0
EPC2308*	3 x 5 QFN	150	6	10	0

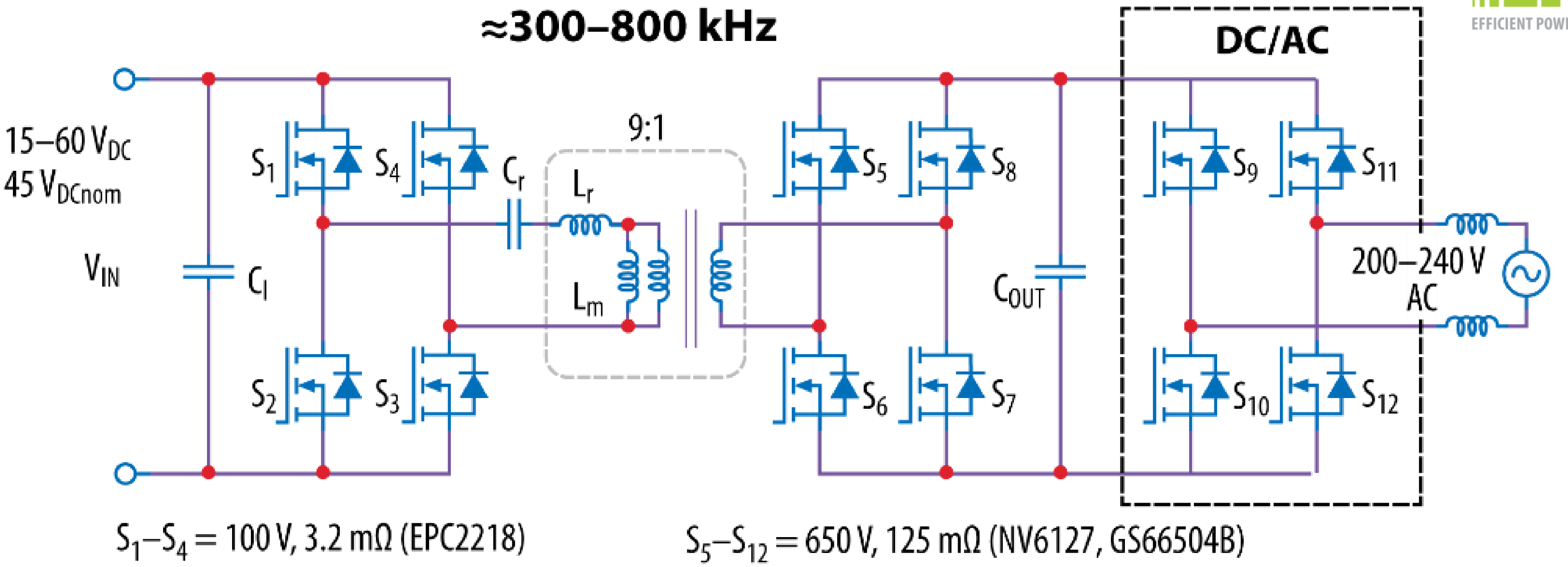
** Sampling*

Drain Bias: Flyback Topology for Solar

- EPC2059 (170V V_{DSMax}) eGaN FET is a good fit for Flyback
- A representative EPC2059 device was tested under continuous hard switching at 100 kHz and 137V (80% V_{DSMax}) with case temperature of 80ºC



Microinverter Full Bridge Topology (Power Optimizer)

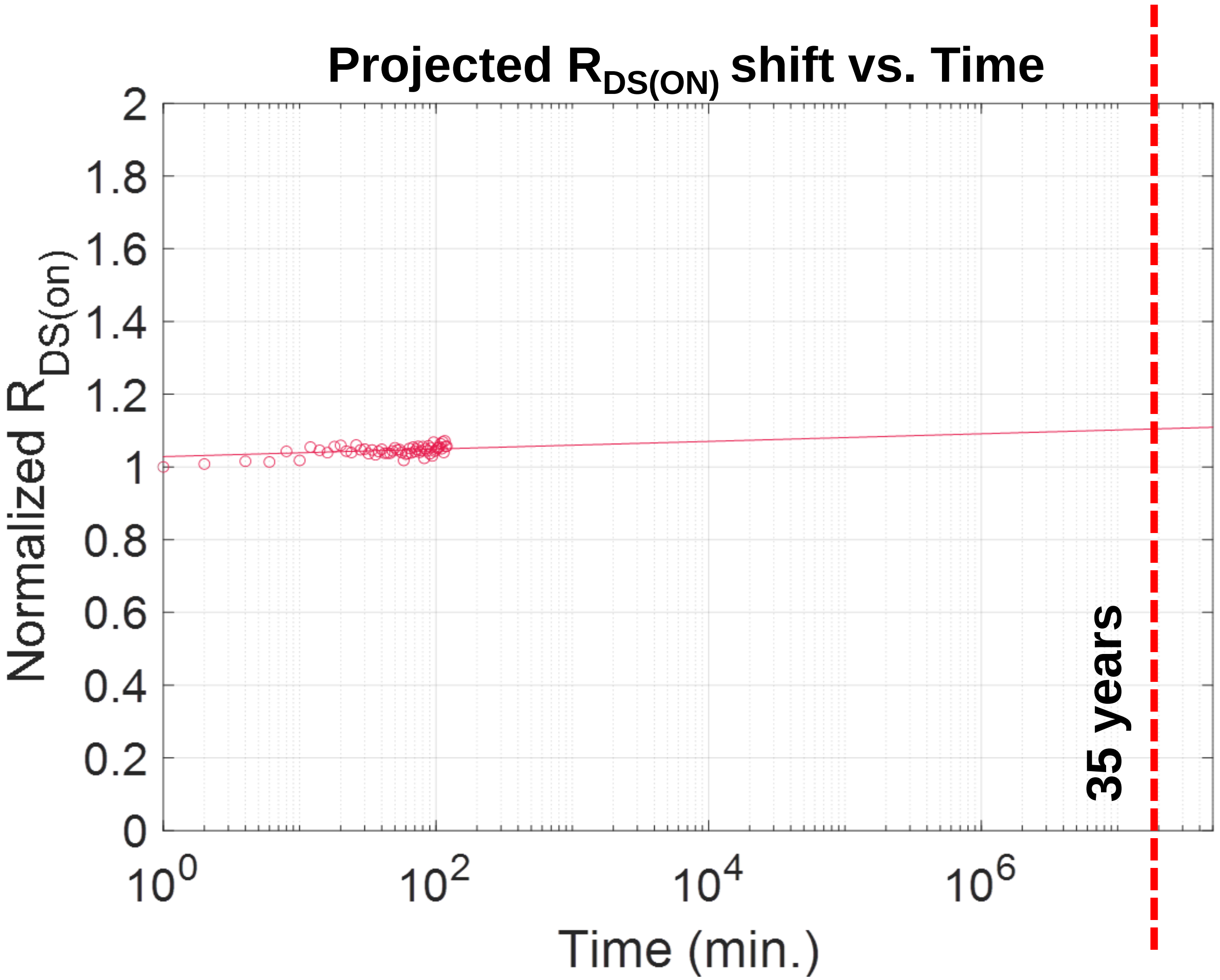


Function	Part Number	Size (mm x mm)	V_{DS} (V)	$R_{DS(on)}$ max (mΩ)	Q_G typ (nC)	Q_{RR} typ (nC)
Primary	EPC2218	3.5 x 1.95	100	3.2	11.8	0
Primary	EPC2302	3 x 5 QFN	100	1.8	18	0
Primary	EPC2306*	3 x 5 QFN	100	3.8	11	0

** Sampling*

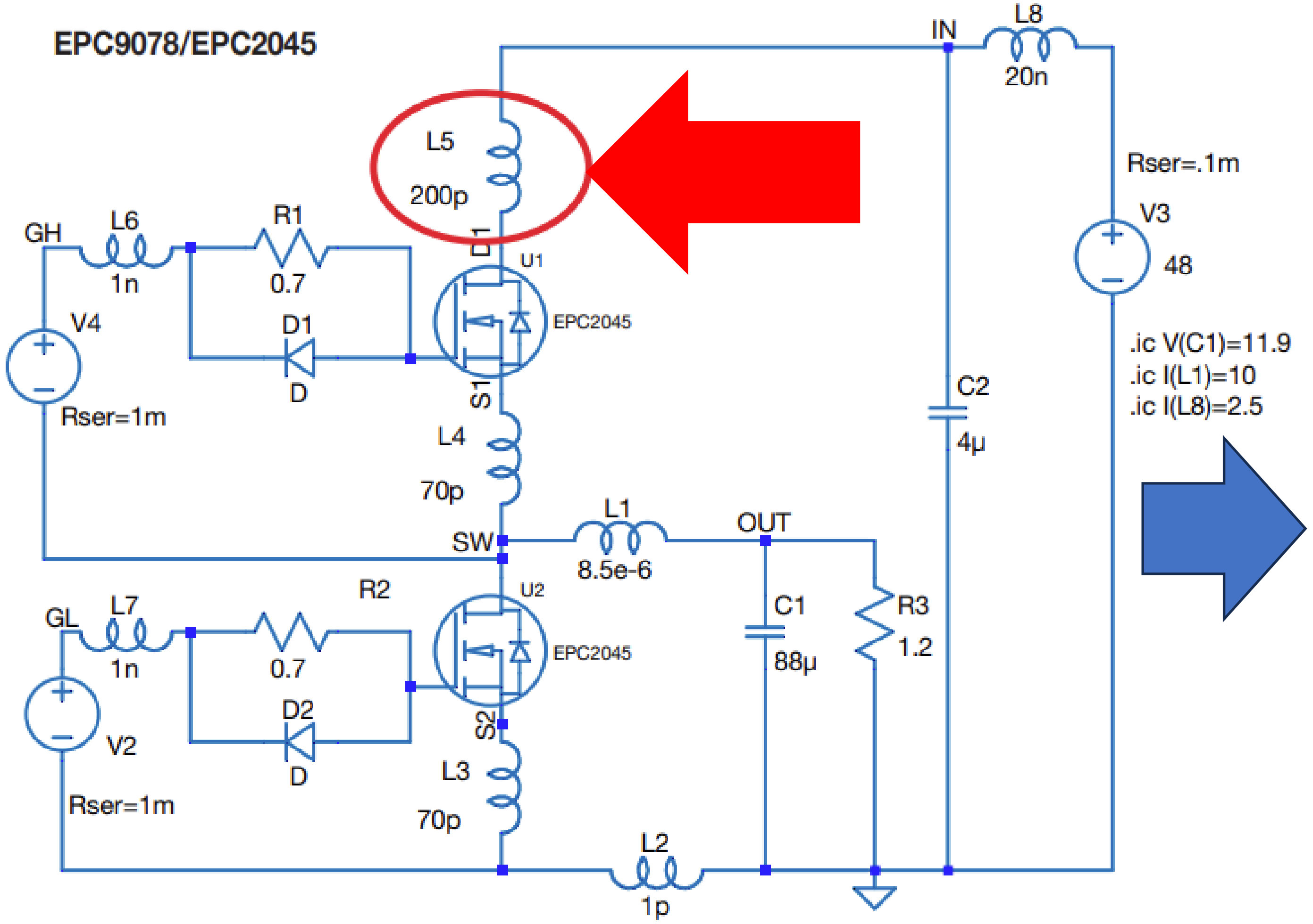
Drain Bias: Full Bridge Topology for Solar

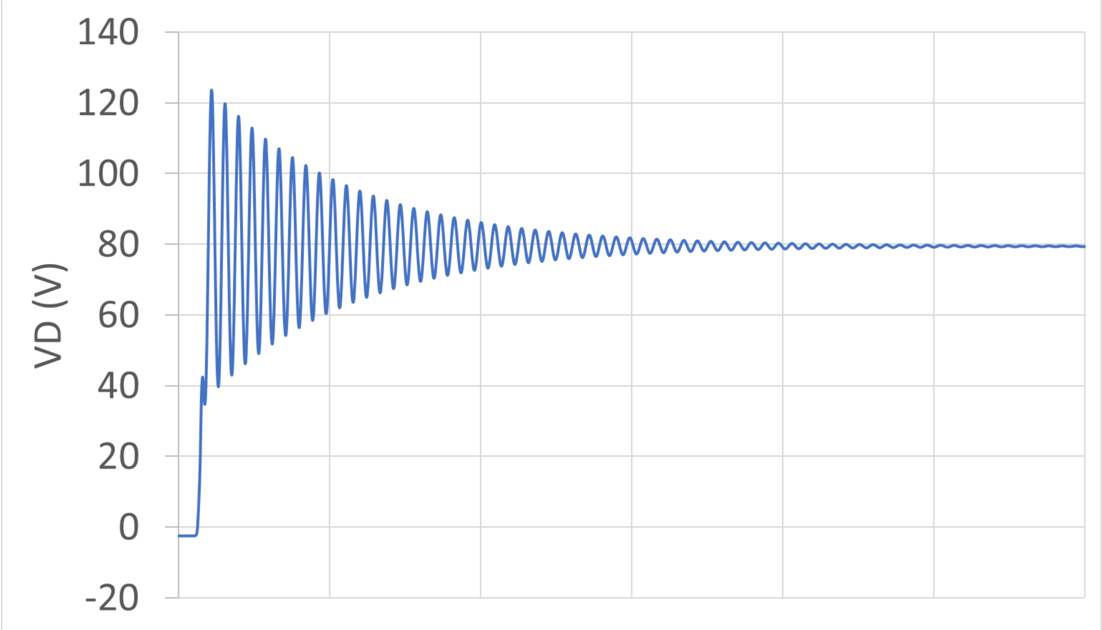
- EPC2218 (100V V_{DSMax}) eGaN FET is a good fit
- A representative EPC2218 device was tested under continuous hard switching at 100 kHz and 80V (80% V_{DSMax})



Apply the Model to Project Lifetime for a Buck Converter

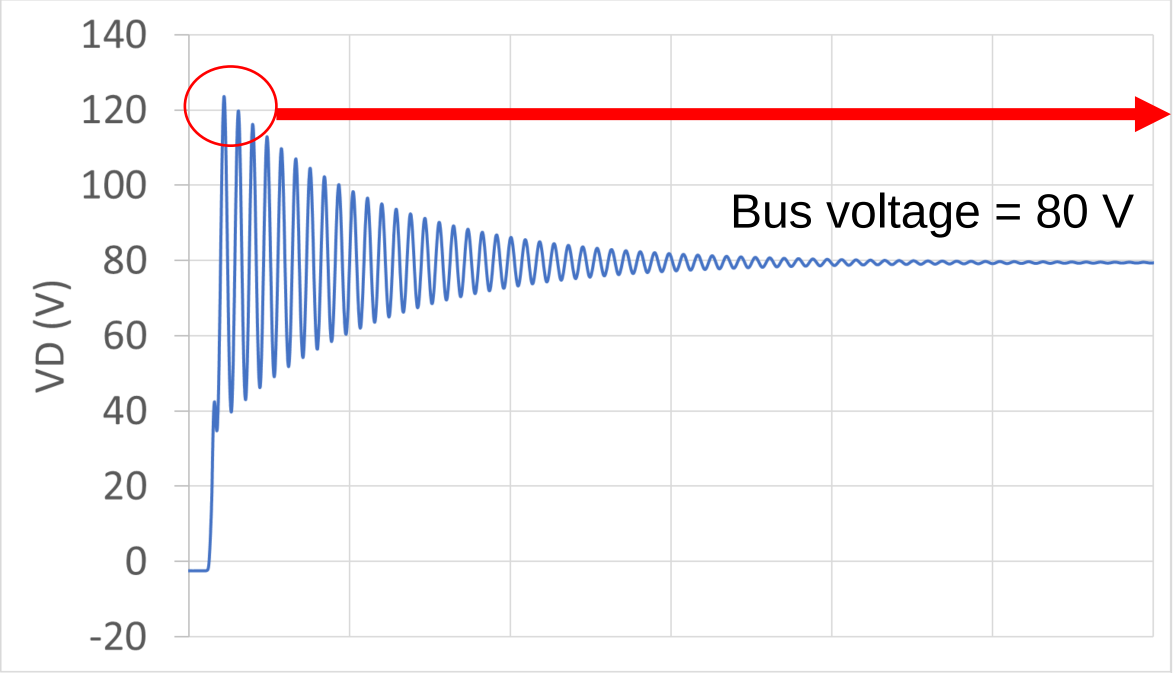
A Common 48 V–12 V Buck Converter



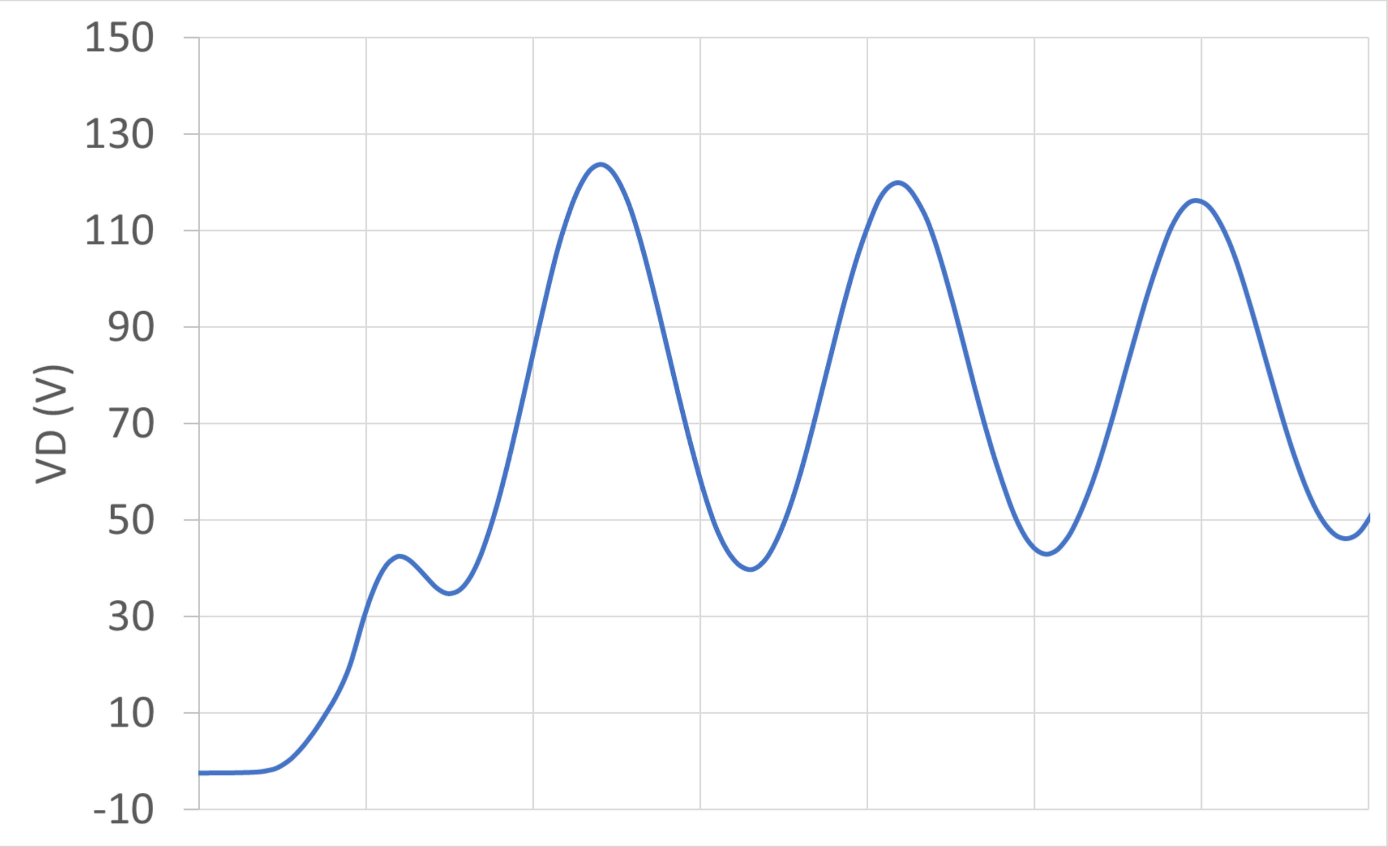


Key Stressor 1: Overvoltage Ringing

Simulated turn-off waveform of a buck with a peak ringing at 120V

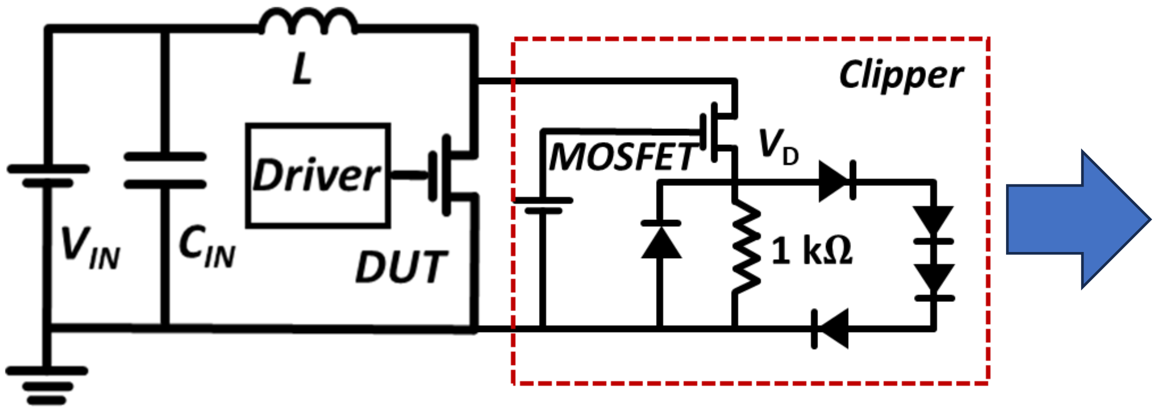


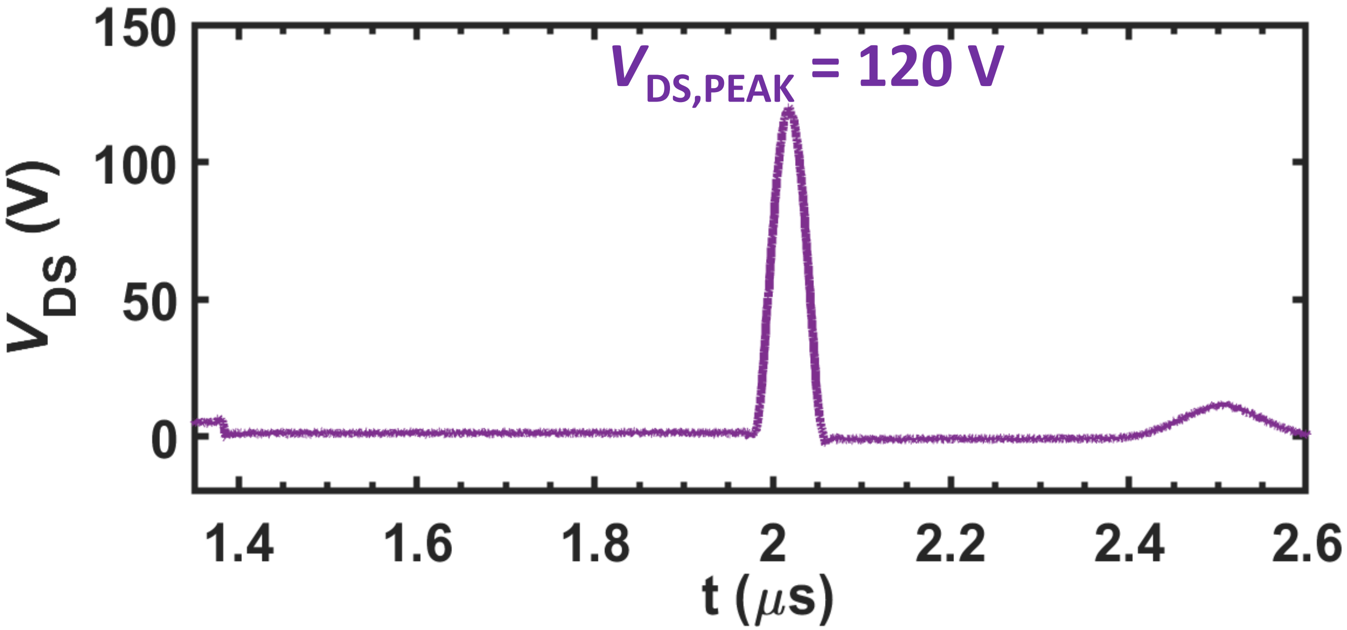
Overvoltage ringing can be simulated by sinusoidal voltage pulses.



Unclamp inductive switching: 120V Peak Transient Overvoltage

Unclamped inductive switching (UIS) circuit is developed to simulate the overvoltage ringing at 120V (120% of $V_{DS,\ Max}$ = 100 V)



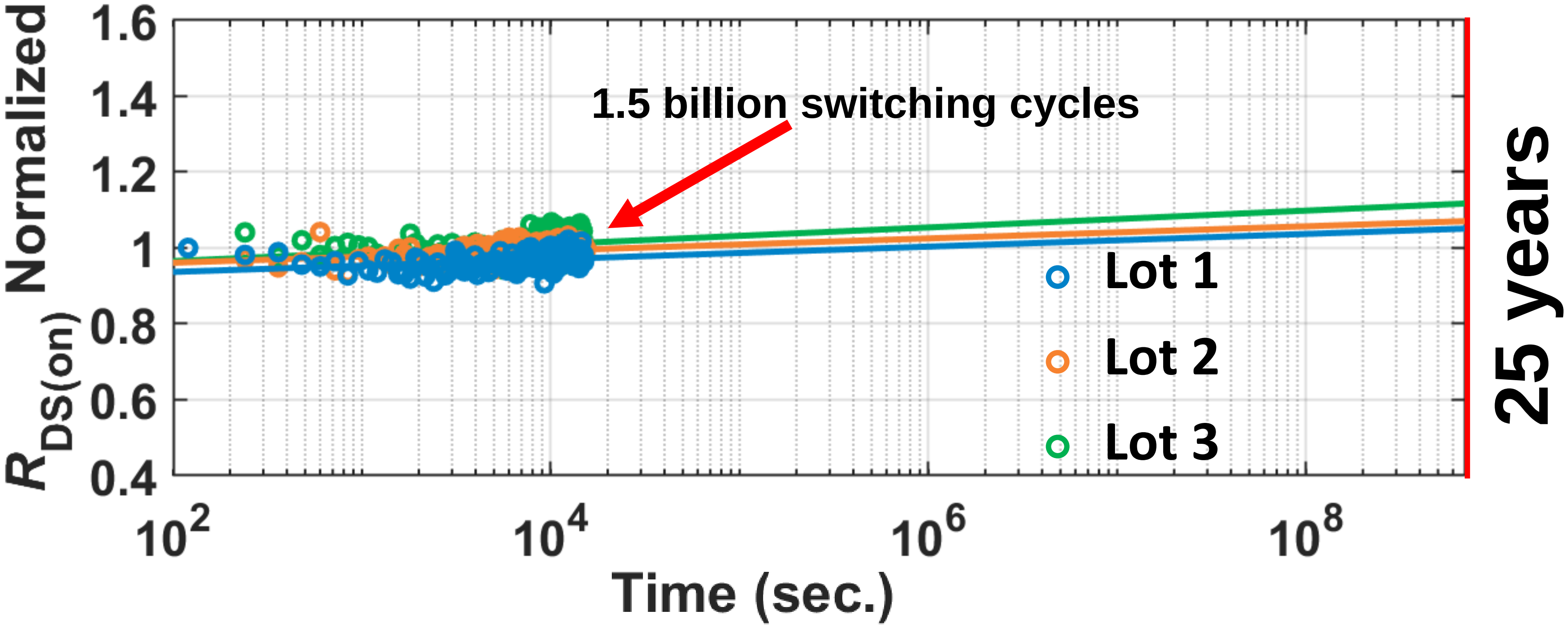


- 100 kHz frequency
- 6% duty cycle where $R_{DS(on)}$ is measured in-situ

R. Zhang, R. Garcia, R. Strittmatter, Y. Zhang and S. Zhang, "In-situ RDS(ON) Characterization and Lifetime Projection of GaN HEMTs under Repetitive Overvoltage Switching," IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2023.3290117.

120V Overvoltage Ringing on EPC2218 (100V rated)

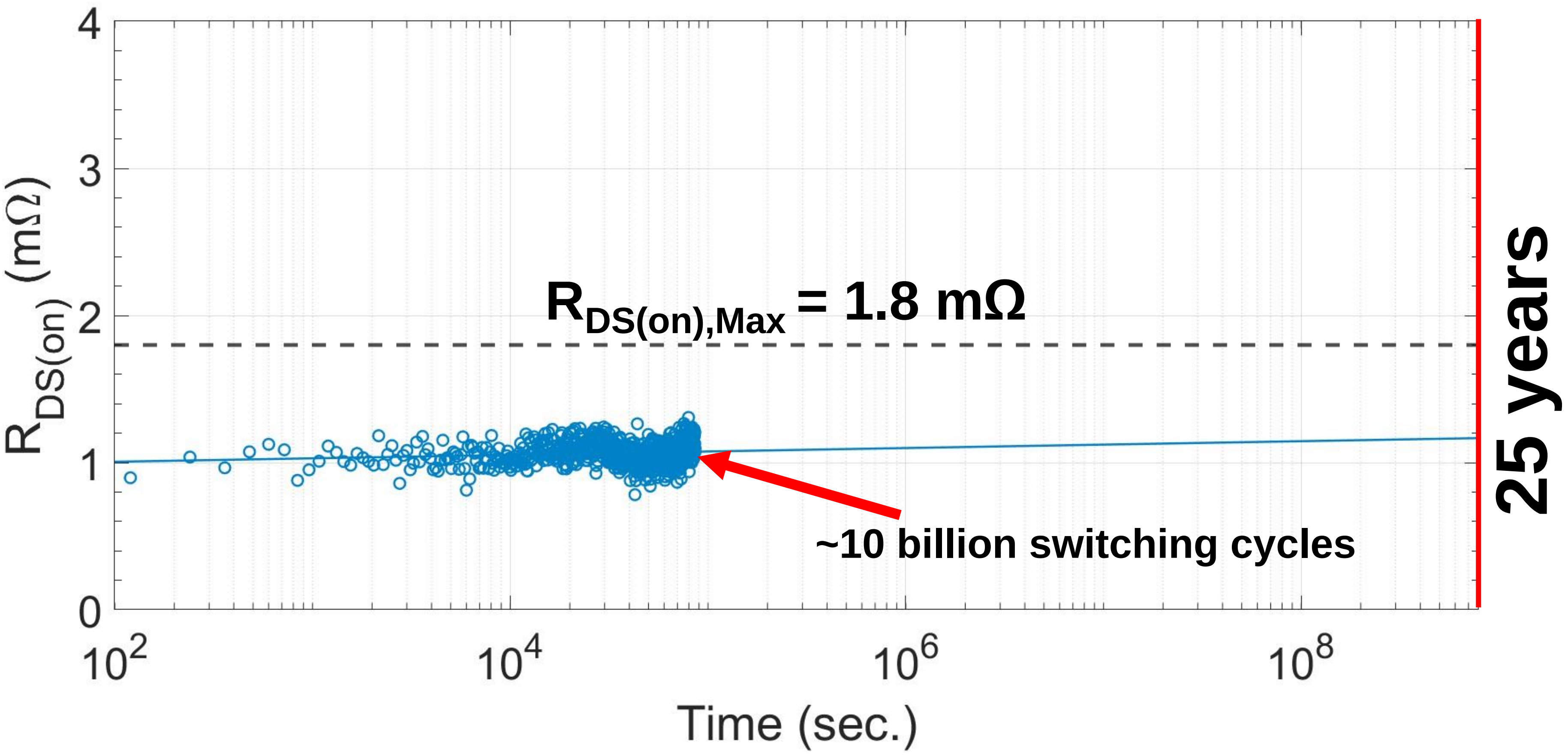
- Three representative EPC2218 devices from 3 different lots were tested under ***120V peak overvoltage pulses*** to 1.5 billions switching cycles.



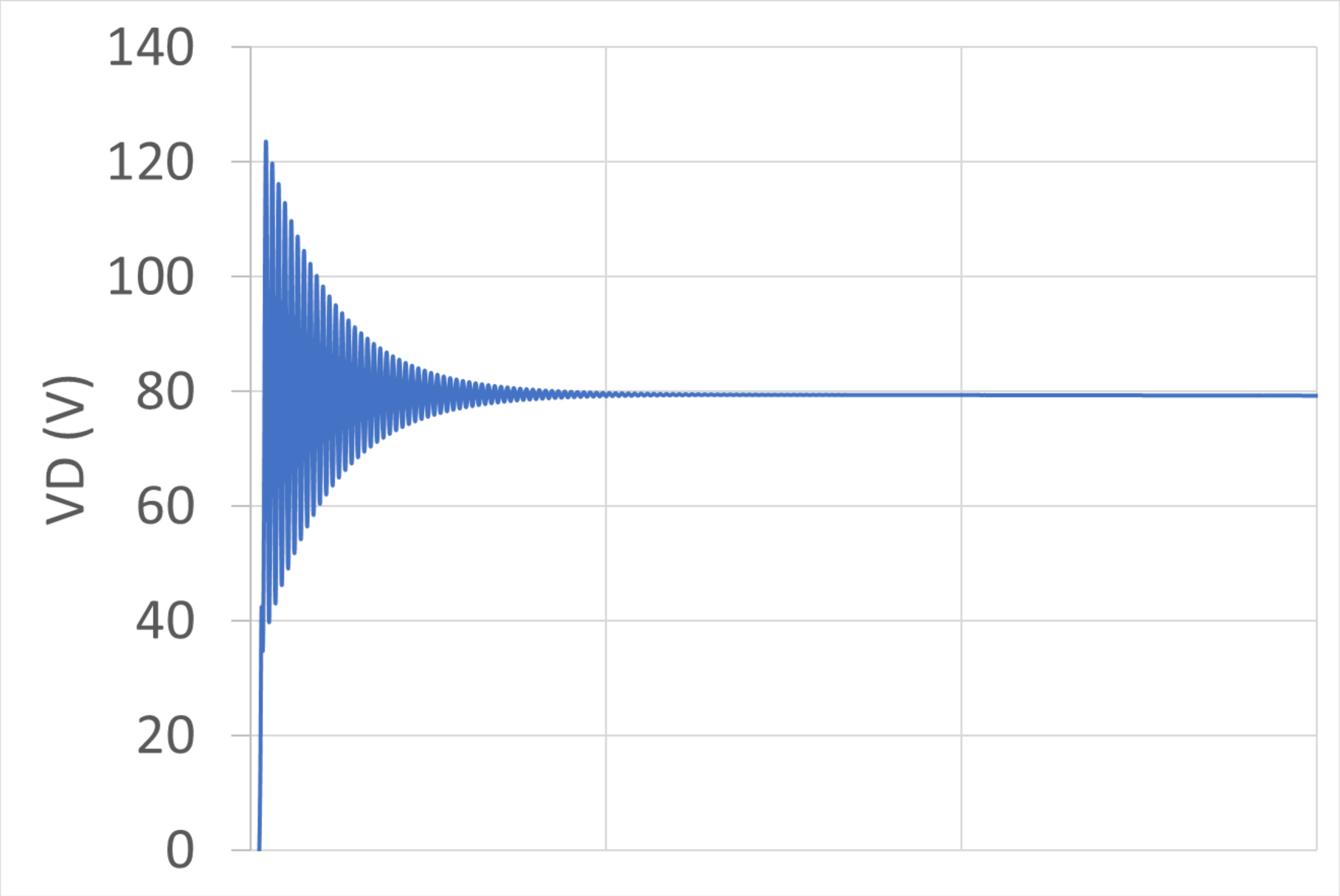
R. Zhang, R. Garcia, R. Strittmatter, Y. Zhang and S. Zhang, "In-situ RDS(ON) Characterization and Lifetime Projection of GaN HEMTs under Repetitive Overvoltage Switching," IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2023.3290117.

120V Overvoltage Ringing on EPC2302 (100V rated)

- One representative EPC2302 devices was tested under 120V peak overvoltage pulses to ~10 billions switching cycles.

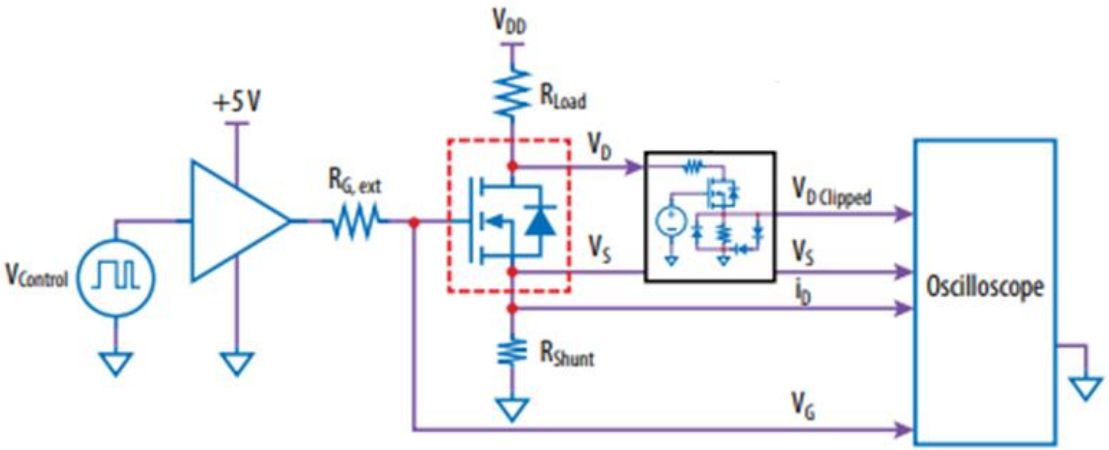


Key Stressor 2: Bus Voltage = 80 V



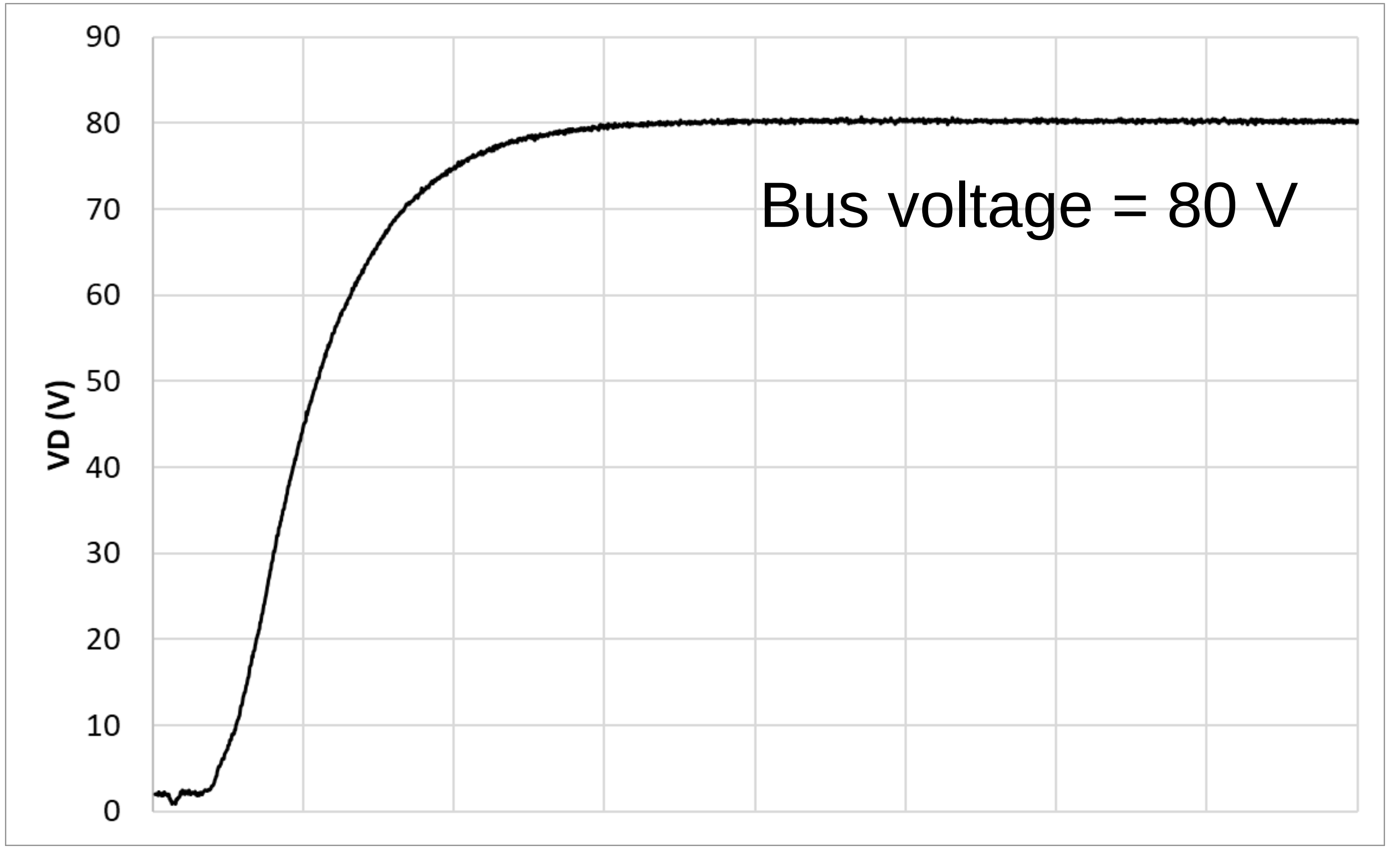
Key Stressor 2: Bus Voltage

Resistive Load Hard Switching Circuit



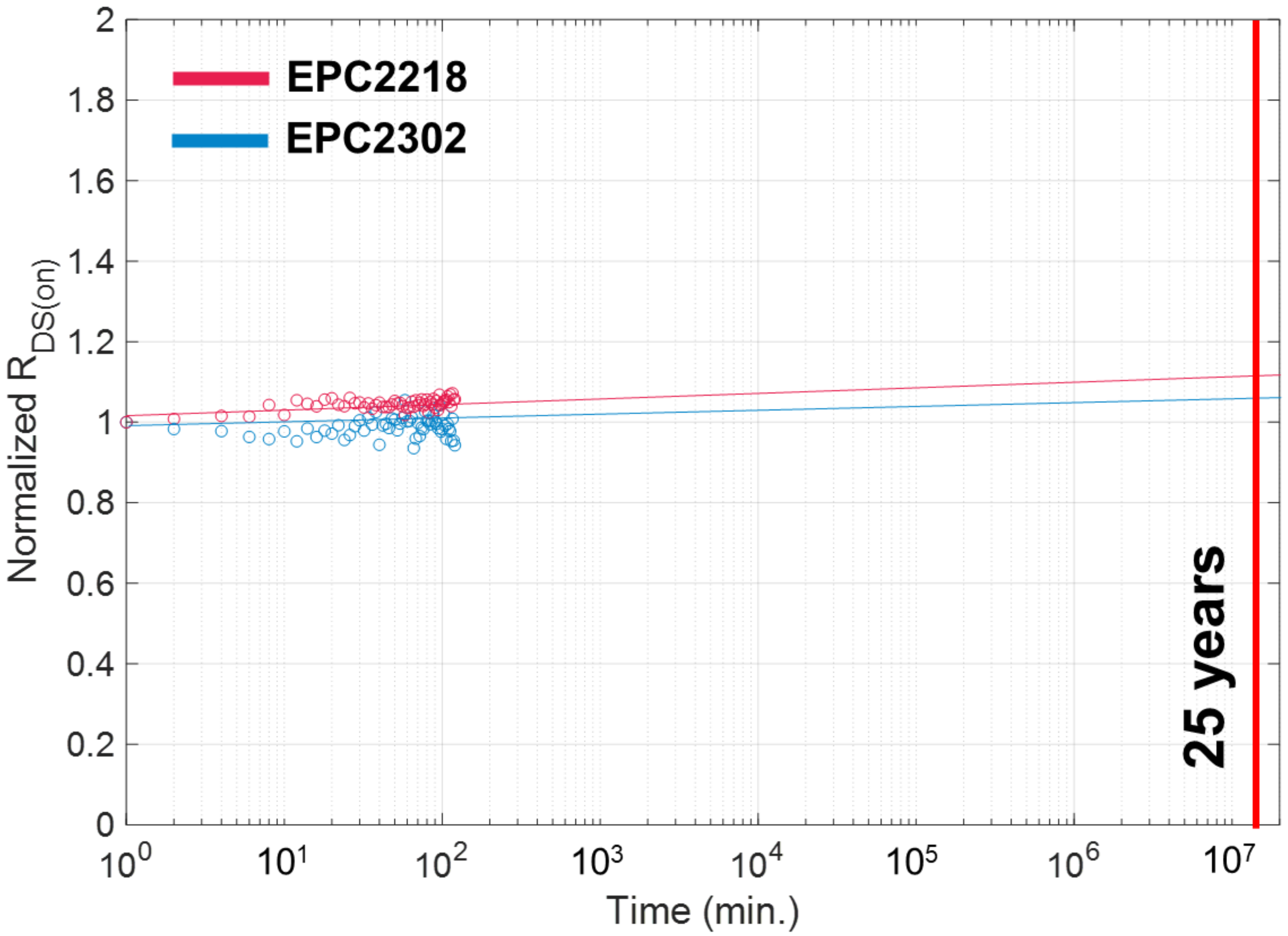
- 100 kHz frequency
- 15% duty cycle where RDS(on) is measured in-situ

Measured VD switching Waveform in Turn-off

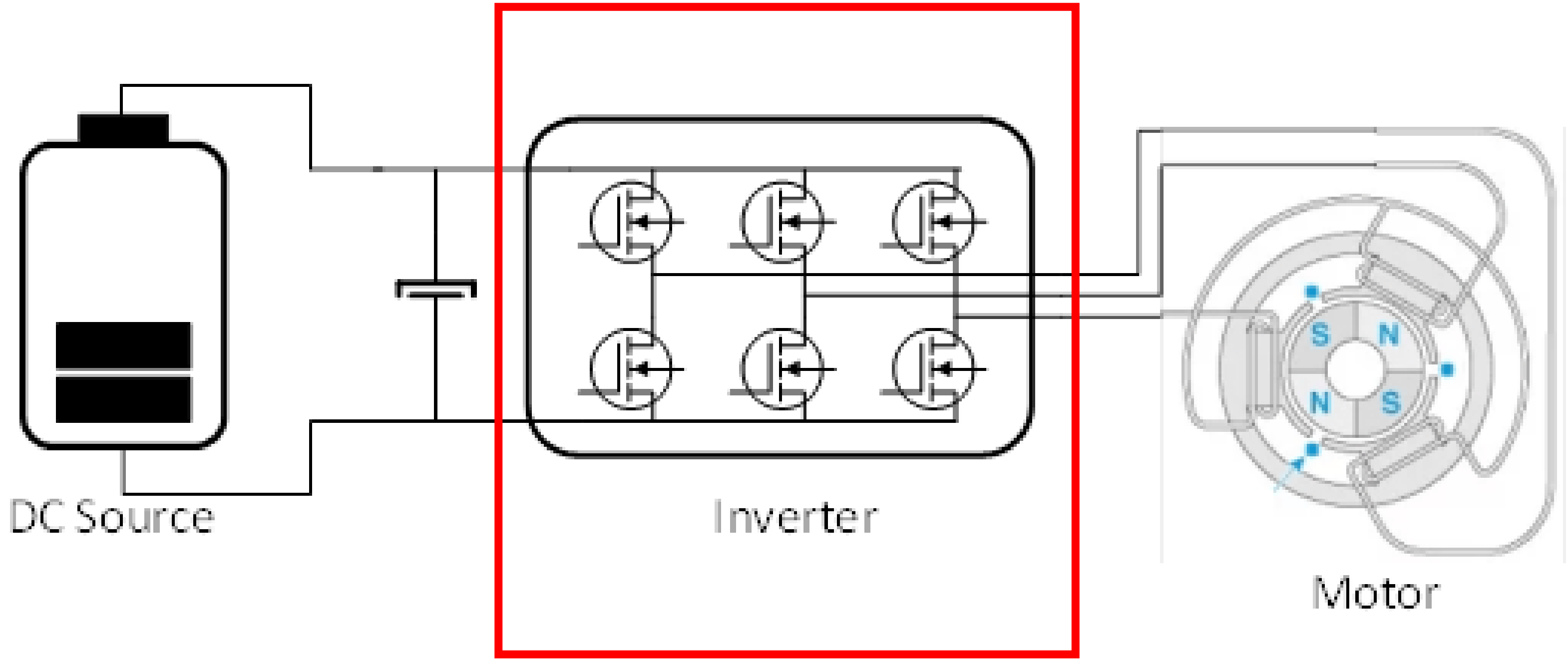


Resistive Load Hard Switching Test Results

- A representative EPC2218 and EPC2302 were tested under continuous hard switching at 100 kHz and **80V (80% V_{DSMax}).**

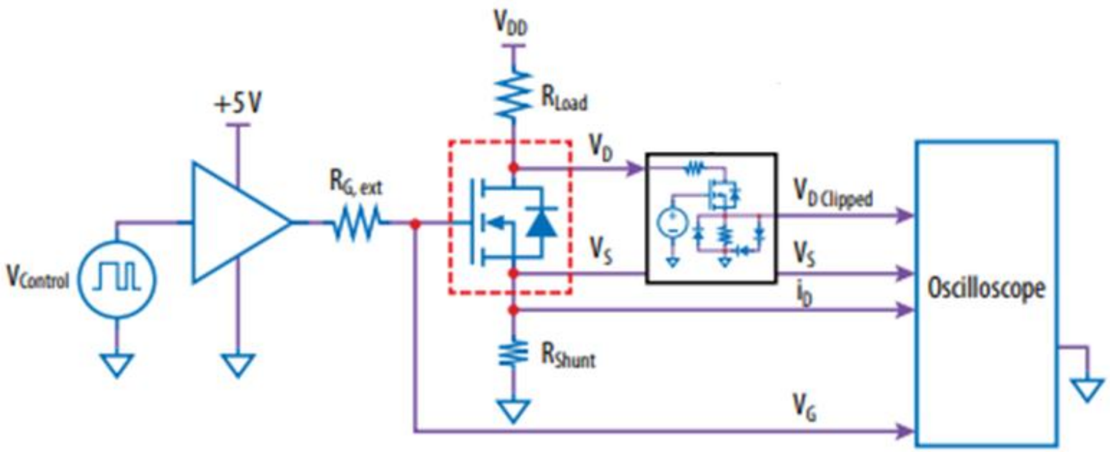


Apply the Drain Lifetime Model to Motor Drives

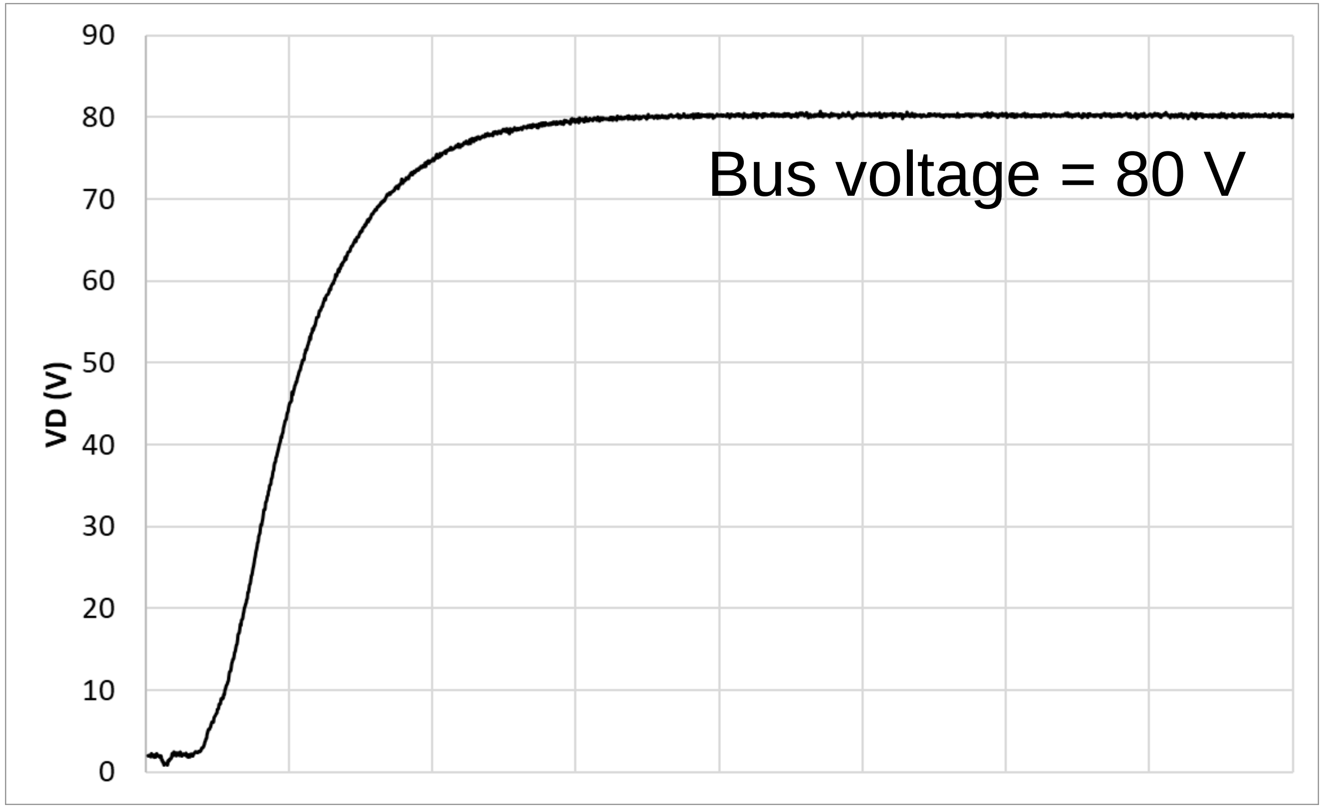


EPC's 100V rated ($V_{DS,Max}$) eGaN solution is a good fit for this motor drive application

Resistive Load Hard Switching Circuit



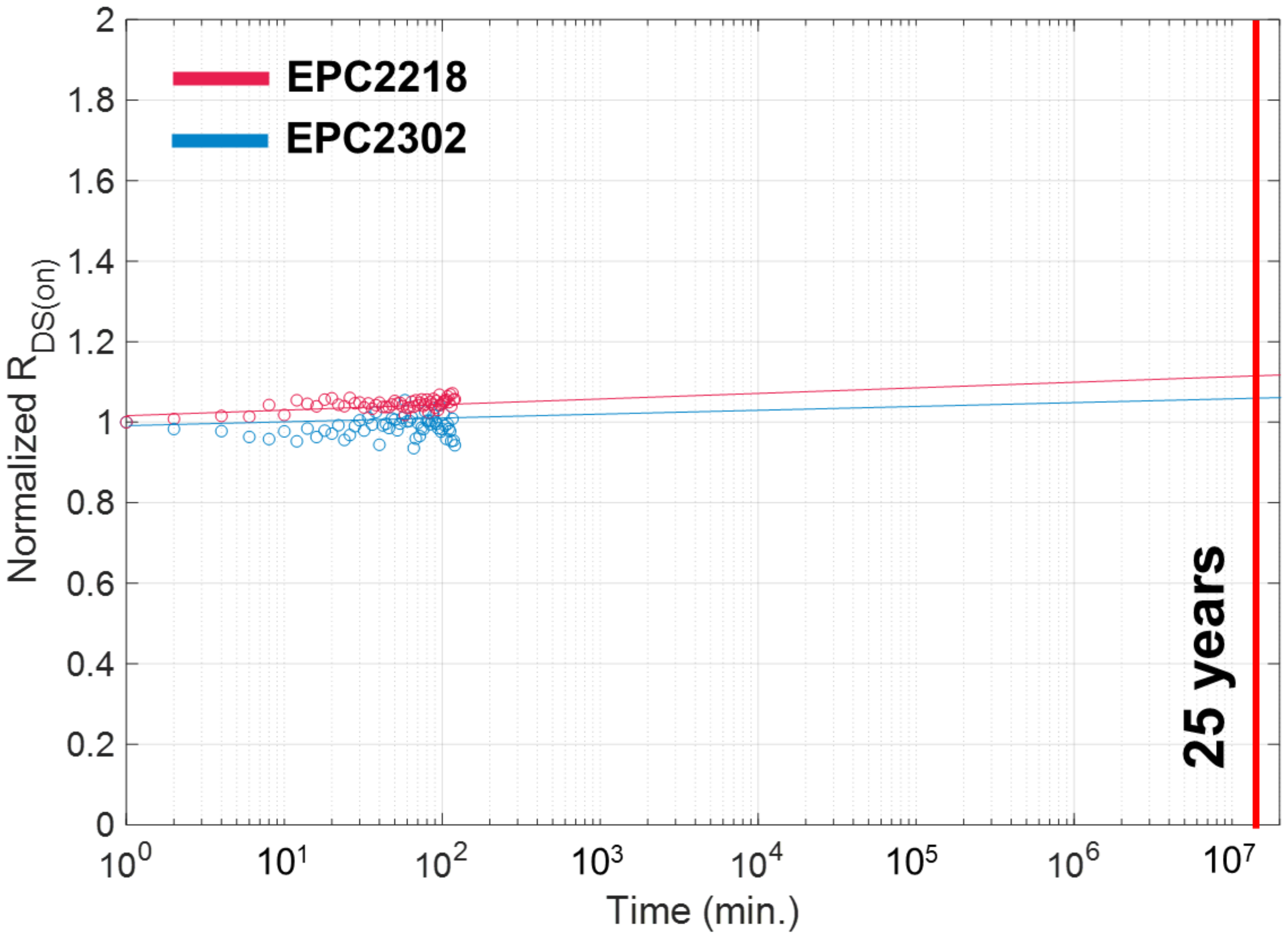
Measured VD switching Waveform



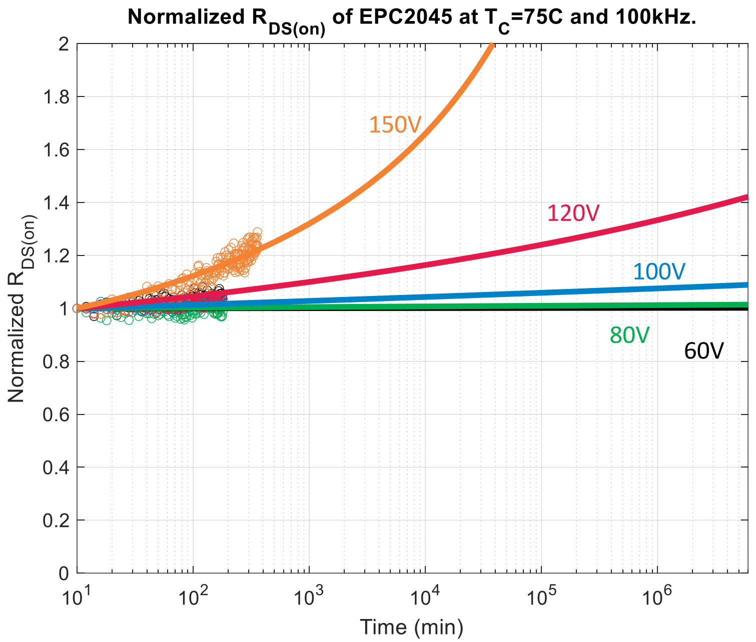
- 100 kHz frequency
- 85% duty cycle (8.5 us) during which the GaN FET is Off.
- 15% duty cycle (1.5 us) during which $R_{DS(on)}$ is measured *in-situ.*

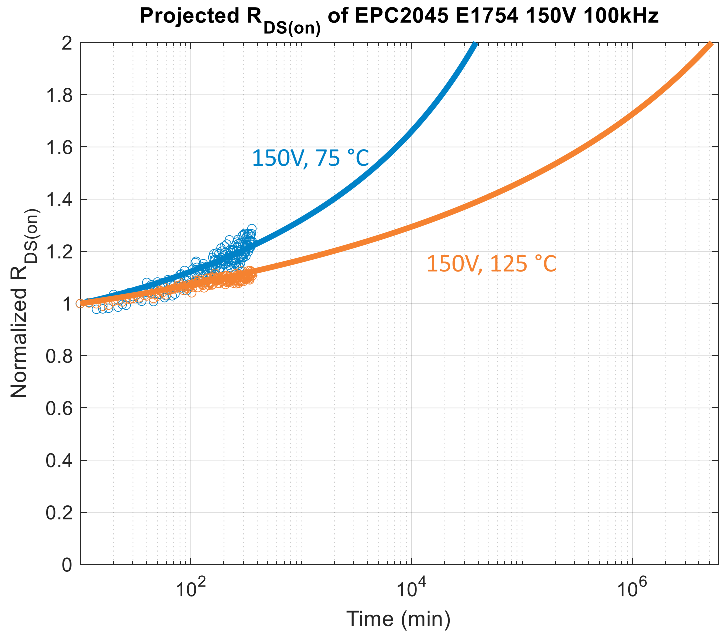
Resistive Load Hard Switching Test Results

- A representative EPC2218 and EPC2302 were tested under continuous hard switching at 100 kHz and **80V (80% V_{DSMax}).**



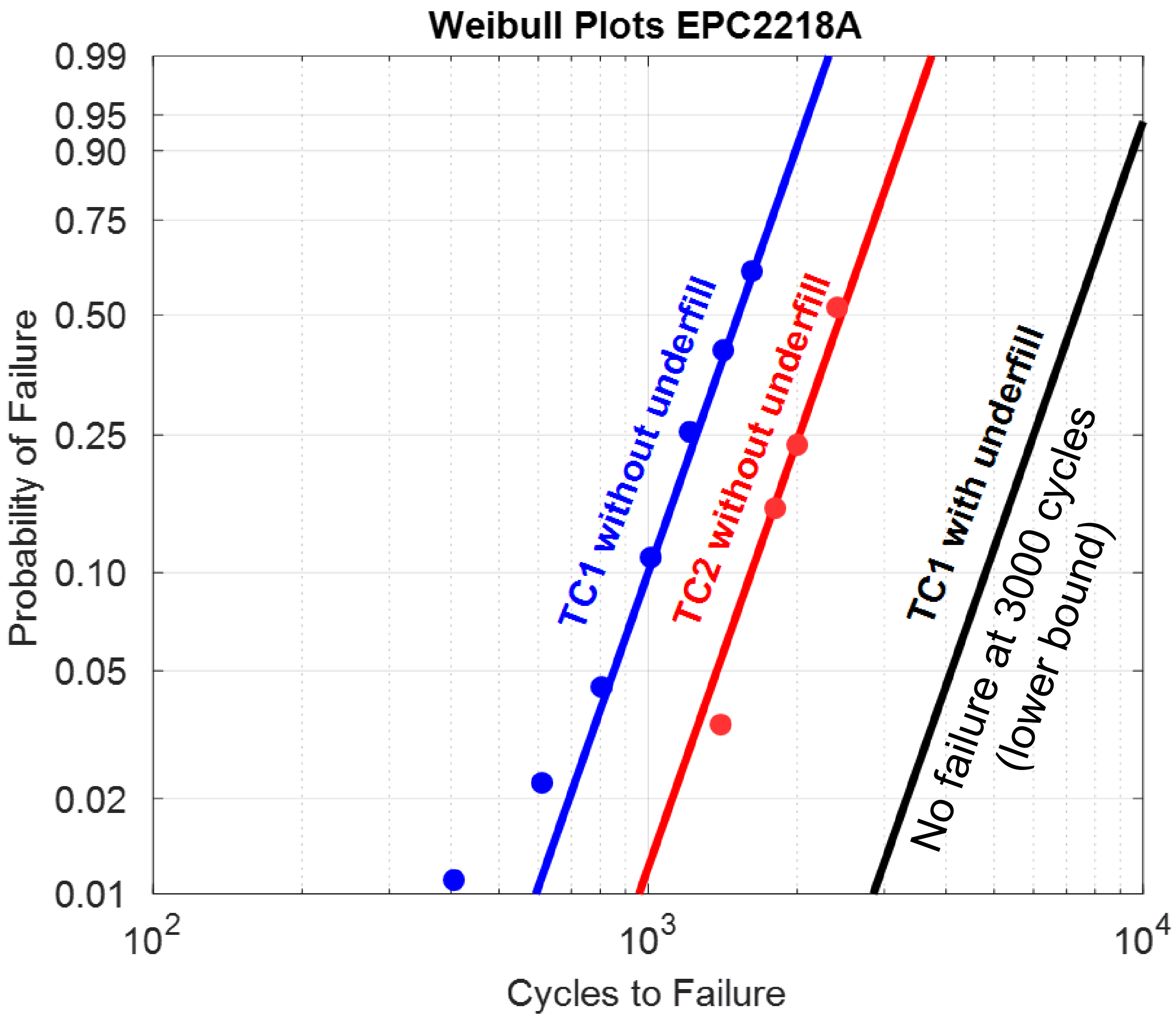
Going to Extremes





Temperature Cycling (TC)

Board Level TC of EPC2218A (100V eGaN transistor)



- TC1: -40°C to 125°C
  - With underfill, 88 devices
  - Without underfill, 88 devices
- TC2 : -40°C to 105°C
  - Without underfill, 88 devices

Development of Lifetime Model for TC

Arrhenius term:

Solder Creep

Frequency term:

No. of cycle/day

ΔT term:

Solder Fatigue

$$N = A \cdot \boxed{f^{-\alpha}} \cdot \boxed{\Delta T^{-\beta}} \cdot \boxed{\exp\left(\frac{E_a}{kT_{Max}}\right)}$$

For EPC2218A using SAC305 solder: α = -1/3; β = 2.3; E_a = 0.18 eV

1. B. Han , Y. Guo, "Determination of an Effective Coefficient of Thermal Expansion of Electronic Packaging Components: A Whole-Field Approach," IEEE TRANSACTIONS ON COMPONENTS, PACKAGING. AND MANUFACTURING TECHNOLOGY-PART A, VOL. 19, NO. 2, JUNE 1996
2. Automotive Electronics Council, "FAILURE MECHANISM BASED STRESS TEST QUALIFICATION FOR DISCRETE SEMICONDUCTORS IN AUTOMOTIVE APPLICATIONS", AEC-Q101-Rev E, March 2021
3. Norris, K. C., & Landzberg, A. H., "Reliability of Controlled Collapse Interconnections", IBM Journal of Research and Development, 13(3), pp. 266–271, 1969
4. Vasudevan, V., and Fan, X., "An Acceleration Model for Lead-Free (SAC) Solder Joint Reliability Under Thermal Cycling," ECTC, pp. 139–145, 2008

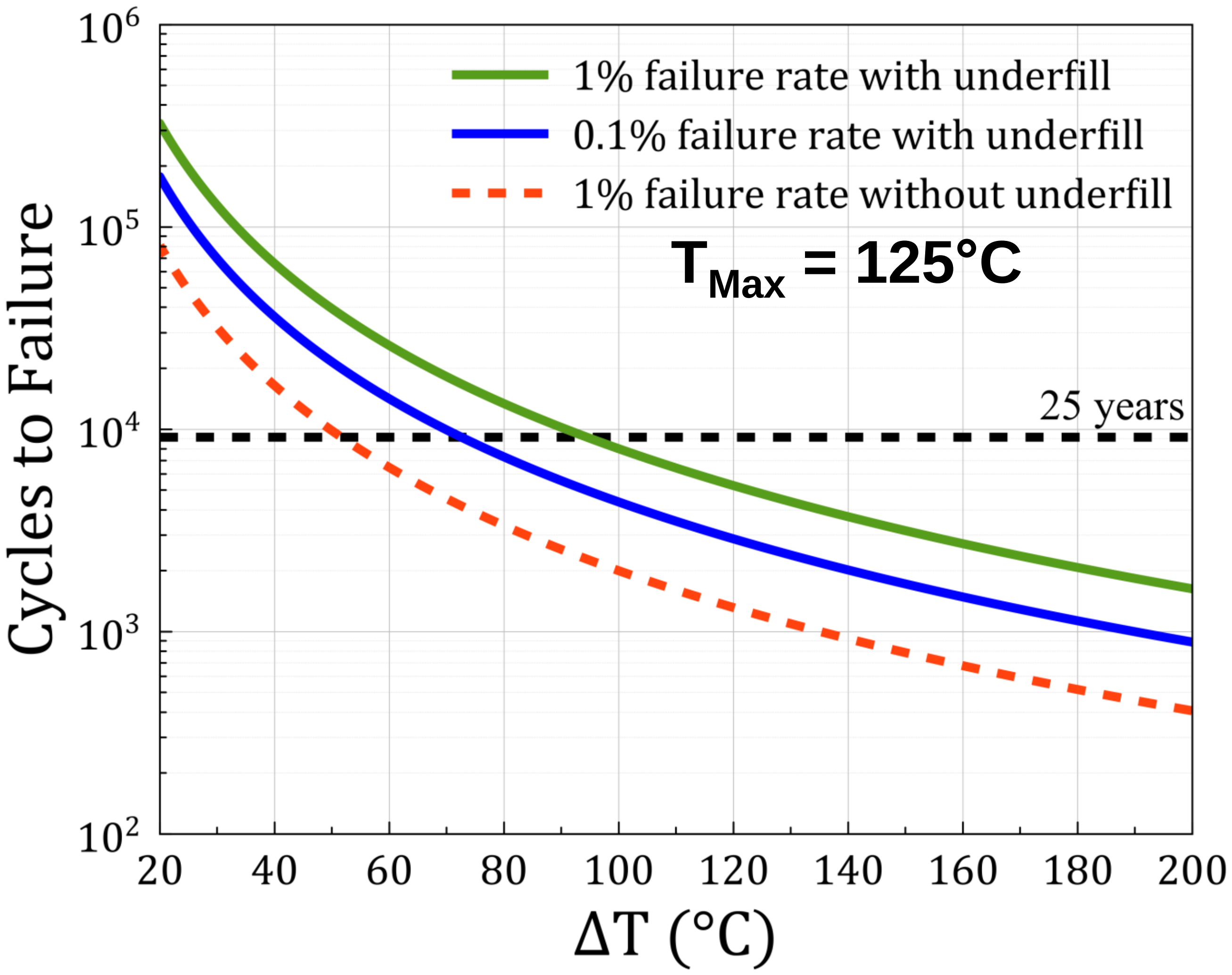
Temperature Cycling of EPC2218A (100V eGaN transistor)

1% of failure rate:

- With underfill - ΔT of 95°C
- Without underfill - ΔT of ~50°C

0.1% of failure rate:

- With underfill - ΔT of ~73°C



Apply the TC Lifetime Model to Real-world Scenarios (Solar)

Estimate Lifetimes in Real-World Scenarios

Each mission profile

$$\frac{1}{N_{Total}} = \frac{a}{N_{\Delta T_a}} + \frac{b}{N_{\Delta T_b}} + \cdots + \frac{i}{N_{\Delta T_i}}$$

a, b, … i = the factional lifetime of each mission profile

$N_{\Delta Ti}$ = No of cycles-to-failure for a given mission profile

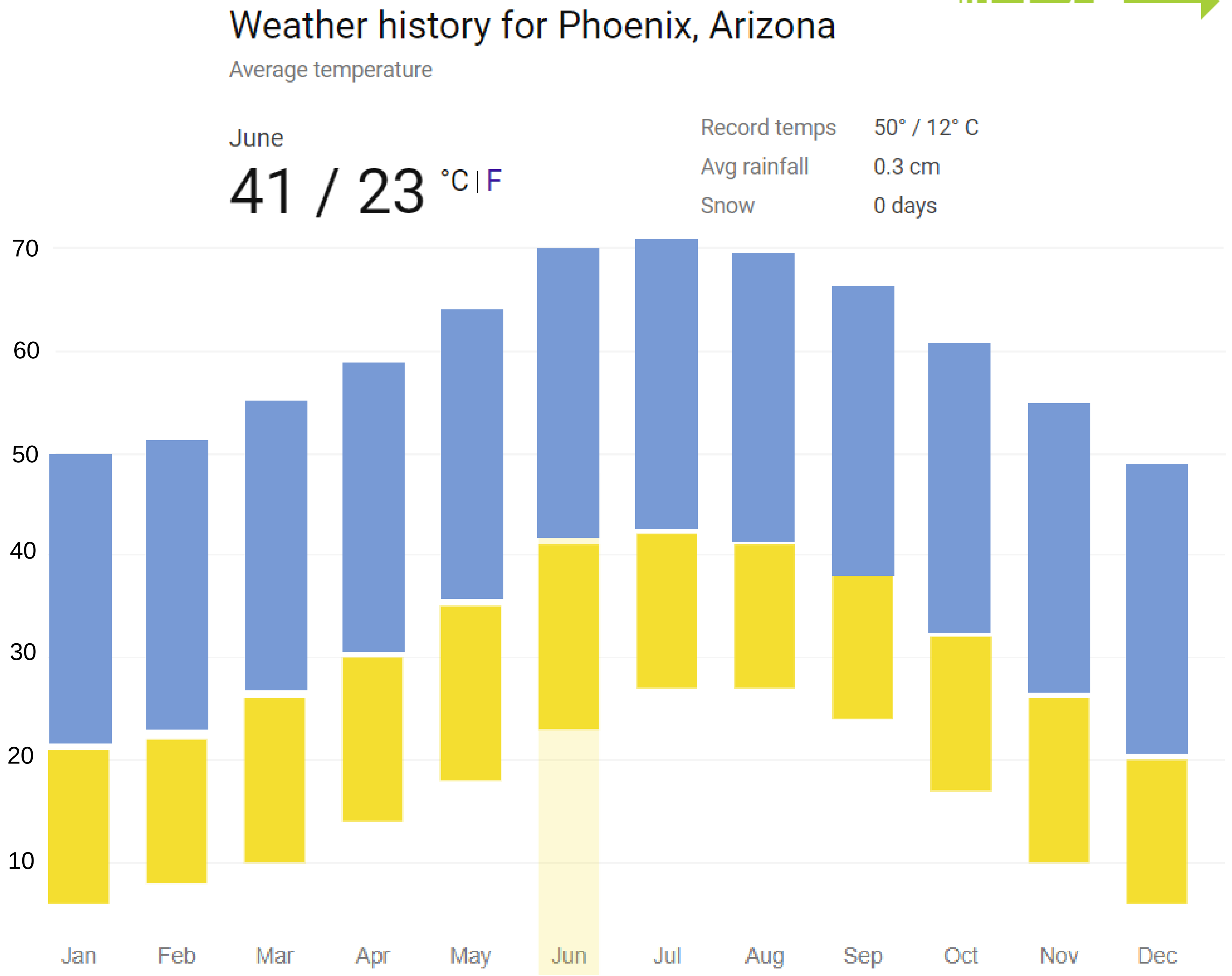
The most stringent mission profile ($N_{\Delta Ti}$) dominates the overall lifetime (N_{Total})

Predict Lifetime in a Real-world Scenario

N_{total} at Phoenix, AZ is estimated to be 10,971 cycles (10ppm failure rate), equivalent of *~30 years of continuous operation*

Self Heating (30°C)

Ambient Temperature



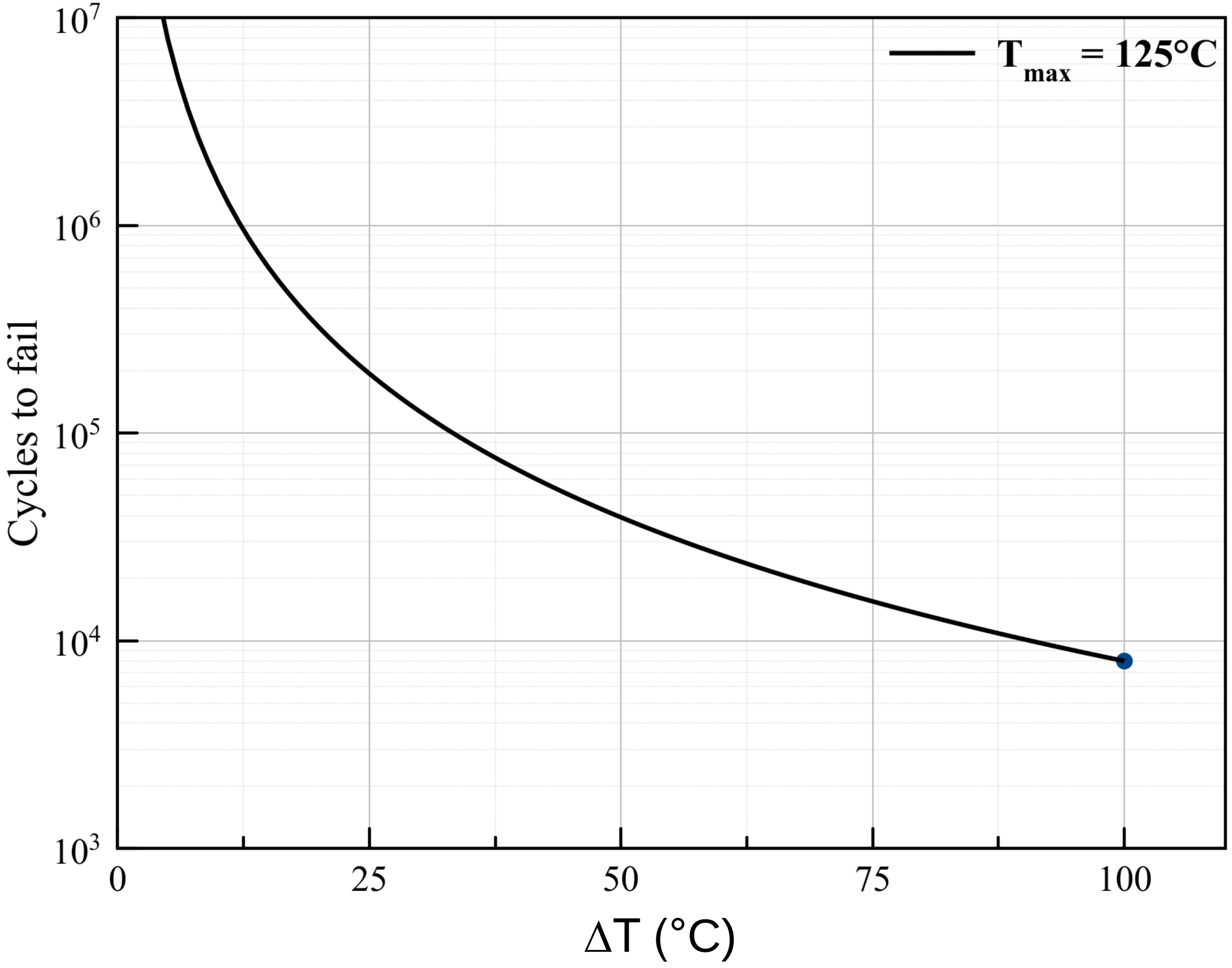
Apply the TC Lifetime Model to Real-world Scenarios (DC-DC)

Lifetime Projection at 1% Failure Rate for EPC2218 with Underfill

$T_{Max} = 125°C$

$$N = A \cdot f^{-\alpha} \cdot \Delta T^{-\beta} \cdot \boxed{\exp\left(\frac{E_a}{kT_{Max}}\right)}$$

Plot **N** (cycles-to-fail) vs. Δ**T** at ***1% failure rate*** from Test-to-Fail Weibull.

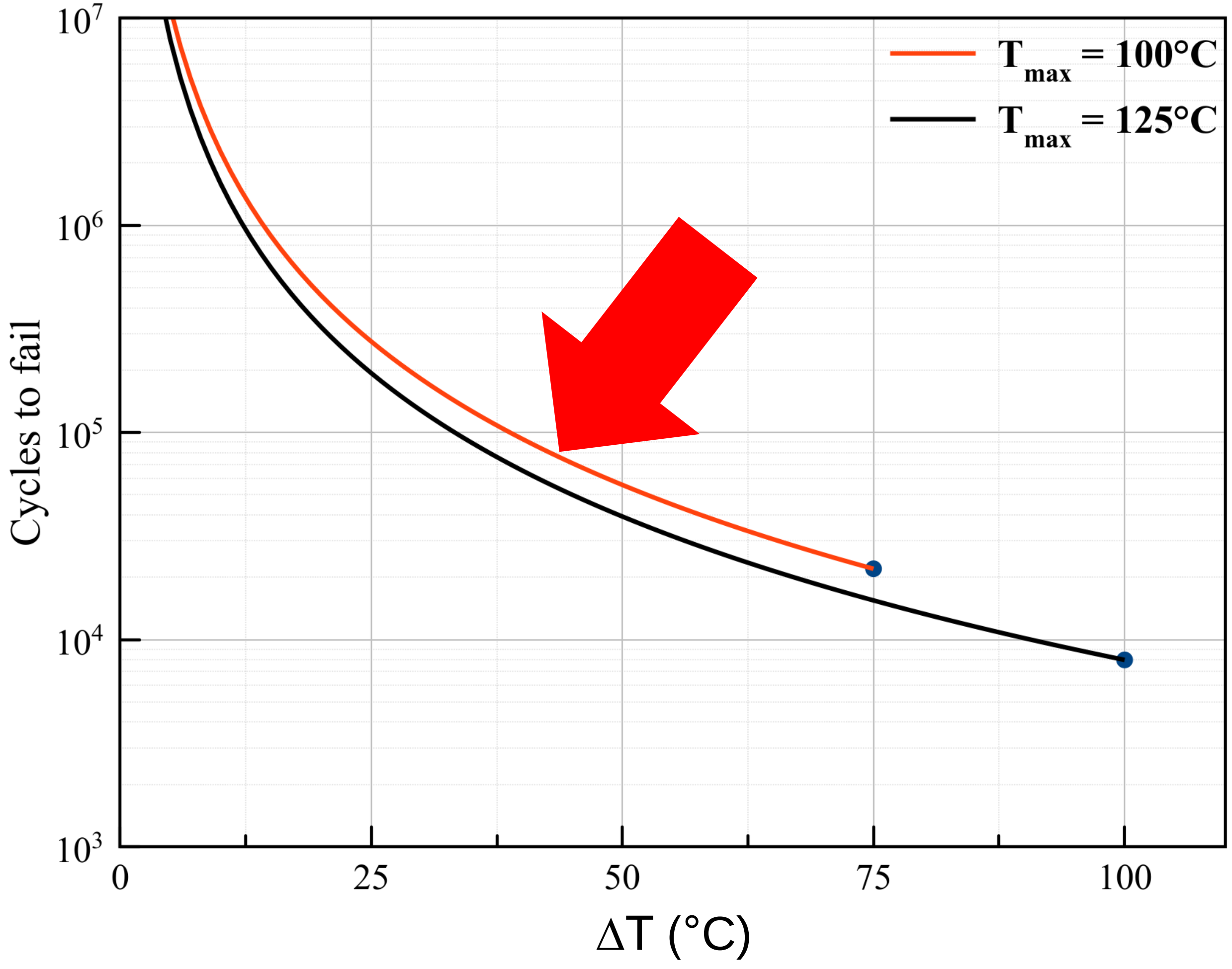


Lifetime Projection at 1% Failure Rate for EPC2218 with Underfill

$T_{Max} = 100°C$

$$N = A \cdot f^{-\alpha} \cdot \Delta T^{-\beta} \cdot \boxed{\exp\left(\frac{E_a}{kT_{Max}}\right)}$$

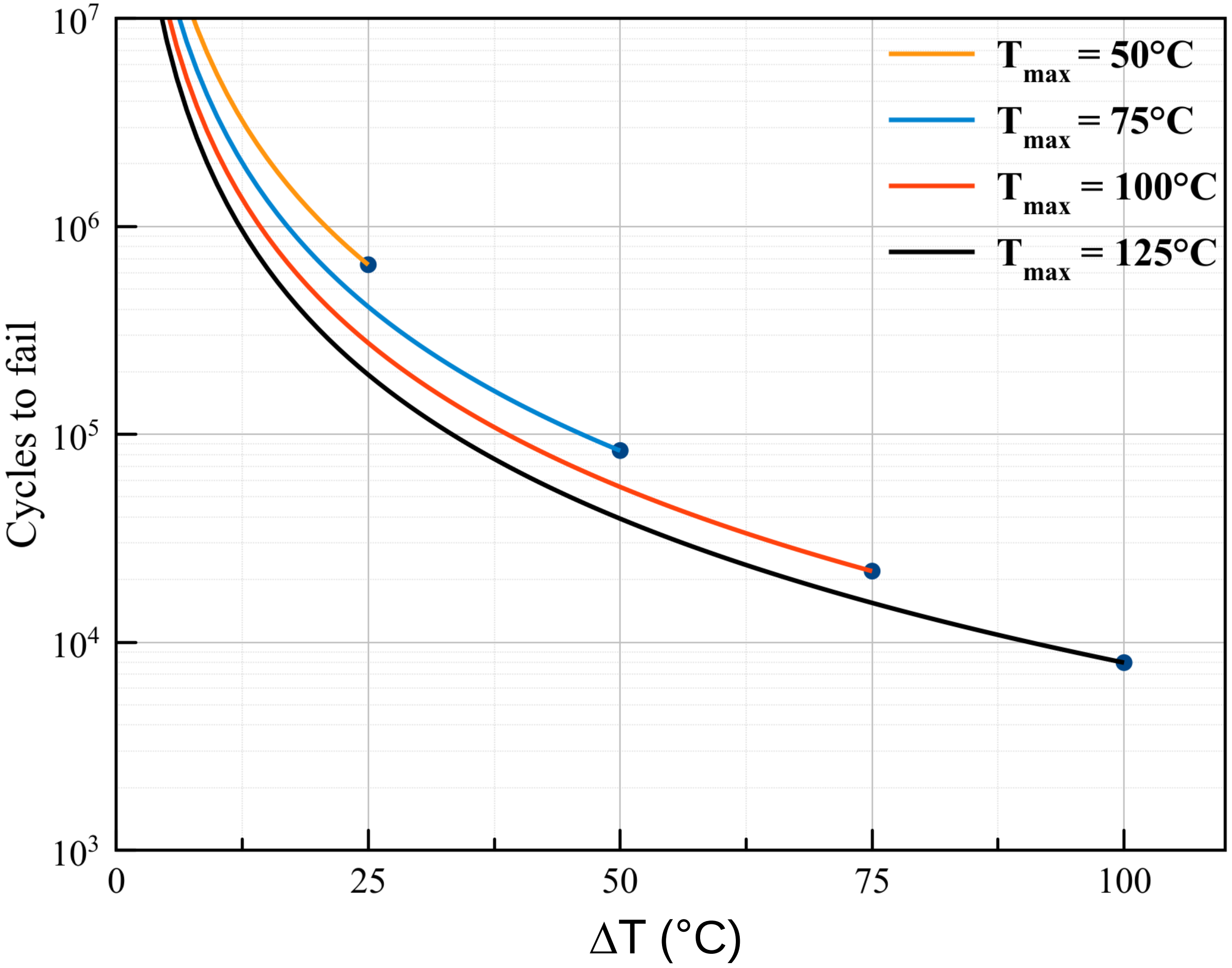
Plot **N** (cycles-to-fail) vs. Δ**T** at ***1% failure rate*** from Test-to-Fail Weibull.



Lifetime Projection at 1% Failure Rate for EPC2218 with Underfill

$$N = A \cdot f^{-\alpha} \cdot \Delta T^{-\beta} \cdot \boxed{\exp\left(\frac{E_a}{kT_{Max}}\right)}$$

- T_{Max} = 75°C
- T_{Max} = 50°C



Short Circuit

Short Circuit Test Method and Results

Fault under load (FUL): drain voltage is applied while gate is ON.

EPC2051 is a 100V rated eGaN transistor

Short-circuit pulse $V_{DS} = 60$ V	EPC2051 (Gen 5)	
	$V_{GS} = 6$ V	$V_{GS} = 5$ V
Mean TTF (µs)	9.33	21.87
Std. dev. (µs)	0.21	2.95
Min. TTF (µs)	9.08	18.53
Avg pulse power (kW)	3.03	2.03
Energy (mJ)	27.71	42.49
Die area (mm^2)	1.105	
Avg power/area (kW/mm^2)	2.74	1.84
Energy/area (mJ/mm^2)	25.08	38.46

Extreme Short Circuit Testing Results

Under extreme conditions of 500,000 pulses at 85 A, 5 µs pulse width ($I_{pulse,DS}$=37A), all electrical parameters remained within datasheet limits.

EPC2051	t = 0	100 k pulses	500 k pulses
V_{TH} (V)	1.8	2	2.1
I_{GSS} (µA)	11	33	55
I_{DSS} (µA)	7	5.5	5.1
$R_{DS(on)}$ (mΩ)	22	22.3	22.3
$I_{short\ circuit}$	84	77	74

Mechanical Stress Induced by Motor Movement

Bending Test setup

Followed IEC 60068 – 2 – 21 for the bending test

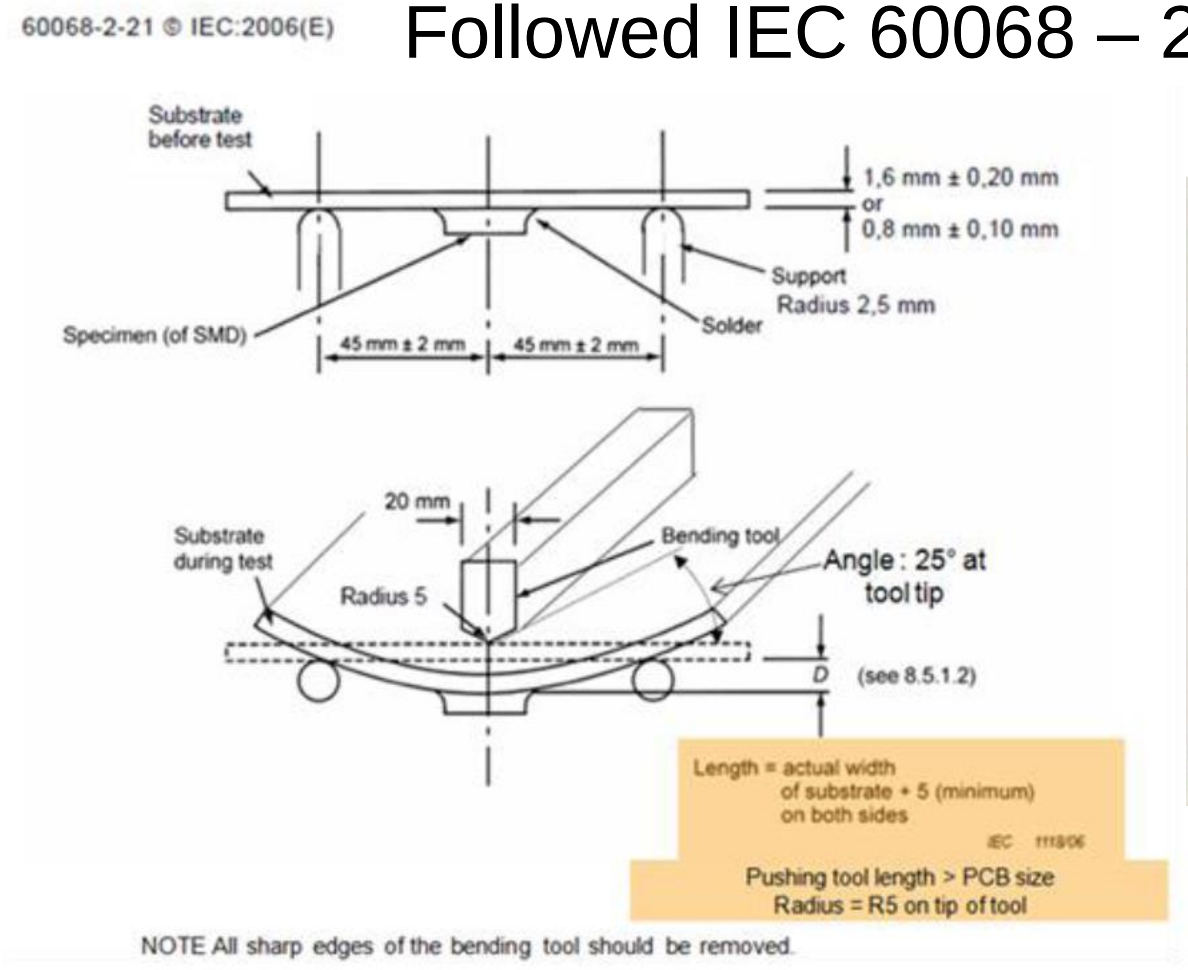
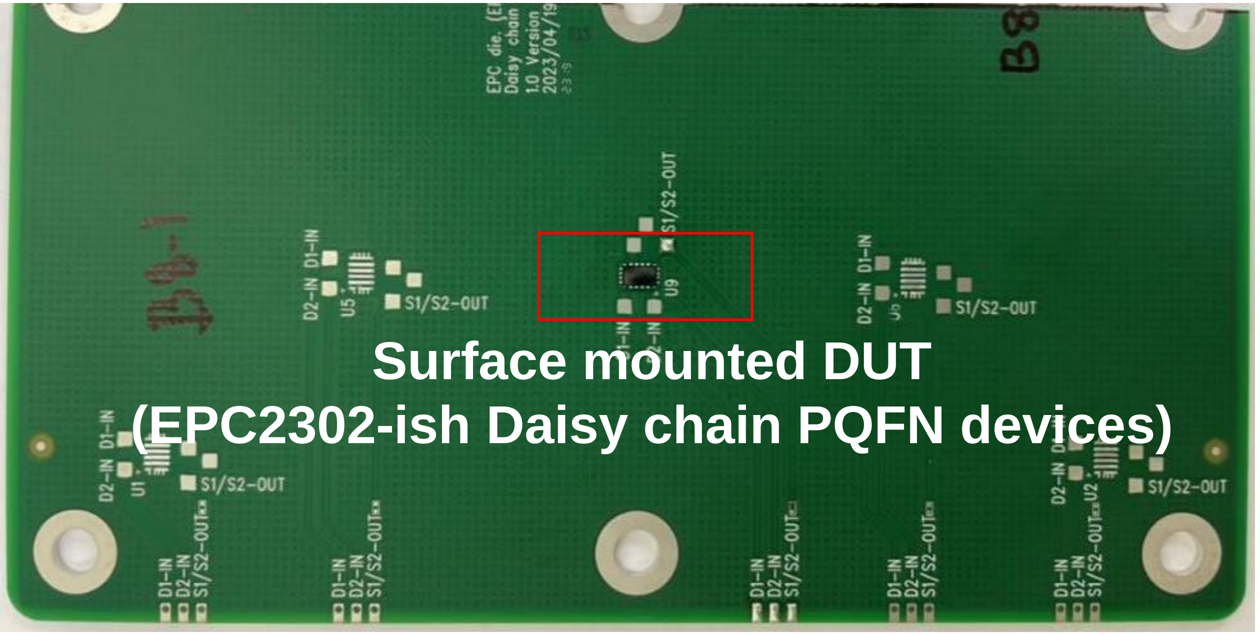


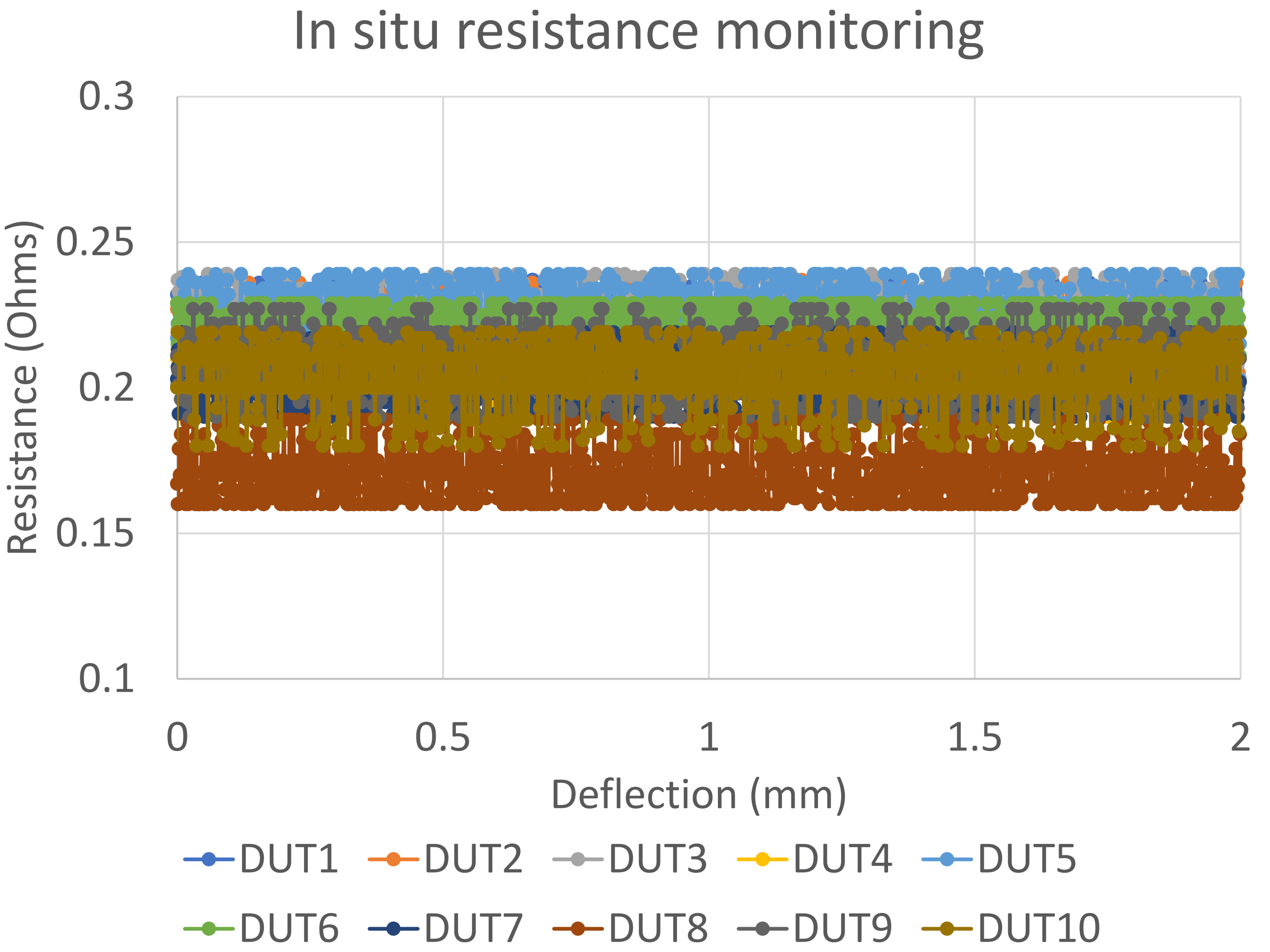
Figure 9 – Bending Test Set-up acc. IEC 60068-2-21 with additional Notation



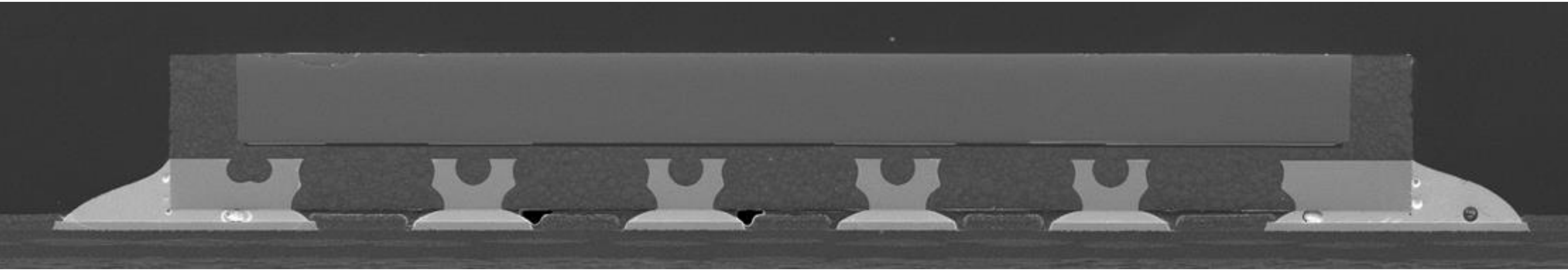
Surface mounted DUT
(EPC2302-ish Daisy chain PQFN devices)

Bending Test Results

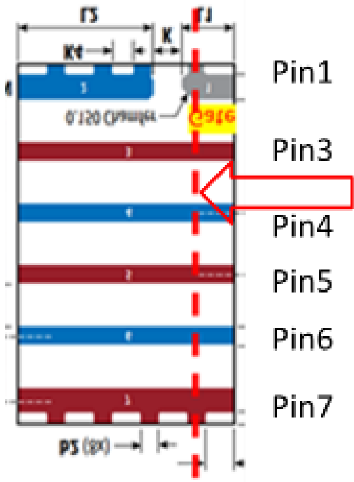
No observable resistance shift was found to 2 mm bending



Bending Test Results:
Cross-section Results post 2 mm Max Bending



No solder joint cracking observed!



Conclusions

- Gates have very near-zero failure rate when the bias is kept at or below the max rated voltage (6V).
- GaN devices are projected to have less than 10% shift over 25 years of continuous operation at 80 V bus voltage, 100 kHz.
- Underfilled CSP GaN devices showed excellent temperature cycling capability.
- A methodology is given to estimate TC lifetime in a real-world application for a variety of device sizes.
- GaN FETs demonstrate extreme robustness under short circuit testing.
- PQFN GaN devices also show good mechanical robustness when subjected to board bending stress.

Thank you!

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