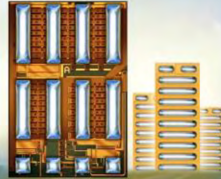
The eGaN® Technology Journey Continues



eGaN器件的栅极失效机理和动态导通电阻的物理模型

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Thank you for joining us today.
非常感谢您参加我们今天举行的线上研讨会。

In this webinar we will explain how physics-based models of eGaN device gate failure mechanisms and of dynamic Rds(on) can be used to project the lifetime of an eGaN device over all voltages and temperature ranges
我们将与您分享氮化镓eGaN器件的栅极失效机理和动态导通电阻$R_{DS(on)}$的物理模型，可以用来预测器件在整个电压和温度范围内的使用寿命。

对芯片及封装进行应力测试
Die and Package Stress Tests

RELIABILITY REPORT | Phase Twelve Testing

EPC eGaN® Device Reliability Testing: Phase 12

Before we get started, I just want to give an overview of EPC's test-to-fail methodology.
在开始介绍物理模型之前，我想分享一下，EPC公司对器件进行的反复测试、直至器件发生故障的方法。

Today, the semiconductor industry tries to qualify devices by testing them at one data point, say for example, maximum temperature and maximum voltage.
半导体行业目前使用的方法，是在一个特定的测试点，确定器件的稳固性，例如在最高温度和最高电压下，测试器件的性能。

And then, making sure that no devices fail after a certain period of time, maybe a thousand hours. In doing that, you don't know when or why devices fail.
然后，在若干时间后，例如器件在工作1000小时之后，确保它们没有发生故障。 如果这样测试，您不知道器件何时失效，或是为什么器件会失效。

So EPC has embarked on a very aggressive program to determine when and how our devices fail under all stress

conditions.
所以，EPC公司采用了要求甚高的测试方法，从而确定器件在经过各种应力测试后，是在何时及如何失效的。

And this table is a summary of that.
这里的图表总结了我们对器件进行测试后的结果。

(Build# 1) In the left-hand column, we have the stressors. They include voltage, current, current and voltage together, high rate of change in voltage and current, temperature, humidity, mechanical stress, thermo mechanical stresses, all the different ways that a device will experience stress.
左边的第一栏中，我们展示出各种应力测试的方法，包括电压、电流、电流和电压合并测试、电压/电流在大幅度改变下进行测试、温度、湿度、机械应力和热机械应力测试。这是器件会遇到的各种不同应力。

(Build#2) And from that, we found a large group of intrinsic failure mechanisms.
从这些测试结果，我们了解到各种固有的失效机理。

At times, what we had to do was stress devices well beyond the data sheet, in order to find that failure mechanism.
有的时候，我们需要对器件施加高于数据表所建议的参数，从而找出失效机理。

In the Phase 12 report, we report on several new mechanisms. (Build#3) And it's shown here on the right-hand column.
我们在第12阶段产品可靠性测试报告中，分享了几种全新的失效机理。这就是右边第二栏中所显示的各种失效机理。

The ones that are in green are the ones that are addressed in the Phase 12 report now available online at www.epc-co.com.
这里绿色所标示的，就是第12阶段测试报告所发布的，详细信息可从我们的网站www.epc-co.com找到。

The ones that have numbers on them are addressed in references at the end of the report, which are previous phase

reliability reports from EPC available on our website.
您在这里看到的编号，是代表第12阶段测试报告末端所提及、之前已经发布的可靠性测试报告编号，所有报告可以在我们的网站找到。

So, let's go ahead and look at one of the basic failure's mechanisms based on voltage stress on the gate to source.
现在，让我们看看从栅极至源极施加电压应力的测试，从而了解到其中一种基本的失效机理 。

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应力测试 – 电压
Stress – Voltage

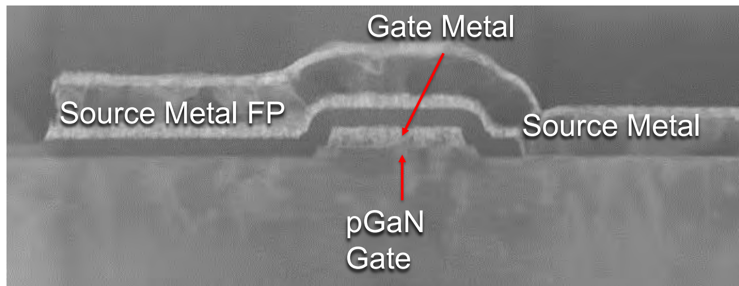
栅–源极
Gate-Source

Initially this was thought to be the simplest case and, the one with the most concrete answers to it. Over time, however, we found there were a few unanswered questions that needed more digging. That's what we will report on today.

一开始，大家以为这个应力测试是最简单的，和很容易找到器件为何失效的具体答案。

可是，我们逐渐地发现未能解答的几个问题，需要进一步探讨。 这就是我们今天要与您分享的报告内容。

栅-源极电压应力测试
Gate-Source Voltage Stress



To start off with, let's look at the structure of our gate to source in our eGaN transistors.
首先，让我们看看氮化镓（eGaN）晶体管栅极到源极的结构。

This is a scanning electron micrograph cross section, showing you where the various features of the device are.
这是扫描电子显微照片的横截面，您看到器件的各个部分。

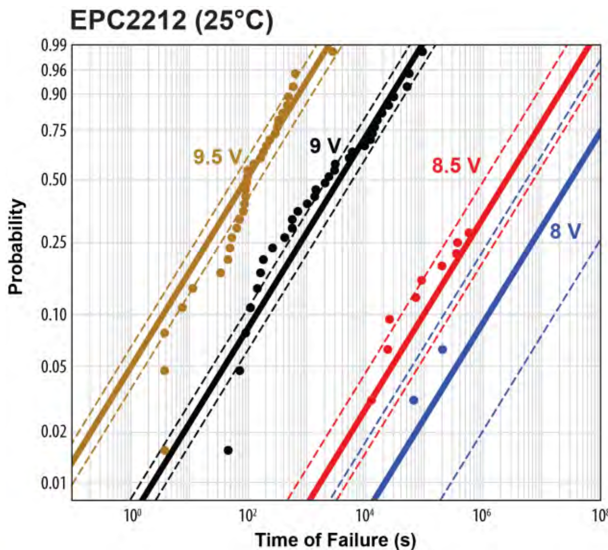
You can see the source metal, the gate metal, where the red arrow is pointing, the pGaN Gate, which is a gallium nitride doped with magnesium. It sits on top of a barrier, which is aluminum gallium nitride, which sits on top of gallium nitride.
您可以看到源极金属，和红色箭头指出的栅极金属，而pGaN栅极是掺杂了镁的氮化镓，它位于阻挡层的顶部。
阻挡层是氮化铝镓，位于氮化镓的顶部。

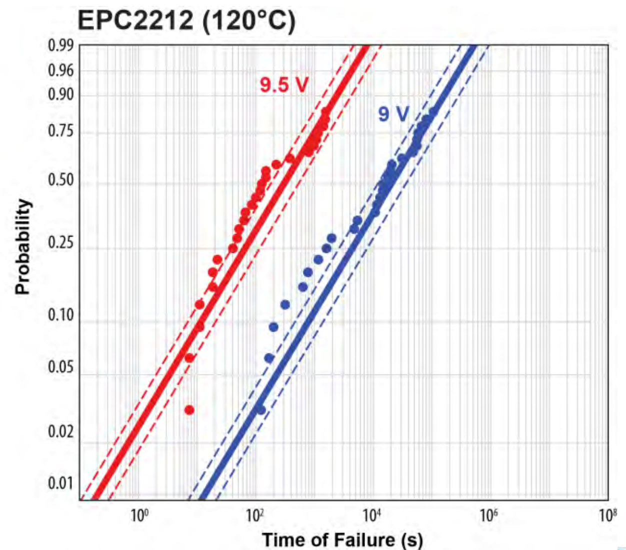
You will also notice the dark area between the source metal and the pGaN Gate, and this is silicon nitride.
您也可以看到，源金属和pGaN栅极之间的暗区，这是氮化硅。

Keep this cross section in mind. We will go back to it as we talk about failure mechanisms.
请记住这个横截面。 当我们讲解器件的失效机理时，将再提及它。

对栅极进行加速应力测试 - 分析
Gate Acceleration: Analysis

Data Sheet Maximum = 6 V_{GS}





So we took devices well beyond their data sheet to monitor how they fail.
我们可以用高于数据表提供的极限值来测试器件，从而可以监察器件如何失效。

The graph on the left shows the probability of a failure on the vertical axis. And on the horizontal axis, the time for that failure.
左图的Y轴展示器件的失效机率。而X轴是器件发生故障的时间。

We took groups of about 32 devices and we put bias at 8 volts, 8.5 volts, 9 volts and 9.5 volts.
我们测试了大约32个器件，对器件施加8 V、8.5 V、9 V 和 9.5 V偏压。

And we measured exactly when that device exceeded the data sheet limits for the gate.
之后，测量器件的栅极在何时超过数据表所提供的偏压极限值。

And you can see, the first device failed at 9.5 volts after a little while, and then more and more devices failed at each voltage
您可以看到，第一个器件在很短时间内，在9.5 V时失效。而且有越来越多的器件陆续在各个测试电压点也相继失效。

And at 9.5 volts you can see that by the time we get to about 2,000 seconds all 32 divices failed.

而在施加9.5 V偏压、大约在2000秒后，32个器件全部失效。

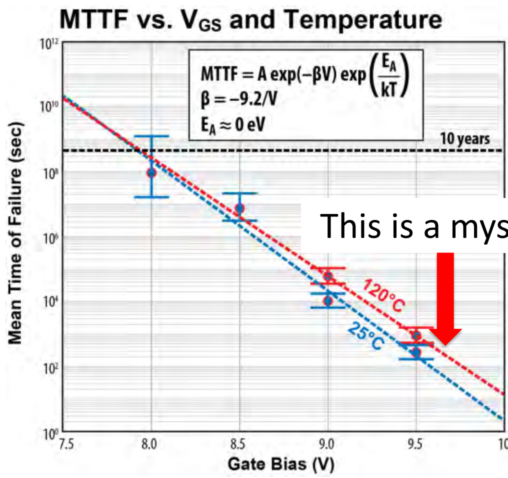
At this point in time, and with this applied DC voltage, the probability of failure is 100% or 1.0
这时，在施加的直流电压条件下，器件的失效机率是100%， 或是1.0。

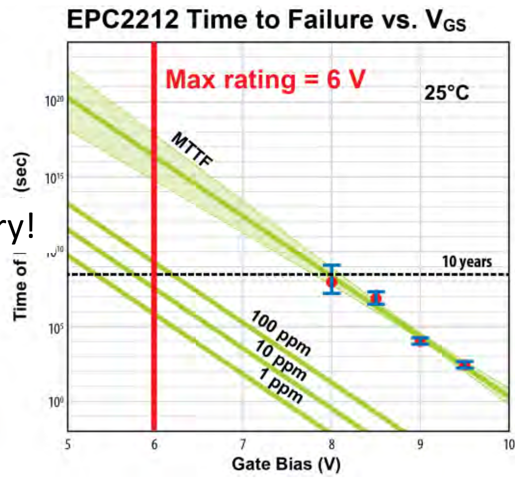
We did that same test at a higher temperature.
我们在更高的温度下，对器件进行相同的测试。

You can see that in the graph on the right where we did 9 volts and 9.5 volts
从右图您可以见到，我们在9 V及9.5 V对器件进行测试。

对栅极进行加速应力测试 – 器件的失效时间

Gate Acceleration: Time to Failure





From this, we can create these graphs. On the left-hand side, we show the mean time to failure for devices versus gate voltage at two different temperatures.
我们构建了两个图表。左图展示出在两个不同的温度下，器件的平均失效时间（MTTF）与栅极偏压的关系。

And on the right-hand side, we answer the question, what is the time to failure for a certain percentage of the devices versus gate bias?
对于部分器件，它的平均失效时间与栅极偏压的关系是什么？右图为您提供了答案。

In this case, we took the automotive qualified EPC2212 as a representative device.
本例子使用通过认证的车规级氮化镓器件EPC2212。

As you go to higher gate bias, the failure rate of course, increases, and the mean time to failure goes down.
当栅极偏压越高，失效率当然会更高，而平均失效时间将更短促。

On the right-hand side, we show that in terms of the percentage of failure.
在右图，我们展示出这个失效比率。

We drew a vertical red line to show the maximum rating of our devices, six

volts, and you can see the first diagonal green line that says one PPM, that’s a prediction when you'll see one part per million failures of our gates.
右图中的红色垂直线代表器件的最大额定电压为6 V。 第一条绿色的对角线是1 PPM，这是我们所预测的，一百万个器件中会有一个器件的栅极发生故障。

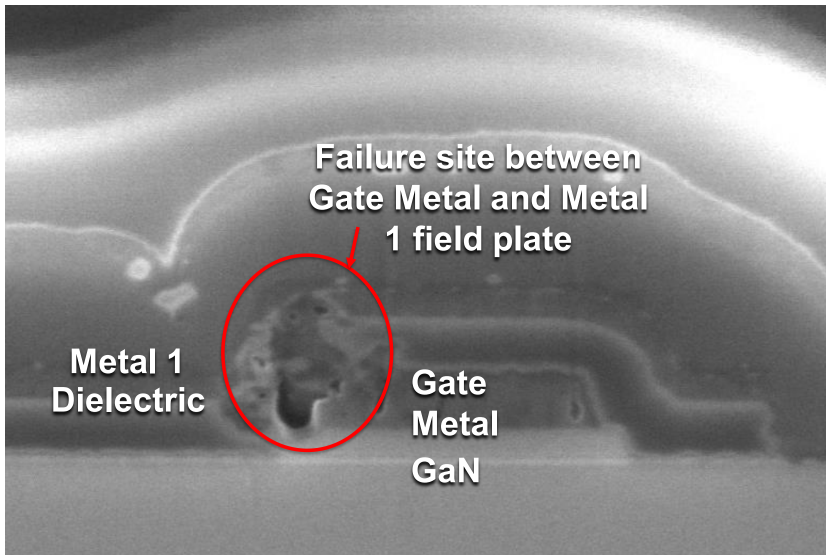
Now, if you follow that line up to the dotted line that says, 10 years, you'll see that at 10 years, we'd expect one part per million fail at approximately 5.25 volts on the gate.
现在看看，1 PPM线与10年时间的虚线的交汇点，这是我们预计在10年时，在大约是5.25 V的栅极电压时，一百万个器件之中会有一个器件的栅极发生故障。

So, if you put 5.25 volts, DC on our gate, and you waited 10 years, you'd see approximately one part per million failure based on this time dependent dielectric breakdown model.
所以，如果您在直流栅极施加5.25 V电压并等待十年，可以大约计算出，每一百万个器件之中，会有一个器件失效，这是基于这个随时间而变化的介电击穿模型。

The graph on the left shows the MTTF vs temperature. Whereas there isn’t a large change with temperature, it does seem strange that the MTTF (build 1) actually goes up with temperature. Time dependent dielectric breakdown predicts a small degradation with temperature, not an improvement.
左图显示了器件的平均失效时间（MTTF）与温度的关系。 尽管温度没有很大的变化，奇怪的是，器件的平均失效时间实际上随着温度上升而延长。理论上，随时间变化的介电击穿模型预测，当温度升高，器件会更快一点损坏。

氮化镓器件的栅极没有失效
Gate Failures Not in GaN

EFFICIENT POWER CONVERSION



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When we did fail devices, again, by going way beyond the data sheet limits, this is what we saw.
当器件发生故障，并超过数据表所提供的极限值，我们会看到这个情况。

You can see a cross-section of the gate, the gate metal began underneath it, the metal field plate and the dielectric between the metal field plate and the gate metal, and that's where the failure occurred.
这里您可以看到栅极的截面图。从底部开始是栅极的金属层，上面是金属场板，以及在金属场板与栅极金属中间的电介质－这就是发生故障的部分。

In fact, all the devices failed in this manner, sometimes on the left side of the gate sometimes on the right.
实际上，所有器件的失效机理都是这样的，有的时候是在栅极的左边，有的时候是在栅极的右边。

While this initial lifetime study provided a solid phenomenological model of gate reliability in eGaN FETs, many fundamental questions remained unanswered:

尽管这项初期的器件寿命研究为eGaN FET栅极的可靠性提供了优越的现象模型，但是很多基本问题仍未能解答：

- Why does dielectric rupture occur in a high-quality silicon nitride film at an electric field well below its breakdown strength? And, why does this rupture occur at the corner of the gate?
- 为什么高质量的氮化硅薄膜在远低于其击穿强度的电场下，会发生介电破裂？ 为什么在栅极的拐角处发生这种破裂情况？

- Why does gate lifetime increase as temperature rises?
- 为什么随着温度升高，栅极的寿命会更长？

- Is the simple exponential scaling of MTTF with gate voltage truly applicable to eGaN FETs? Is there perhaps a different model that is predicated on the root physics of failure in GaN?
- 用栅极电压对MTTF进行简单的指数缩放是否真的适用于eGaN FET？是否有可能有别的模型是基于氮化镓器件的失效物理原理？

碰撞电离机理
Impact Ionization Mechanism

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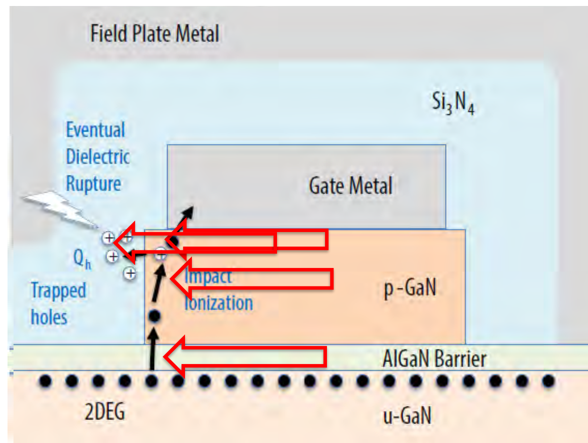

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As a result of these collective observations, EPC theorized that a multi-step process was responsible for gate failure at high V_{GS}.

从以上观察所得，EPC的理论是，在高VGS栅-源极电压时，多步工艺是导致器件失效的原因。

This process is shown schematically here (build 1).

让我们看看这个工艺的示意图。

In the first step, electrons are injected into the p-GaN gate layer from the 2DEG. They are injected via tunneling or thermionic emission over the AlGaN hetero-barrier.

第一步，将电子从2DEG注入p-GaN的栅极层。 它们通过隧穿或热电子发射方式，注入AlGaN异质势垒之上。

Once inside the p-GaN layer, the electrons gain energy rapidly from the electric field (build 2), with some gaining sufficient energy to cause impact

ionization (build 3).

一旦进入p-GaN层，电子就会从电场中迅速获得能量，当中一些电子会获得足够的能量以引起碰撞电离。

This leads to the generation of electron-hole pairs, particularly in the high field region just under the gate metal .

这会产生电子空穴对，特别是在栅极金属层下方的高电场区域。

In the second step of this process, holes move away from the gate metal under the influence of the field.

第二步是在电场的影响下，空穴从栅极金属移开。

Near the sidewall of the gate, a certain fraction of holes scatter into the Si_3N_4 dielectric, where they become trapped in deep states (build4) . This process is aided by the fact that the Si_3N_4/GaN interface has a Type II staggered band alignment whereby the valence band maximum in Si_3N_4 is higher than in GaN. This means holes generated in GaN near the interface have no (or low) barrier for emission into the dielectric.

在栅极侧壁附近，部分空穴会扩散到Si_3N_4电介质中，并深陷其中。Si_3N_4/GaN界面采用Type II 交错式带宽对齐，Si_3N_4中的价带最大值，会高于GaN的价带最大值。 这意味着在GaN界面附近产生的空穴，没有（或低）势垒，阻碍电子发射到电介质中。

In the final step of this process, holes become trapped in the dielectric, leading to a growing positive charge density Q_h. This charge, in turn, leads to an increasing electric field in the dielectric between the metal field plate and gate metal in the vicinity of the gate sidewall. Once this charge density reaches a critical density (Q_c), the dielectric ruptures, leading to the kind of catastrophic damage near the sidewall observed in failure analyses of gate failures.

最后一步，空穴被困在电介质中，导致正电荷密度Qh增大。该电荷导致金属场板和栅极侧壁附近的栅极金属之间的电介质中的电场增加。 一旦电荷密度达到临界密度（Qc），电介质就会破裂，从而导致侧壁附近发生灾难性损坏，这是栅极故障分析所提到的。

开发碰撞电离模型
Impact Ionization Model Development

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q}$$

$$\alpha_n = a_n e^{-(b_n/F)^m}$$

Ref	a_n(1/cm)	b_n(V/cm)	m
Ji et al.[12]	2.10E+09	3.70E+07	1
Ozbek [13]	9.20E+05	1.70E+07	1
Cao et al. [8]	4.48E+08	3.40E+07	1
Ooi et al. [15]	7.32E+07	7.16E+06	1.9

$$a_n(T) = a_{n;0}(1 - c\Delta T)$$

$c = 6.5x10^{-3}$ K^{-1}

$G \approx \alpha_n \frac{|J_n|}{q}$ $J_n >> J_p$ $MTTF \propto \frac{Q_c}{G}$

$$MTTF \propto \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{qQ_c}{J_n a_{n,0}(1-c\Delta T)} exp\left[\left(\frac{b_n}{F}\right)^m\right]$$

$$MTTF = \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V+V_0}\right)^m\right]$$

$m = 1.9$
$V_0 = 1.0$ V
$B = 57.0$ V
$A = 1.7x10^{-6}$ s
$c = 6.5x10^{-3}$ K^{-1}

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And we can calculate all of these mechanisms using basic physics and data supplied from academic research papers.

我们可以使用基本物理学和学术研究论文提供的数据，计算出所有失效机理。

Shown here are these calculations and (build 1) highlighted is the resulting new equation for predicting the lifetime of eGaN device gates under all voltage and temperature conditions.

这里显示的，是这些计算程式，红色框图内，显示了由此产生的新方程式，用于预测eGaN器件栅极在所有电压和温度工作条件下的寿命。

To the right of this equation are the variables that were used in the model that come from prior academic research.

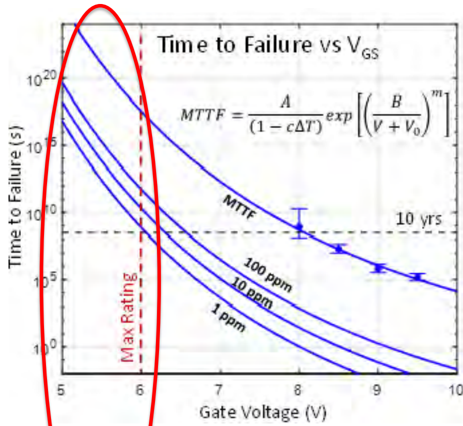
这个新方程式的右边，是模型中使用的变量，这些变量来自先前的学术研究。

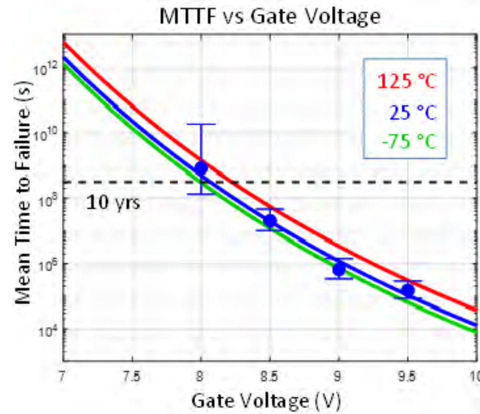
Now let's see how well this explains the experimental data.

现在让我们看看，它可否清楚解析实验数据。

理论与实验结果的比较

Theory vs. Experimental Results





$$MTTF(V_{GS}, \Delta T) = \frac{A}{(1 - c\Delta T)} exp\left[\left(\frac{B}{V_{GS} + V_0}\right)^m\right]$$

$m = 1.9$
$V_0 = 1.0$ V
$B = 57.0$ V
$A = 1.7 \times 10^{-6}$ s
$c = 6.5 \times 10^{-3}$ K^{-1}

(Build 1) Using the equation we just developed we can compare against our experimental results.

我们可以把刚刚谈过的方程式，与实验结果进行比较。

(Build 2) Here we show the measured EPC2212 mean time to failure vs. gate to source voltage, at 25° C for four different voltage legs.

这里显示了在25° C、4个不同的电压值下，测量出EPC2212器件的平均失效时间和栅极至源极电压的关系。

The solid line corresponds to the impact ionization lifetime model. Extrapolations of time to failure for 100 ppm, 10 ppm, and 1 ppm are shown as well.

实线代表碰撞电离寿命模型，这里也推断了100 ppm、10 ppm和1ppm的器件失效时间。

Note that the non-uniform acceleration with voltage of the model (build 3) matches the data well. This voltage acceleration appears as curved rather than linear when viewed in log-linear space.

请注意，加速与模型电压不一致，与数据非常吻合。 从对数线性空间来看，该电压加速为曲线，而不是线性。

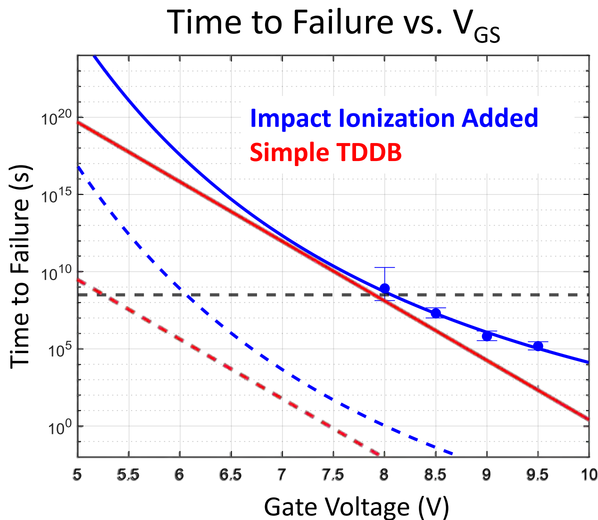
This new model provides a better fit to measurement, wherein the voltage acceleration is observed to decrease as gate to source voltage rises. The model also predicts the negative temperature coefficient (build 4) as can be seen in this graph.

这个新模型与测量数据更匹配，电压加速会j随着栅极至源极电压的上升而减慢。 从这里的图形看到，这个模型也可以预测到负温度系数。

TDDB与碰撞电离模型的比较

TDDB vs. Impact Ionization Models

EFFICIENT POWER CONVERSION



Here is a comparison of the impact ionization model and the simple time dependent dielectric breakdown model previously reported. Included is the extensive experimental data showing the reasonable fit.

这里是比较碰撞电离模型，和早前报道的简单且随时间而变化的介电击穿模型，包含大量实验数据支持结论。

This implication is that parts are even more reliable at lower voltages than reported previously. Instead on 1 PPM projected failure rate after 10 years at 5.25 V DC, we now believe we should see about 1 PPM failure rate at 6 V DC after 10 years.

相比之前报道的，在较低的电压时，元件像是更加可靠。与之前预计在10年后、5.25 V DC下发生的1 PPM器件失效率不一样，我们现在预测1 PPM会于10年后、6 V DC下发生。

This is supported by the fact that we have yet to have a field failure due to gate failure.

如何证明这一点？从现场没有发现任何器件故障是由栅极损坏所引致的， 就证明了这一点。

应力测试 – 电压

Stress – Voltage

漏–源极

Drain-Source

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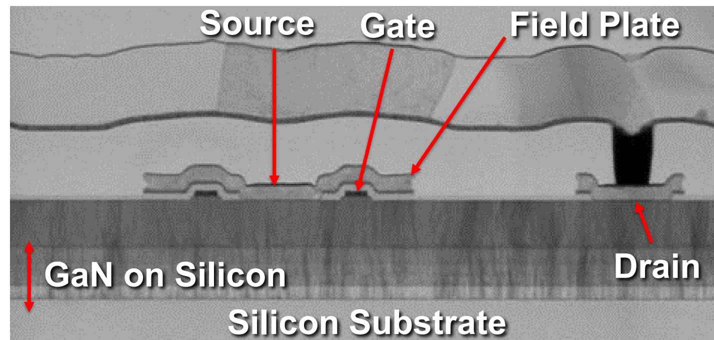
Now let's take that case and let's go to one that's more complicated and one that certainly has had a lot more discussion in the industry, and that's drain source voltage stress.

现在，让我们看看更复杂、业界讨论更多的测试方法 – 漏极至源极电压应力测试。

漏-源极电压应力测试
Drain-Source Voltage Stress



And we'll start off again with the cross-section, and this is what a device looks like.
让我们再由截面图开始解析，这里的图片看到器件的样子。

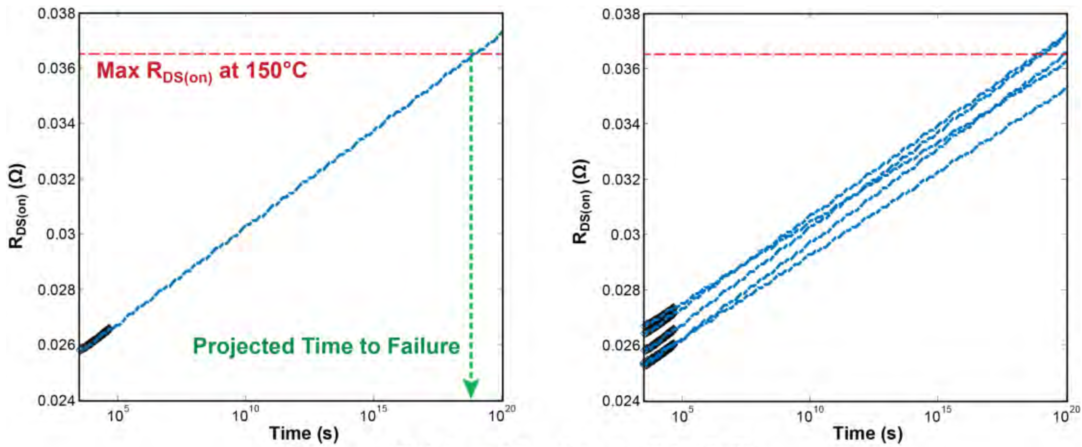
For each and every different device cross-section, we need to do these tests to establish the failure mechanisms and make sure that we're seeing a single failure mechanism.
我们对每个不同器件的横截面进行应力测试，从而确立各种失效机理，以及确定主要失效机理。

We have done that, and we do see a single primary failure mechanism from drain source voltage.
完成测试后，从漏极到源极电压，我们找出主要失效机理。

导通电阻随时间而变化的特性

Characterizing $R_{DS(on)}$ Shift in Time

120 V overstress at 150°C (100 V Rated Device)



$$R(t) = R_0 (\alpha + \beta \ln[t])$$

And the mechanism is something called dynamic RDSon.
这个机理叫动态导通电阻$RDS_{(on)}$

And this is what it looks like when you measure the on resistance of a device versus time.
这里可以看到，器件的导通电阻与时间的关系。

On the left-hand side, it's just one single device, and we've measured it as time goes on. This test is being done at 120 volts, and 150 degrees C on a 100 volt rated device.
在左图，我们测量单个器件，它随时间而变化的导通电阻。我们对100 V 器件在120 V 和摄氏150度下进行测试。

Now, we've tested many, many of these devices, and you'll see on the right-hand side, a larger population showing that there's some variation from device to device.
在右图，我们对很多器件进行了测试，并发现测试大量器件后，每个器件所得结果不一样。

But by measuring these devices, we have noted that we can extrapolate out the rate of increase in on resistance, that blue line, because it's quite a straight line on a log plot.
从测试这些器件后发现，可以推算导通电阻的上升幅度，由这里的蓝色线代表，其对数图差不多是一条直线。

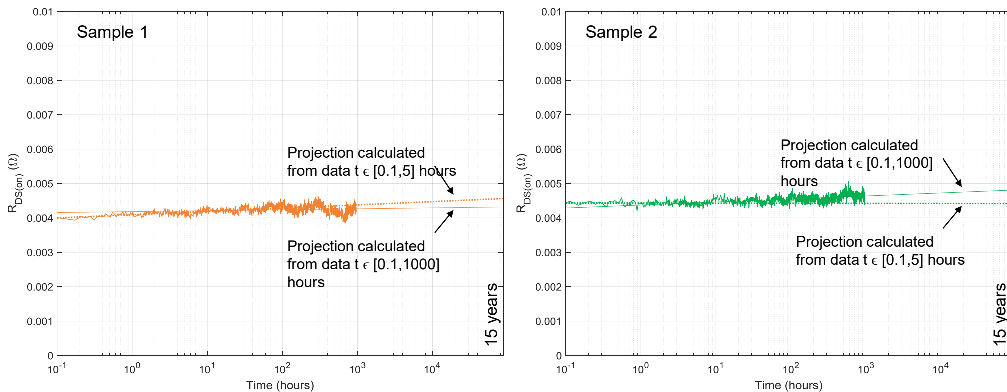
And when it crosses the datasheet limit, the red line, that's when we call it a failure.
当蓝色线越过数据表提供的极限值时，这里由红色线代表， 就是器件发生故障的时间。

So as in all these initial tests we looked at failure as being something that is no longer meeting data sheet limits.
跟所有初步测试一样，我们认为器件失效，就是超过数据表内的极限值的时间。

So this is much worse than you would see on a normal device under normal conditions.
这比正常器件在正常工作条件下，情况是差很多的。

预测导通电阻的分析

$R_{DS(on)}$ Projection Analysis



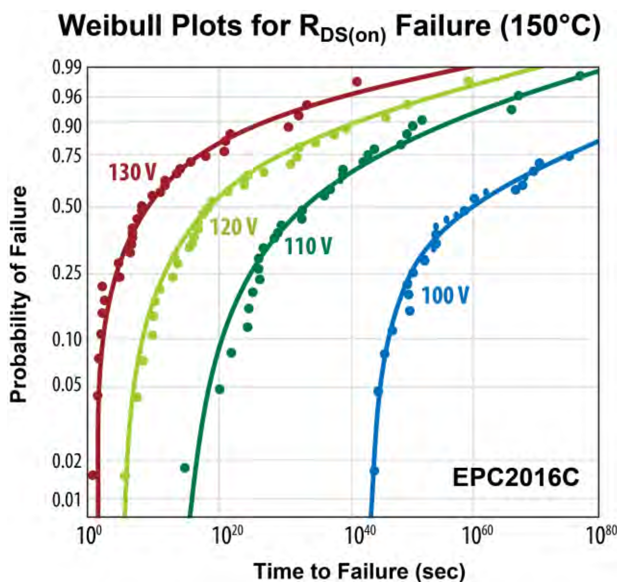
We frequently are asked if our long-term projections are a valid extrapolation from relatively short tests of around 48 or less hours.

我们经常被问到，长期预测是否根据大约48小时或更短的时间内，测试得出的有效推断？

Here are the $R_{DS(on)}$ projection generated with the first 5 hours ($t_{0\text{-}5h}$) of the test compared with the projection after 1000 hours. The errors are +/-10%, and even these small errors in the projection may be influenced by ambient temperature fluctuations during $t_{0\text{-}5h}$. These fluctuations tend to average out over long periods of time.

这里的测试，比较了首5小时（$t_{0\text{-}5h}$）和1000小时后器件的导通电阻$R_{DS(on)}$。误差为+/- 10％。误差虽然小，也可能会受到在首5小时期间的环境温度波动的影响。 这些波动通常在很长的时间内减少。

对漏极进行应力测试 - Weibull分布计算出平均失效率
Drain Stress Weibull Fits



So once again, we took a bunch of devices, in this case, the 100 V EPC2016C, and we're measuring the probability of failure on the vertical axis, the time to failure and the horizontal axis.
我们再对多些器件进行测试，这次是测试100 V的EPC2016C。Y轴是失效机率， 而X轴是器件的失效时间。

And we did it at the rated voltage, 100 volts.
我们在额定电压100 V下进行测试。

And then we also did it well beyond the datasheet limit, all the way up to 130 volts.
我们也在高于数据表的极限值下，从100 V至130 V测试器件。

And you'll see that by extrapolating to when these devices will cross the data sheet, we can create a time to fail.
你可以看到，我们推算器件在何时会超过数据表的极限值时，就得出器件的失效时间。

And that's when we put the dot on this curve.
这就形成一个时间点，从而构成图中的曲线。

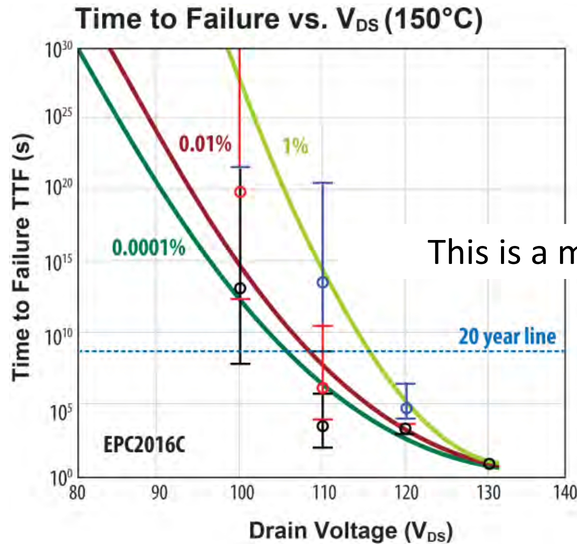
Now, when you're at 130 volts, the devices exceed data sheet limits quickly.
当您在130 V时，器件很快就超过了数据表的极限值。

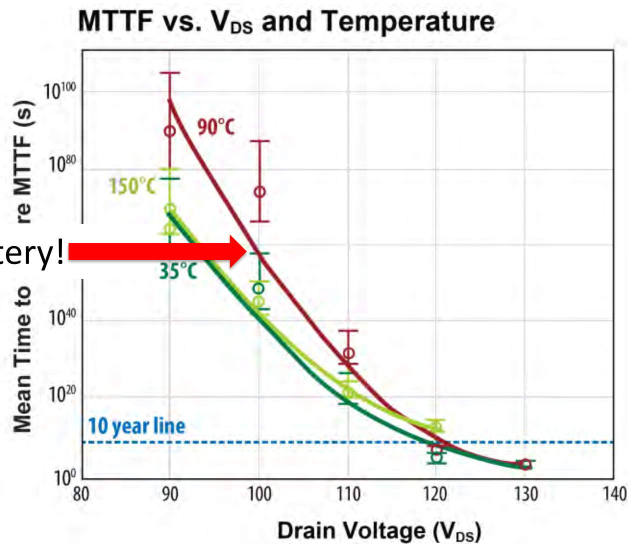
So you can measure the actual time it crosses the data sheet.
因此，您可以测量出器件超过数据表的极限值的实际时间。

When you're at 100 volts, you have to extrapolate when you predict it will cross the data sheet.
当您在100 V时，您需要推算器件在何时超越数据表的极限值的时间。

器件的稳固性与 V_{DS} 的关系

Device Robustness vs. V_{DS}





Those graphs can be translated into this. On the left-hand side, you have the time to failure for various percentage failure rates.
之前的几个图表，可转化为这里的图表。左图展示在不同百分比的失效率，器件的失效时间。

So point zero zero zero 1%, that's one part per million.
如果是0.0001%，这代表一百万份之一个器件。

And 1%, of course, you know, what that is and we also draw a 20 year line on this one.
您也必定理解1% 。我们也绘画出20年的蓝色虚线。

And you can see at the one hundred volt rating of the EPC2016C, we would expect that the devices would see less than one part per million failure in far more than 20 years, hundreds of years actually. However, if you look at the error bars, you'll see the error bar dips under the 20 year line to a little bit to a little less than 10 years.
您可以看到，100 V的EPC2016C在远远超过20年时间，其实是几百年，它们的失效机率是一百万分之一个器件会失效。可是，看看误差线，它们在20年线之下、稍微低于10年线之下。

And that's the 90% probability line.
这就是90% 机率线。

So with 90% probability, we can say you should see about one part per million failures at 100 volts, DC bias in about 10 years.

90%机率代表在100 V、直流偏压下、于大约10年时间，其失效机率将是一百万份之一个器件会失效。

But on the right-hand side, there's a mystery.
可是，右图展示出一个不可思议的情况。

If you look at the drain voltage on the horizontal axis and the mean time to failure on the vertical axis, this is showing the rate of failure versus temperature.
从X轴的漏极电压，和Y轴的器件平均失效时间可以看到，失效率与温度的关系。

(Build #1) Note that the 90 degrees C line is above the 150 C line and the 35 degrees C line.
请注意，摄氏90度的曲线是在摄氏150度及35度曲线之上。

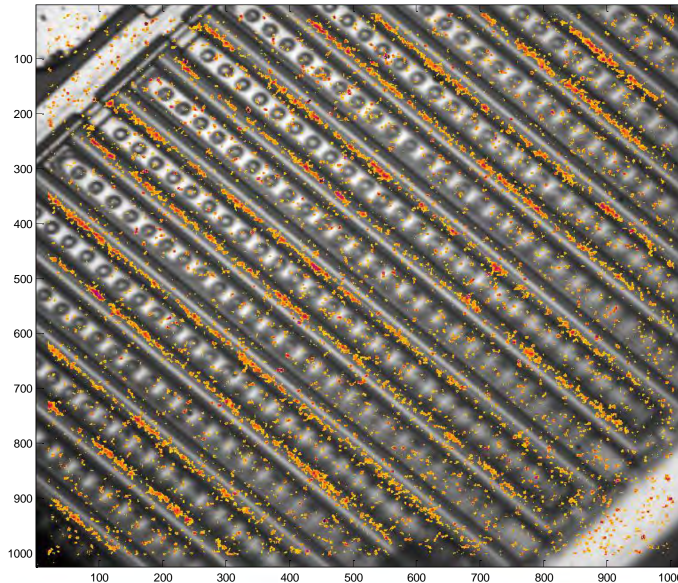
In other words, at 90 degrees C, the time to failure is much longer than at lower temperatures or at higher temperatures.
这是说，相比低于及高于摄氏90度的温度条件下，器件在摄氏90度时的失效时间大幅延长了。

We didn't understand that for several years, and that's a mystery that I want to solve today for you.
在多年以来，大家都不了解这个不可思议的情况，就让我们今天为您解答。

导通电阻变化的物理学 – 发射热载流子

Physics of $R_{DS(on)}$ Shift – Hot Carrier Emission

EPC EFFICIENT POWER CONVERSION



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To begin to solve this mystery, let’s look at what we think is the mechanism of failure.
让我们开始解释这个不可思议的现象。首先，让我们看看，什么是器件的失效机理。

It's well documented that you can generate hot carriers in gallium nitride when electrons are exposed to high electric fields.
很多文章详细描述，当电子处于高电场时，氮化镓可以产生热载流子。

These electrons get accelerated to a high energy, and it's high enough that they can actually penetrate layers in the device and get trapped.
这些电子加速成为高能量，能量在足够高时可以穿透器件层而被捕获。

This image is an actual photograph of the photons emitted by hot carriers as they get trapped in a generation 4 eGaN device.
这个图像是热载流子所发射出的光子的照相，这些光子在第四代氮化镓（eGaN)器件被捕获。

And we can zoom in on that. (Build#1)
让我们放大来看看。

And you can see here, each of the electrons emit a photon as they get trapped and we imaged that light in this photograph.

您可以看到，每个电子发射的光子被捕获，我们在这照片把这些光制成这个图像。

We've also overlaid the mask design so we can tell exactly where those electrons are and where they're getting trapped.
我们加入屏蔽设计，从而知道这些电子真正在哪里，以及它们在哪里被捕获。

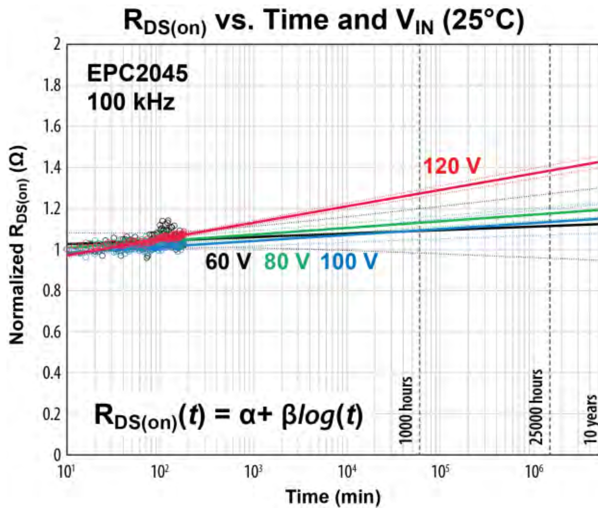
And it turns out it's the point of highest electric field in the device.
结果是在器件的最高电场。

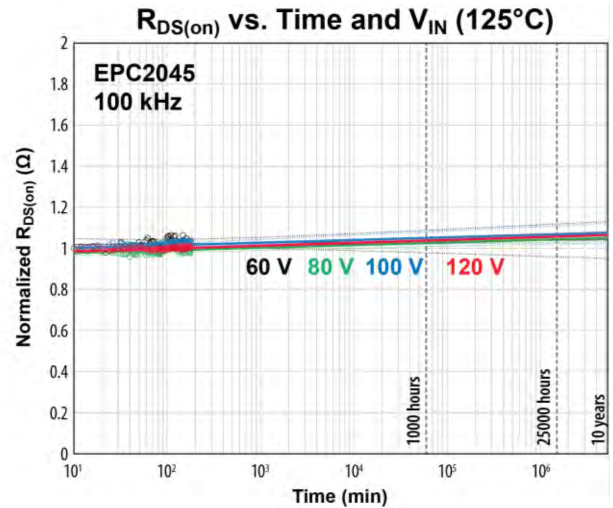
With this imaging tool we could actually modulate the voltage on the device and see when the hot carriers come in and when they don’t.
用了这个制图工具，我们就可以调节施加在器件上的电压，从而看到热载流子何时进入及何时没有进入。

Based on that, we designed our new fifth generation devices.
基于以上所说的，我们设计出第五代器件。

So, they would be much less susceptible to hot carrier injection induced dynamic RDSON
第五代器件受到注入的热载流子引致的动态导通电阻的影响会较少。

硬开关：输入电压的影响
Hard-Switching: Effect of V_{IN}





But let's go back to the story that we had a minute ago where we apply DC bias on devices in a test called high-temperature reverse bias, or HTRB, and let them sit for thousands of hours and measure the increase in on resistance.
之前一分钟刚刚谈过，器件施加直流偏压的测试，称为高温反向偏压测试，或者称为HTRB。测试器件在数千小时后，它的电阻。

Now, when you heat up a device with just DC bias on it, all you have is a leakage current, and that may be just a few micro amps of electrons that are available to be trapped.
现在，只施加直流偏置电压并对器件加热后，只有漏电流和被可以捕获到的数微安的电流。

Well, these graphs are actually a very different kind of a test. In order to make sure that we can really understand failures from hot carriers, we wanted to generate as many hot carriers as we can and cause devices to fail quickly.
这些图表其实展示出一种非常不一样的测试结果。为着真正了解热载流子如何引致器件失效，我们希望产生最多的热载流子，使得器件快速失效。

We developed a circuit that actually generates millions and millions of a hot carriers by generating a 10 ampere current pulse at the voltage that you see on this graph. So instead of micro amps, you have 10 amps going through

the device at 60 volts, 80 volts, 100 volts, 120 volts.
图中可以看到，我们构建的电路，在各电压下，产生10 安培脉冲电流，从而产生数以百万计的热载流子。所以，器件在60 V、80 V、100 V及120 V时，有10安培电流，而不是数微安的电流。

And you can see that as you go up to higher voltages, you can actually start to see the on resistance increasing.
当电压更高时，您可以看到电阻开始上升。

The horizontal axis is time and the vertical axis is normalized Rdson normalized to 10 minutes to allow for thermal equilibrium.
X轴是时间。Y轴是归一化电阻，时间归一化为10分钟，实现热平衡。

The graph on the left is at 25 degrees C. (Build #1)
The graph on the right is at 125 C.
左图展示在温度为摄氏25度下。
右图是在温度为摄氏125度下。

And, here's the essence of the mystery.
这就是不可思议之处。

Why is it that the on resistance or dynamic on resistance is almost 0 at 125 C even as you go to 120 volts on a 100 volt device?
为什么当100 V器件在120 V、摄氏125度时，导通电阻或动态电阻差不多是零？

And yet at 25 C, you can see a significant change in on resistance when electrons are injected at 120 V.
但在摄氏25度时、在120 V注入电子，您可以看到电阻变化很大。

And the answer is that hot carriers, as you raise the temperature of a device, bounce around this thermally vibrating lattice and actually can't go as far before they lose their energy to the point where they can’t jump into a trap.
原因是当器件的温度上升，热载流子围绕格点作晶格振动，它走不远，并在损耗能量后，不能跳进陷阱。

So, hot carriers have less tendency to get trapped at higher temperatures.
所以，热载流子在更高的温度时，趋于更难被捕获。

Now we can solve that mystery.
现在，我们可以解释这个不可思议的情况。

Before we showed that at 90 degrees C devices failed less frequently under DC bias compared to either 35 or 150 degrees C
在直流偏置电压下，与摄氏35或150度的情况相比，器件在摄氏90度的失效率较低。

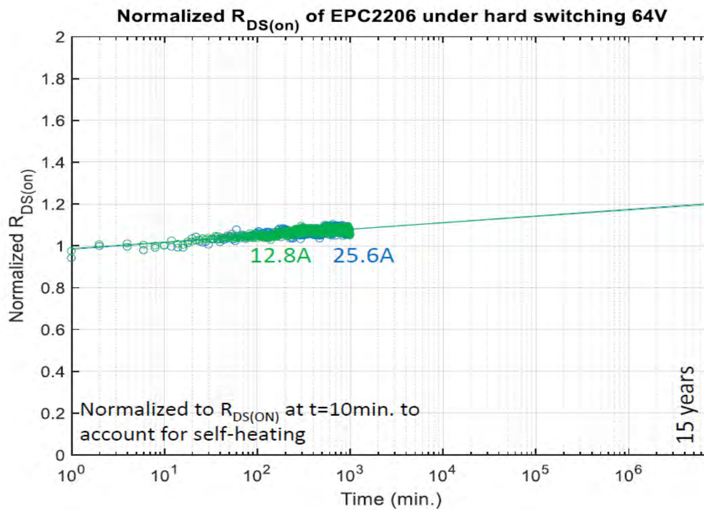
That's because there are two competing effects when you're doing HTRB.
这是由于在进行HTRB测试时，有两种相反的效应。

One effect is, as you go to higher temperatures, you generate more leakage current. The leakage current provides the supply of electrons that can get trapped.
第一种效应是当温度上提时，产生更大的漏电流。这个漏电流提供被捕获的电子。

The second effect is that the hot carriers can't travel as far. So it turns out that as you go to higher temperatures, the temperature effect keeping the hot carriers from getting trapped is more important until you get above 90 degrees C, in which case, you're getting more and more leakage current, so there's a higher number of candidates to get trapped.
第二种的效应是热载流子不可以走远。温度越高的效应，使得被捕获的热载流子更少，直至高于摄氏90度时，漏电流会越来越大，使得被捕获的电子会更多。

It also says that when we're doing traditional HTRB testing at maximum temperature and voltage, we're not testing the devices very well.
也有这样说，在最高温度及最高电压下，对器件进行传统的HTRB测试，并不是测量器件的最好方法。

开关电流的影响
Impact of Switched Current



How about the effect of switch current on dynamic $R_{DS(on)}$? Here we show two EPC2206 devices that were tested under resistive hard switching at 64 V and 200 kHz.

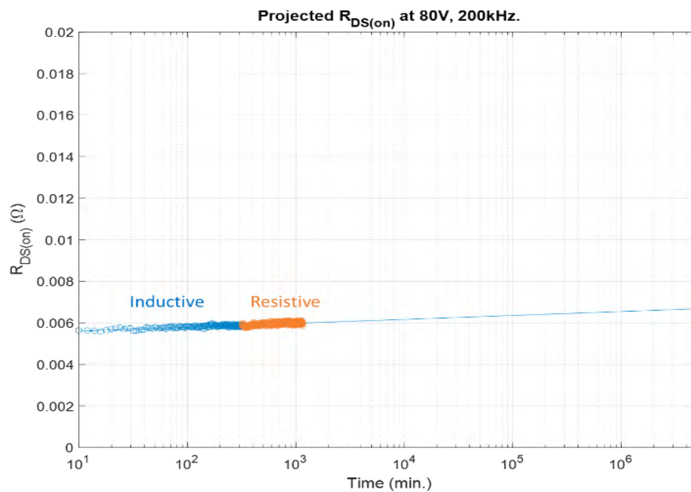
开关电流对动态RDS（on）的影响如何？ 在这里，我们展示了两个EPC2206器件，它们在64 V和200 kHz的电阻硬开关下进行了测试。

The switch current in one device was twice that in the other. No significant difference was found in either the slope or intercept of the log(t) growth characteristic. This indicates that the trapping effect has more than enough electrons to saturate.

一个器件的开关电流是另一个器件的开关电流的两倍。您看到Log（t）增加特性的斜率或截距，都没有发现显着的差异。 这表明捕获效应已经有足够多的电子，达至饱和。

电感与电阻开关的比较

Inductive vs. Resistive Switching



We often get asked about whether the resistive switching results would be the same as inductive switching. Here we have a comparison of inductive versus resistive hard switching on an EPC2204 FET switching at 80 V and 200 kHz.).

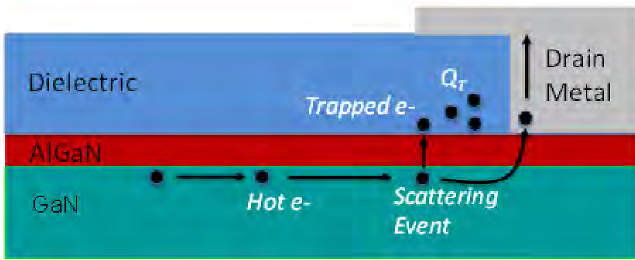
我们经常被问到，电阻开关结果与电感开关是否一样。 在这里，我们对在80 V和200 kHz开关的EPC2204器件的电感式和电阻式硬开关进行了比较。

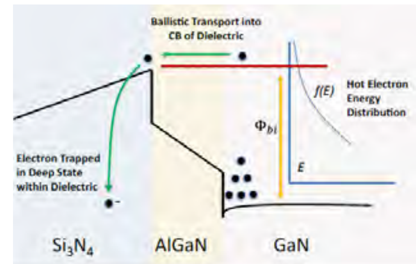
The same part was tested under inductive mode for the first four hours, followed by resistive mode for the next four hours. Both modes are essentially indistinguishable in terms of dynamic $R_{DS(on}$

在开始的四个小时内，在电感模式下测试了同一个器件，在接下来的四个小时内，测试电阻模式。 两种模式的动态导通电阻$R_{DS(on}$基本上是无法区分的。

热载流子捕获机理

Hot Carrier Trapping Mechanism





Here is a schematic diagram showing hot electron scattering into the surface dielectric near the drain contact. To enter this dielectric, electrons must have sufficient energy to surmount the potential barrier. Once in this dielectric, they fall into deep electron trap states and are trapped effectively indefinitely.

这是示意图，显示热电子散射到漏极触点附近的表面电介质中。 为了进入该电介质，电子必须具有足够的能量以克服势垒。 一旦进入该电介质，它们就会陷入深电子陷阱状态，并被无限期有效地捕获。

(Build 1) Now let's look at a band diagram showing band alignment vertically near the drain contact. A surface barrier exists for electrons to enter the conduction band of the Si_3N_4 surface dielectric.

在这里的能带图，看看接近漏极接触的垂直能带对齐。这里有表面势垒，用于电子进入Si_3N_4表面电介质的导带。

The overwhelming majority of channel electrons have insufficient kinetic energy to get over the barrier. (build 2) But a small percentage of hot electrons do have the energy and enter the insulator.

绝大多数通道电子的动能不足以通过势垒。 可是，一小部分的热电子可以有足够的能量，并且可以进入绝缘子。

As more electrons are trapped the surface electrostatic barrier has is enhanced as indicated by the arrow (build 3) and the dashed red lines.

随着更多的电子被捕获，表面静电势垒将增强，从图中的箭头和红色虚线看到。

热载流子捕获模型
Hot Carrier Trapping Model

$$f(E)dE \propto Ee^{-E/qF\lambda}dE \qquad \frac{dQ_S}{dt} = A\int_{\Phi_{bi}+\beta Q_S}^{\infty} f(E)dE = A\int_{\Phi_{bi}+\beta Q_S}^{\infty} Ee^{-E/qF\lambda}dE \qquad \frac{dQ_S}{dt} = B\exp\left(-\frac{\beta Q_S}{qF\lambda}\right)$$

$$Q_S(t) = \frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right) \qquad R(t) = R_0 + \frac{C}{Q_P - Q_S} = R_0 + \frac{C}{Q_P - \frac{qF\lambda}{\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)}$$

$$R(t) \approx R_0 + \frac{C}{Q_P}\left[1+\frac{qF\lambda}{Q_P\beta}\log\left(1+\frac{B\beta}{qF\lambda}t\right)\right] \qquad \tau_{LO} \propto exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \qquad \lambda = v_{th}\tau_{LO} \propto A\sqrt{kT}exp\left(\frac{\hbar\omega_{LO}}{kT}\right)$$

$$\frac{\Delta R}{R} = \frac{R(t)-R(0)}{R(0)} \approx a + bF\exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\sqrt{T}\log(t)$$

And here is the physics behind that mechanism for trapping electrons. This physics takes into account the change in on resistance that results from electrons jumping over the barrier to get permanently trapped in the silicon nitride layer.

这是捕获电子的机理背后的物理原理，它阐释因电子跳过势垒而永久地陷在氮化硅层中，使得导通电阻发生变化。

整体而言 – 热载流子捕获模型

Putting it All Together – Hot Carrier Trapping Model

$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF \exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\sqrt{T}\log(t)$$

$$= a + b\left[\frac{V_{DS}}{1 + exp[-\alpha(V_{DS} - V_{FD})]}\right]^2 exp\left(\frac{2\hbar\omega_{LO}}{kT_l}\right)\log(t)$$

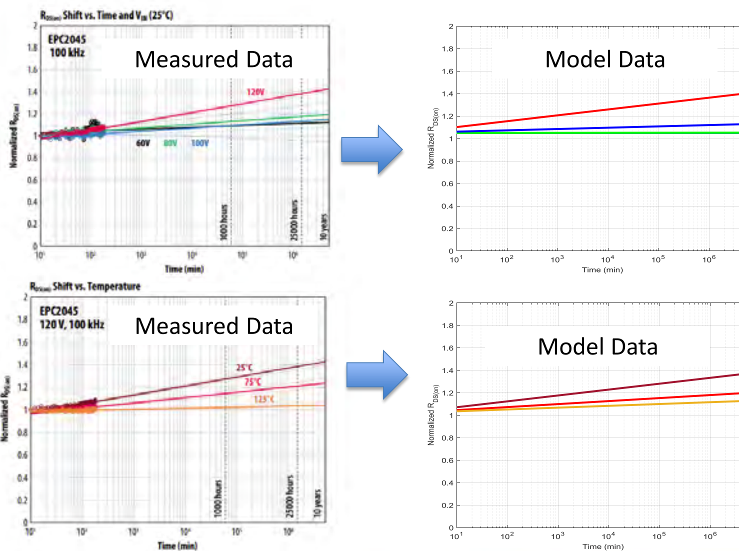
a = 0.02 (unitless)
b = 1.9E-8 (V^{-2})
$\hbar\omega_{LO}$= 60 meV
V_{FD} = 100V (appropriate for Gen5 100V products only)
α = 0.1 (V^{-1})
t = time in min

And here is the end of the calculation and the physical parameters that lead to the lifetime model for on resistance in eGaN devices. Let's now see how well this model fits the experimental data.

这是计算的结果，和eGaN器件的导通电阻寿命模型的物理参数。 现在，让我们看看，这个模型与实验数据的拟合度。

模型数据与测量数据的比较
Model vs Measurement

EFFICIENT POWER CONVERSION



Shown here is a comparison of measurement and model for EPC2045 operated at four different voltages and three different temperatures. The agreement is good to within measurement uncertainty.

这里比较了EPC2045的测量和模型数据，其工作在4种不同电压和三种不同温度下，并在测量不确定度之内，两者的数据拟合。

This demonstrates a good understanding of the mechanisms that cause on-resistance to change over time, temperature, and switching conditions.

这让我们了解，导致导通电阻随时间、温度和开关条件变化的机理。

All of the mysteries we know of have now been explained and the extraordinary reliability of eGaN devices is supported by the science.

我们已经解释到所有谜团，和科学支持eGaN器件的卓越可靠性。

现场测试结果
Field Results

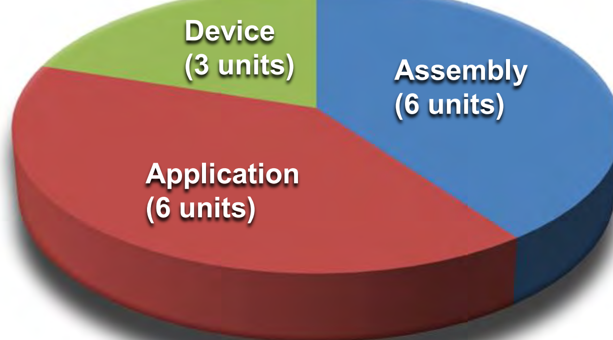
But all of this only matters if the customers get a good result, so let’s look at the experience we have gained after shipping tens of millions of devices over the last four years.

但是，只有在客户使用器件后取得良好结果，这一切才有意义。所以，我们想与您分享，在过去4年交付了数千万个器件后，所获得的经验。

氮化镓场效应晶体管的可靠性
eGaN FET Reliability

EPC EFFICIENT POWER CONVERSION

现场失效原因的分类
Field Failures by Category
1/1/2017– 12/31/2020



证实器件的高可靠性 – 从2017年1月1日起，通过了2,260亿器件-小时的现场测试，只有3个器件失效
Proven Reliability – 226 billion device hours in the field since January 1, 2017 with only 3 device failures

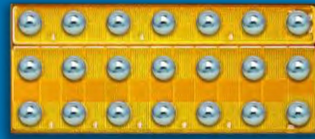
Power Conversion Technology Leader epc-co.com 27

As of this recording, we now have 226 billion device hours documented use in the field since January 2017 in our key automotive and telecommunications applications. And we have a total of three device units that have failed. These three device units failed for an extrinsic failure mechanism, a defect in the wafer fab, that has since been fixed. No MOSFET has ever come close to this level of field reliability.

自2017年1月以来，针对我们的主要车用及通信应用领域，记录了2,260亿器件-小时的现场可靠性测试结果，只有3个器件失效。其失效原因是与外部失效机理相关，这是晶圆制造厂的一个缺陷，之后都已经解决了。从来没有MOSFET器件可以实现这样高的现场可靠性。

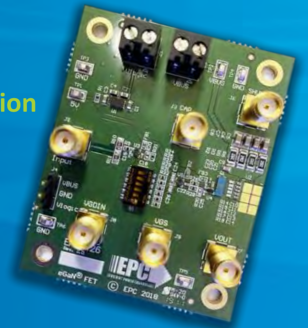
How To GaN Video Series

3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



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This webinar detailed just a few of the critical aspects of the recently published Phase 12 reliability report.
本次线上研讨会为大家讲解了第十二阶段产品可靠性测试报告的几个重要部分。

The full report is available on our website at epc-co.com.cn.
整份报告可以在我们的网站下载，网址是www.epc-co.com.cn。

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谢谢大家！