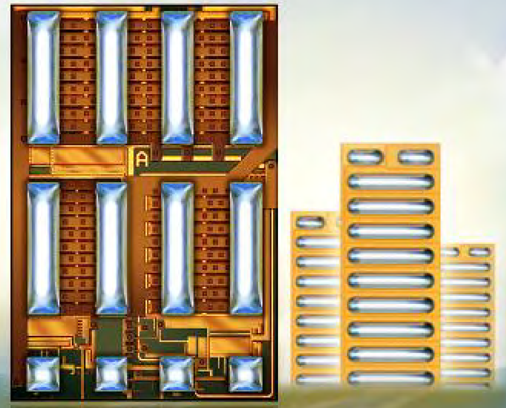
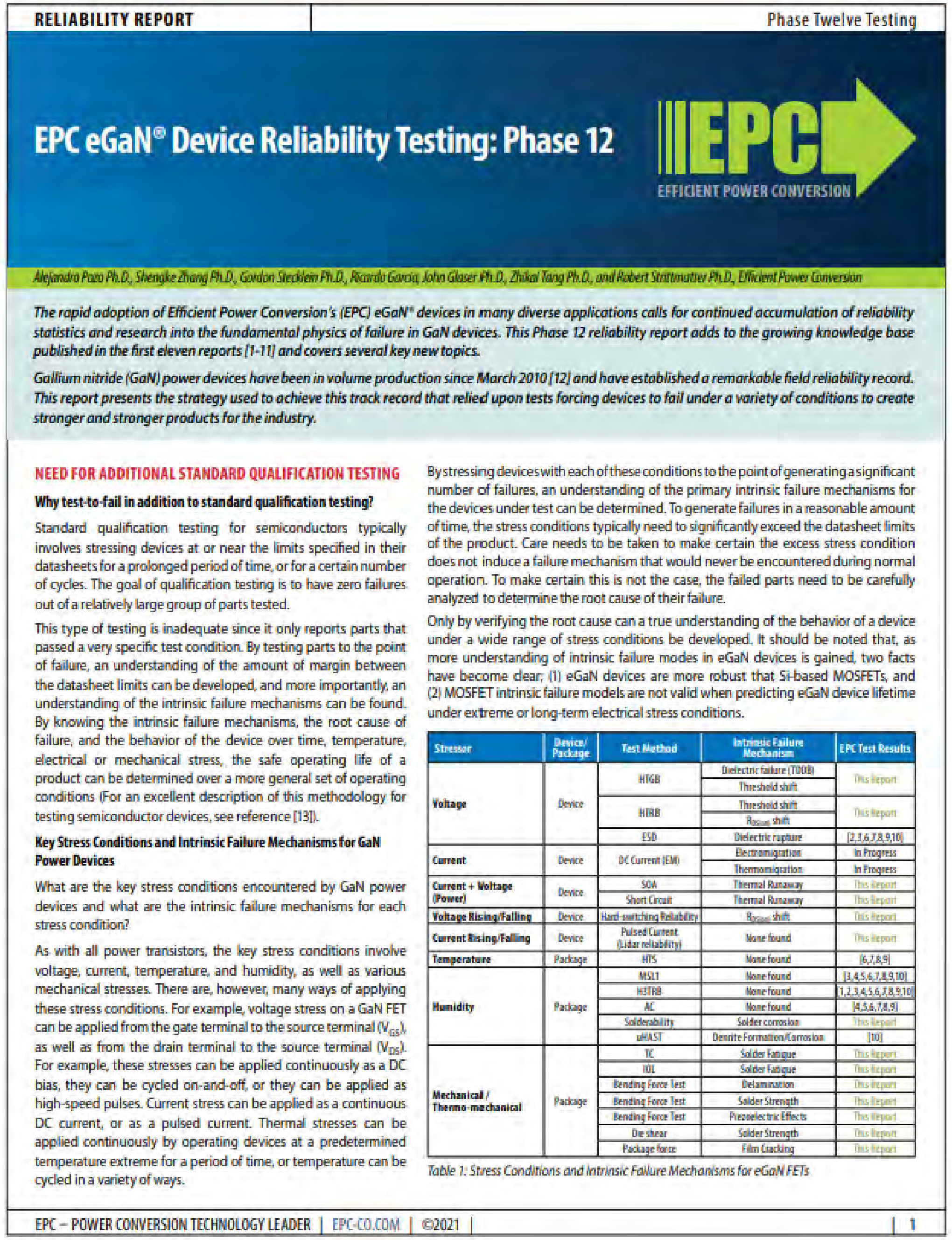
EPC
EFFICIENT POWER CONVERSION



Physics Based Model of eGaN Device Gate Failure Mechanism and Dynamic $R_{DS(on)}$

Alex Lidow, Ph.D.

Die and Package Stress Tests



EPC eGaN® Device Reliability Testing: Phase 12

Alejandro Pozo Ph.D., Shengke Zhang Ph.D., Gordon Stecklein Ph.D., Ricardo Garcia, John Glaser Ph.D., Zhikai Tang Ph.D., and Robert Strittmatter Ph.D., Efficient Power Conversion

The rapid adoption of Efficient Power Conversion's (EPC) eGaN® devices in many diverse applications calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices. This Phase 12 reliability report adds to the growing knowledge base published in the first eleven reports [1-11] and covers several key new topics.

Gallium nitride (GaN) power devices have been in volume production since March 2010 [12] and have established a remarkable field reliability record. This report presents the strategy used to achieve this track record that relied upon tests forcing devices to fail under a variety of conditions to create stronger and stronger products for the industry.

NEED FOR ADDITIONAL STANDARD QUALIFICATION TESTING

Why test-to-fail in addition to standard qualification testing?

Standard qualification testing for semiconductors typically involves stressing devices at or near the limits specified in their datasheets for a prolonged period of time, or for a certain number of cycles. The goal of qualification testing is to have zero failures out of a relatively large group of parts tested.

This type of testing is inadequate since it only reports parts that passed a very specific test condition. By testing parts to the point of failure, an understanding of the amount of margin between the datasheet limits can be developed, and more importantly, an understanding of the intrinsic failure mechanisms can be found. By knowing the intrinsic failure mechanisms, the root cause of failure, and the behavior of the device over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions (For an excellent description of this methodology for testing semiconductor devices, see reference [13]).

Key Stress Conditions and Intrinsic Failure Mechanisms for GaN Power Devices

What are the key stress conditions encountered by GaN power devices and what are the intrinsic failure mechanisms for each stress condition?

As with all power transistors, the key stress conditions involve voltage, current, temperature, and humidity, as well as various mechanical stresses. There are, however, many ways of applying these stress conditions. For example, voltage stress on a GaN FET can be applied from the gate terminal to the source terminal (V_{GS}), as well as from the drain terminal to the source terminal (V_{DS}). For example, these stresses can be applied continuously as a DC bias, they can be cycled on-and-off, or they can be applied as high-speed pulses. Current stress can be applied as a continuous DC current, or as a pulsed current. Thermal stresses can be applied continuously by operating devices at a predetermined temperature extreme for a period of time, or temperature can be cycled in a variety of ways.

By stressing devices with each of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test can be determined. To generate failures in a reasonable amount of time, the stress conditions typically need to significantly exceed the datasheet limits of the product. Care needs to be taken to make certain the excess stress condition does not induce a failure mechanism that would never be encountered during normal operation. To make certain this is not the case, the failed parts need to be carefully analyzed to determine the root cause of their failure.

Only by verifying the root cause can a true understanding of the behavior of a device under a wide range of stress conditions be developed. It should be noted that, as more understanding of intrinsic failure modes in eGaN devices is gained, two facts have become clear; (1) eGaN devices are more robust that Si-based MOSFETs, and (2) MOSFET intrinsic failure models are not valid when predicting eGaN device lifetime under extreme or long-term electrical stress conditions.

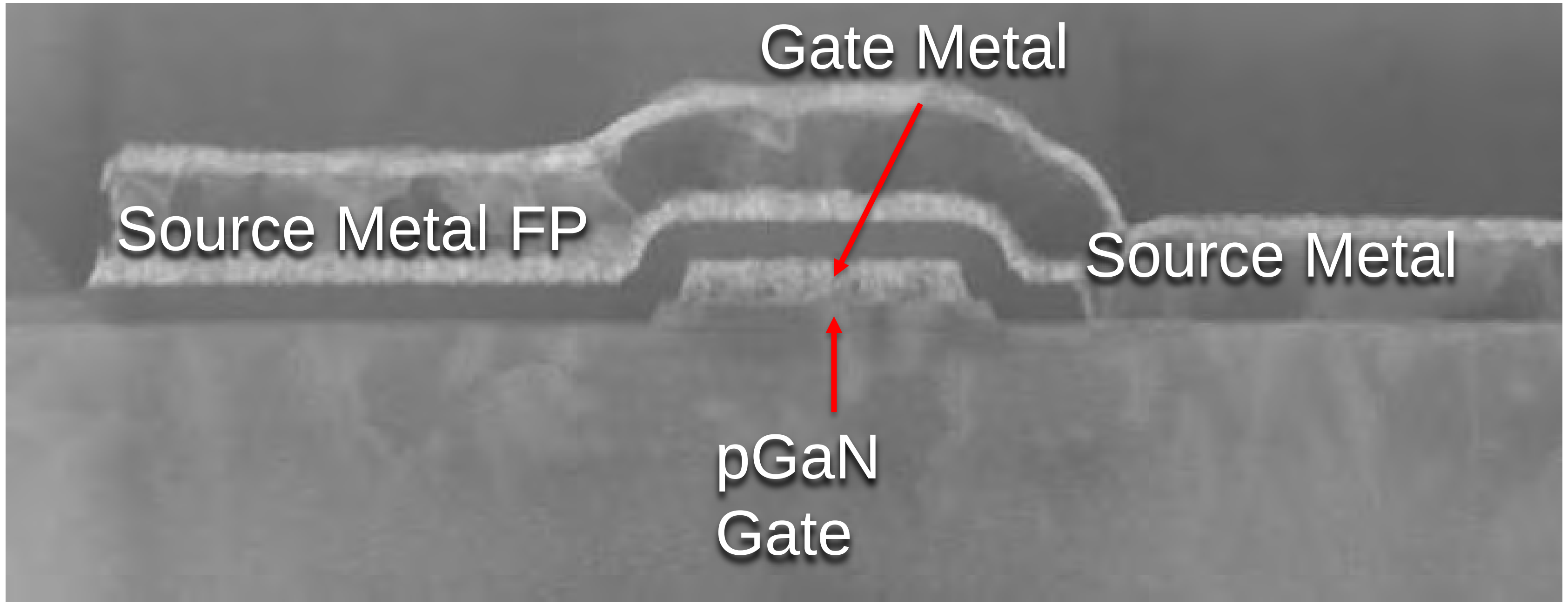
Stressor	Device/ Package	Test Method	Intrinsic Failure Mechanism	EPC Test Results
Voltage	Device	HTGB	Dielectric failure (TDDB)	This Report
			Threshold shift	
		HTRB	Threshold shift	This Report
			$R_{DS(on)}$ shift	
		ESD	Dielectric rupture	[2,3,6,7,8,9,10]
Current	Device	DC Current (EM)	Electromigration	In Progress
			Thermomigration	In Progress
Current + Voltage (Power)	Device	SOA	Thermal Runaway	This Report
		Short Circuit	Thermal Runaway	This Report
Voltage Rising/Falling	Device	Hard-switching Reliability	$R_{DS(on)}$ shift	This Report
Current Rising/Falling	Device	Pulsed Current (Lidar reliability)	None found	This Report
Temperature	Package	HTS	None found	[6,7,8,9]
Humidity	Package	MSL1	None found	[3,4,5,6,7,8,9,10]
		H3TRB	None found	[1,2,3,4,5,6,7,8,9,10]
		AC	None found	[4,5,6,7,8,9]
		Solderability	Solder corrosion	This Report
		uHAST	Dendrite Formation/Corrosion	[10]
Mechanical / Thermo-mechanical	Package	TC	Solder Fatigue	This Report
		IOL	Solder Fatigue	This Report
		Bending Force Test	Delamination	This Report
		Bending Force Test	Solder Strength	This Report
		Bending Force Test	Piezoelectric Effects	This Report
		Die shear	Solder Strength	This Report
		Package force	Film Cracking	This Report

Table 1: Stress Conditions and Intrinsic Failure Mechanisms for eGaN FETs

Stress – Voltage

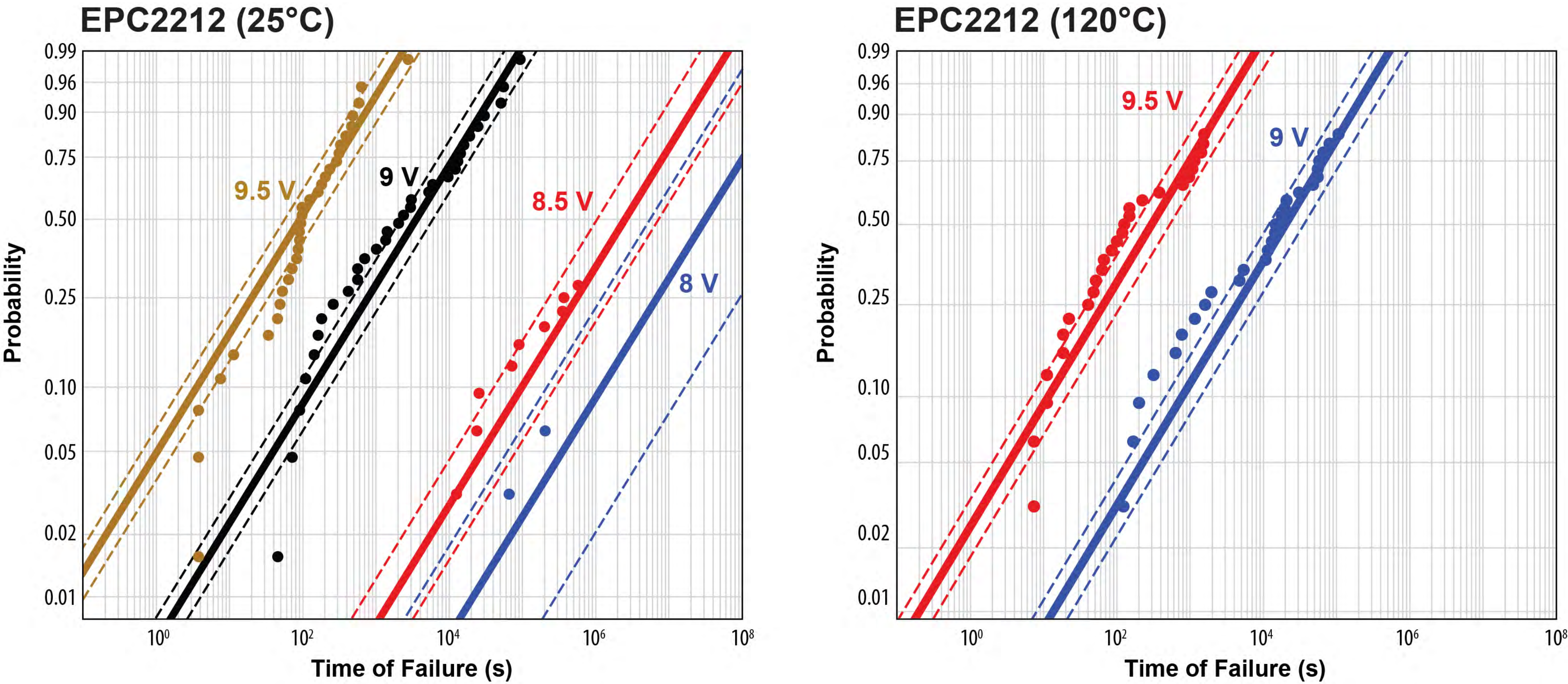
Gate-Source

Gate-Source Voltage Stress

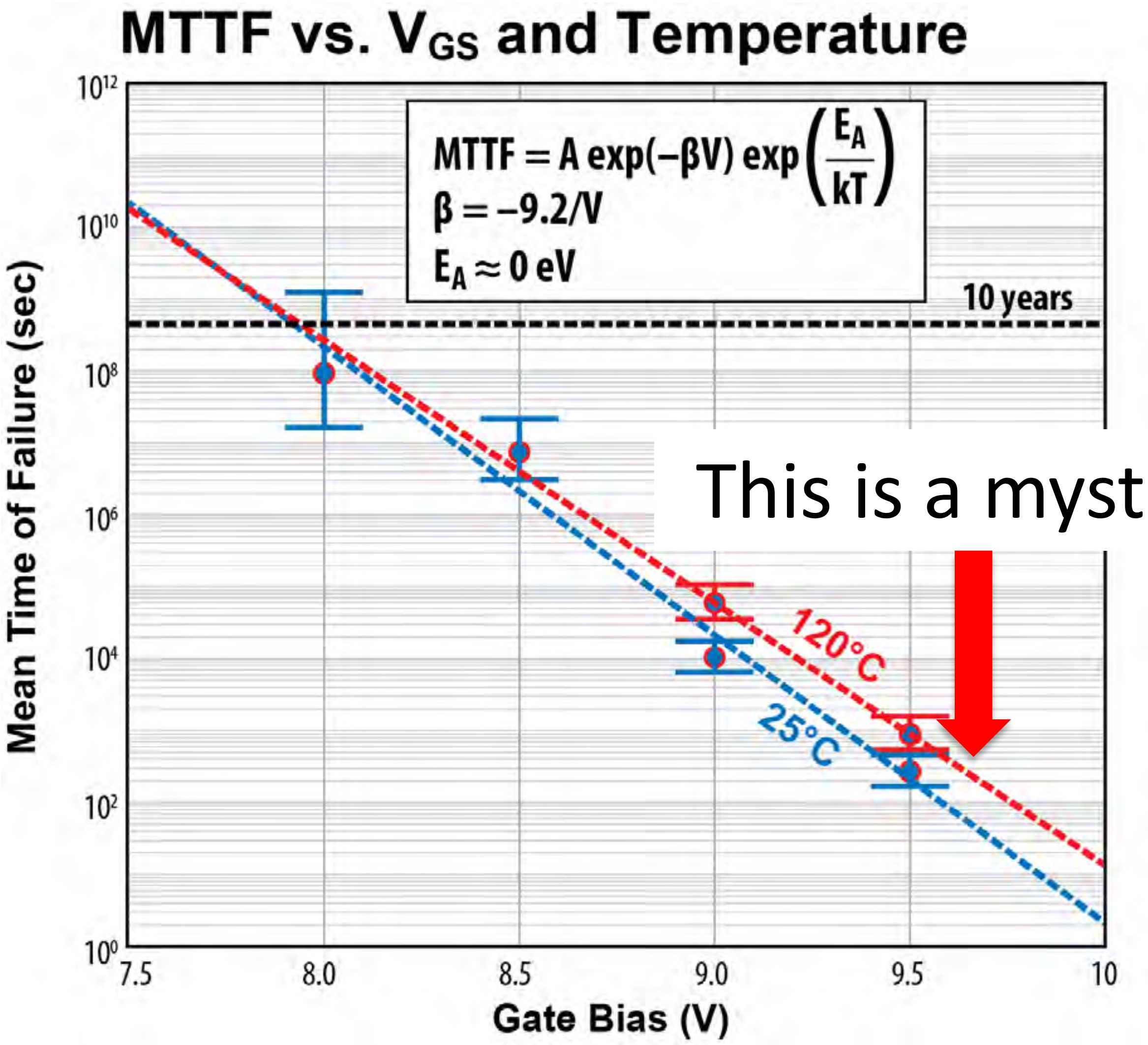


Gate Acceleration: Analysis

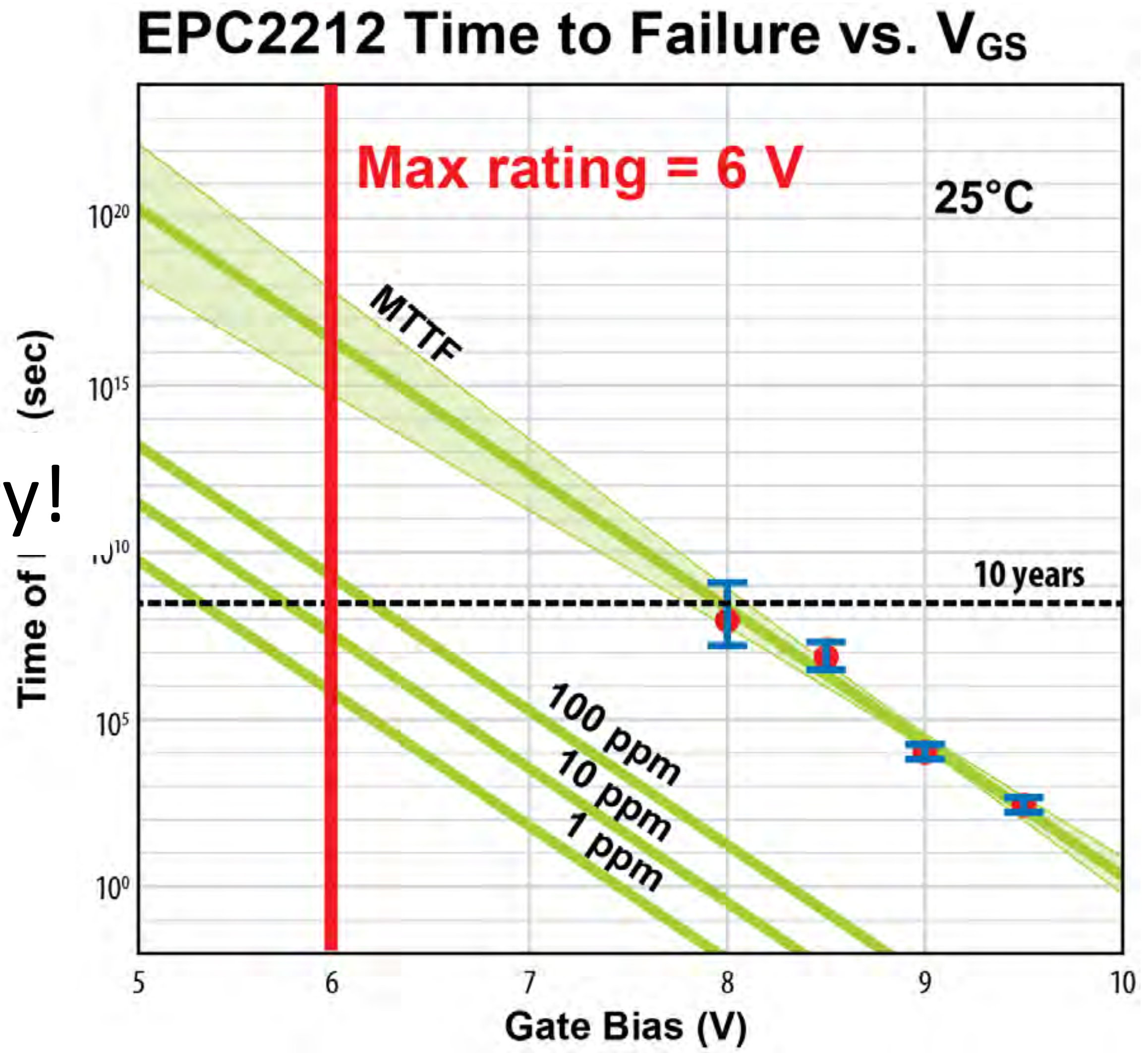
Data Sheet Maximum = 6 V_{GS}



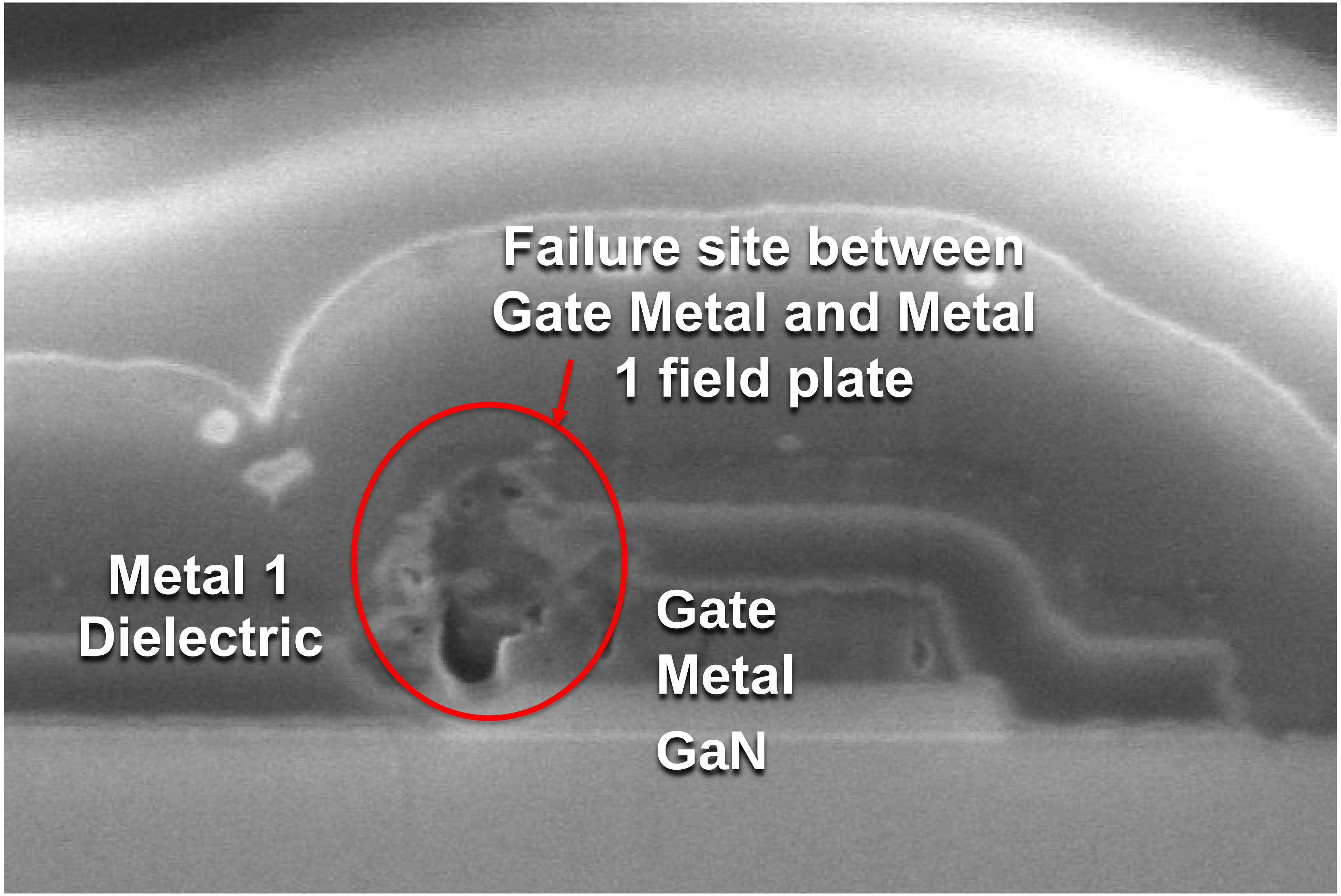
Gate Acceleration: Time to Failure



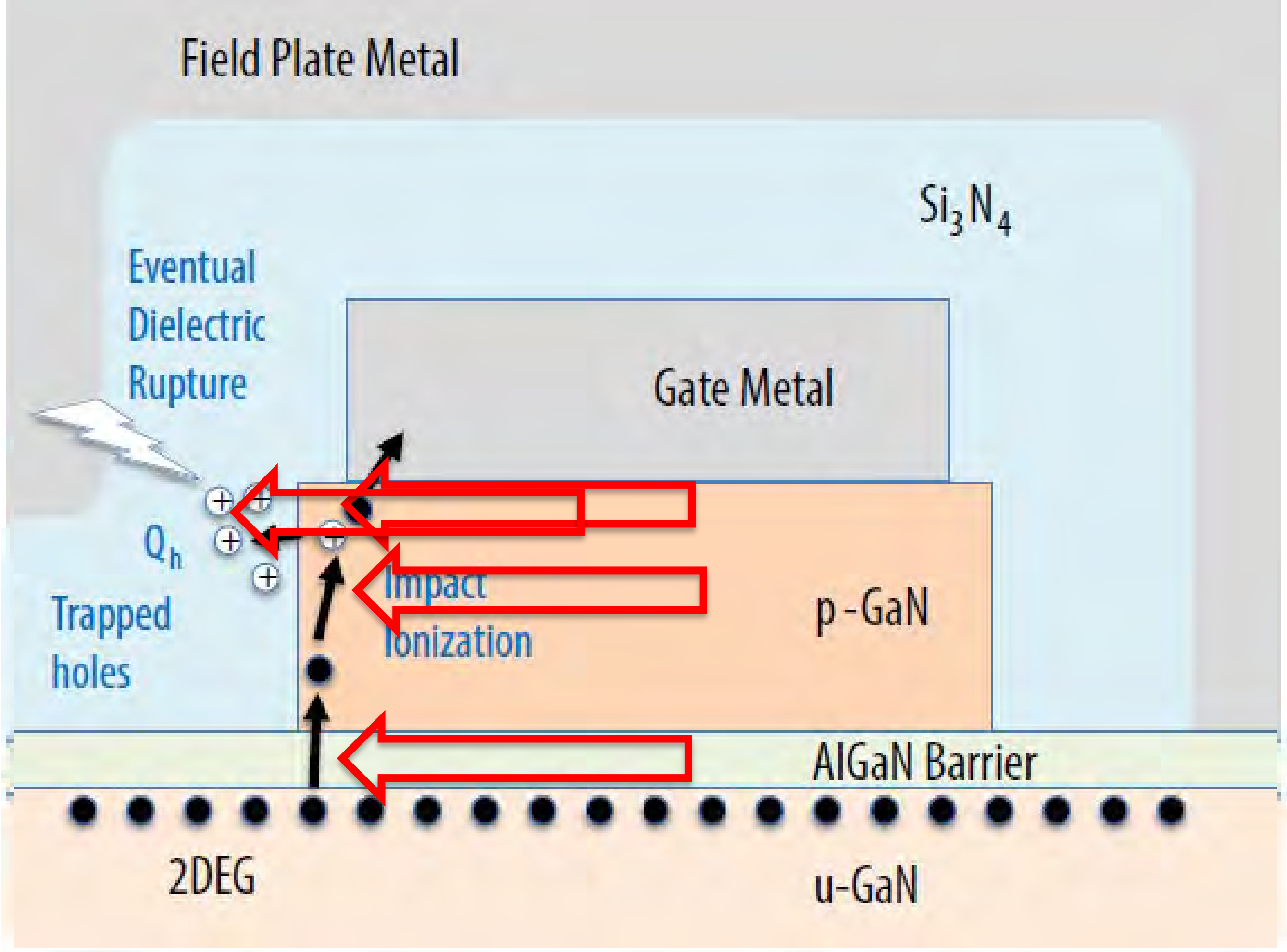
This is a mystery!



Gate Failures Not in GaN



Impact Ionization Mechanism



Impact Ionization Model Development

$$G = \alpha_n \frac{|J_n|}{q} + \alpha_p \frac{|J_p|}{q}$$

$$\alpha_n = a_n e^{-(b_n/F)^m}$$

Ref	a_n(1/cm)	b_n(V/cm)	m
Ji et al.[12]	2.10E+09	3.70E+07	1
Ozbek [13]	9.20E+05	1.70E+07	1
Cao et al. [8]	4.48E+08	3.40E+07	1
Ooi et al. [15]	7.32E+07	7.16E+06	1.9

$$a_n(T) = a_{n;0}(1 - c\Delta T)$$

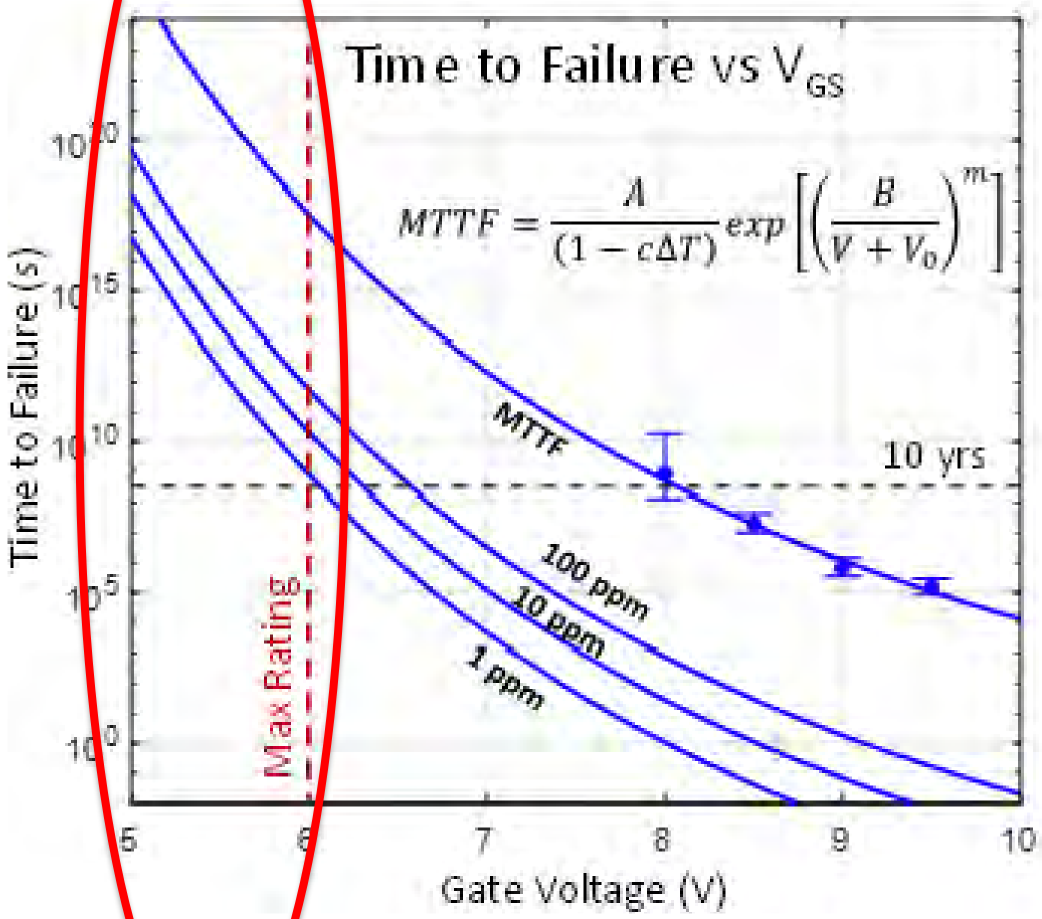
$c = 6.5x10^{-3}\ K^{-1}$

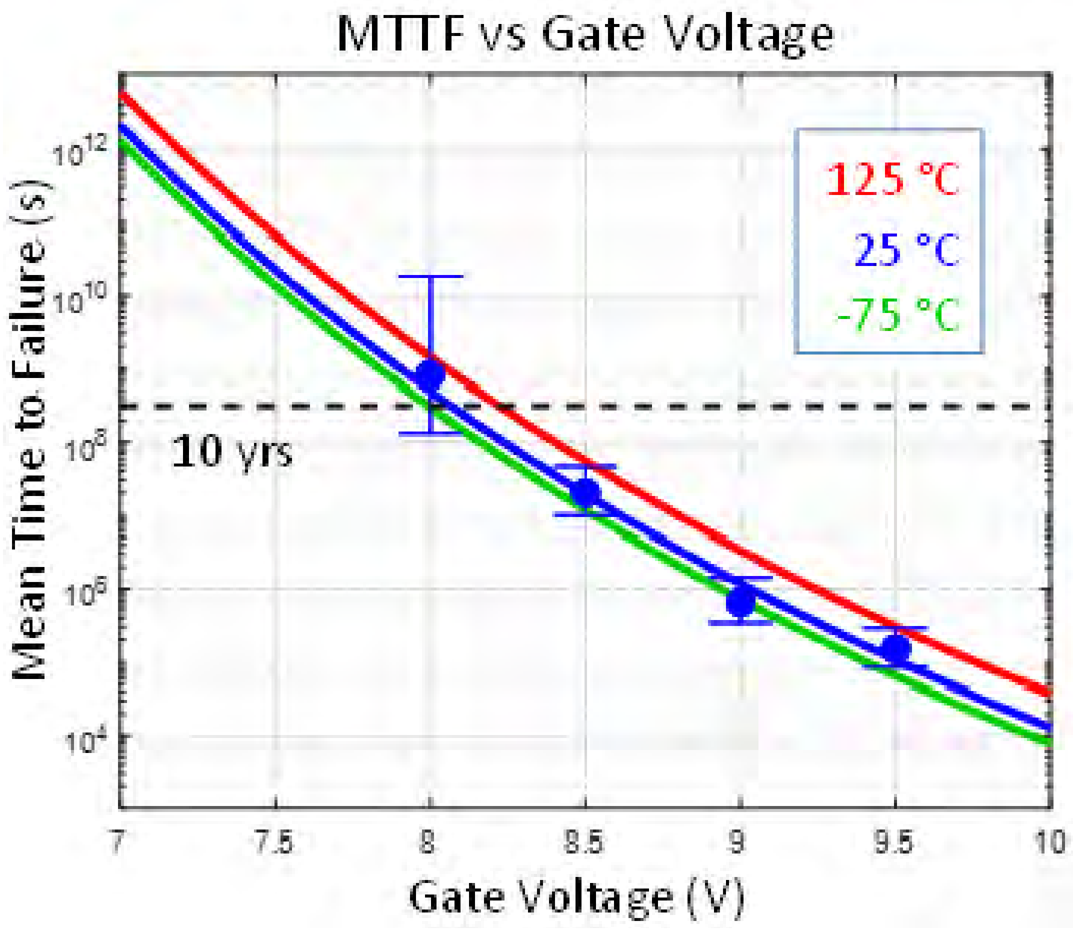
$$G \approx \alpha_n \frac{|J_n|}{q} \qquad J_n >> J_p \qquad MTTF \propto \frac{Q_c}{G} \qquad MTTF \propto \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \frac{qQ_c}{J_n a_{n,0}(1-c\Delta T)} exp\left[\left(\frac{b_n}{F}\right)^m\right]$$

$$MTTF = \frac{Q_c}{G} = \frac{qQ_c}{\alpha_n J_n} = \boxed{\frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V+V_0}\right)^m\right]}$$

$m = 1.9$
$V_0 = 1.0\ V$
$B = 57.0\ V$
$A = 1.7x10^{-6}\ s$
$c = 6.5x10^{-3}\ K^{-1}$

Theory vs. Experimental Results

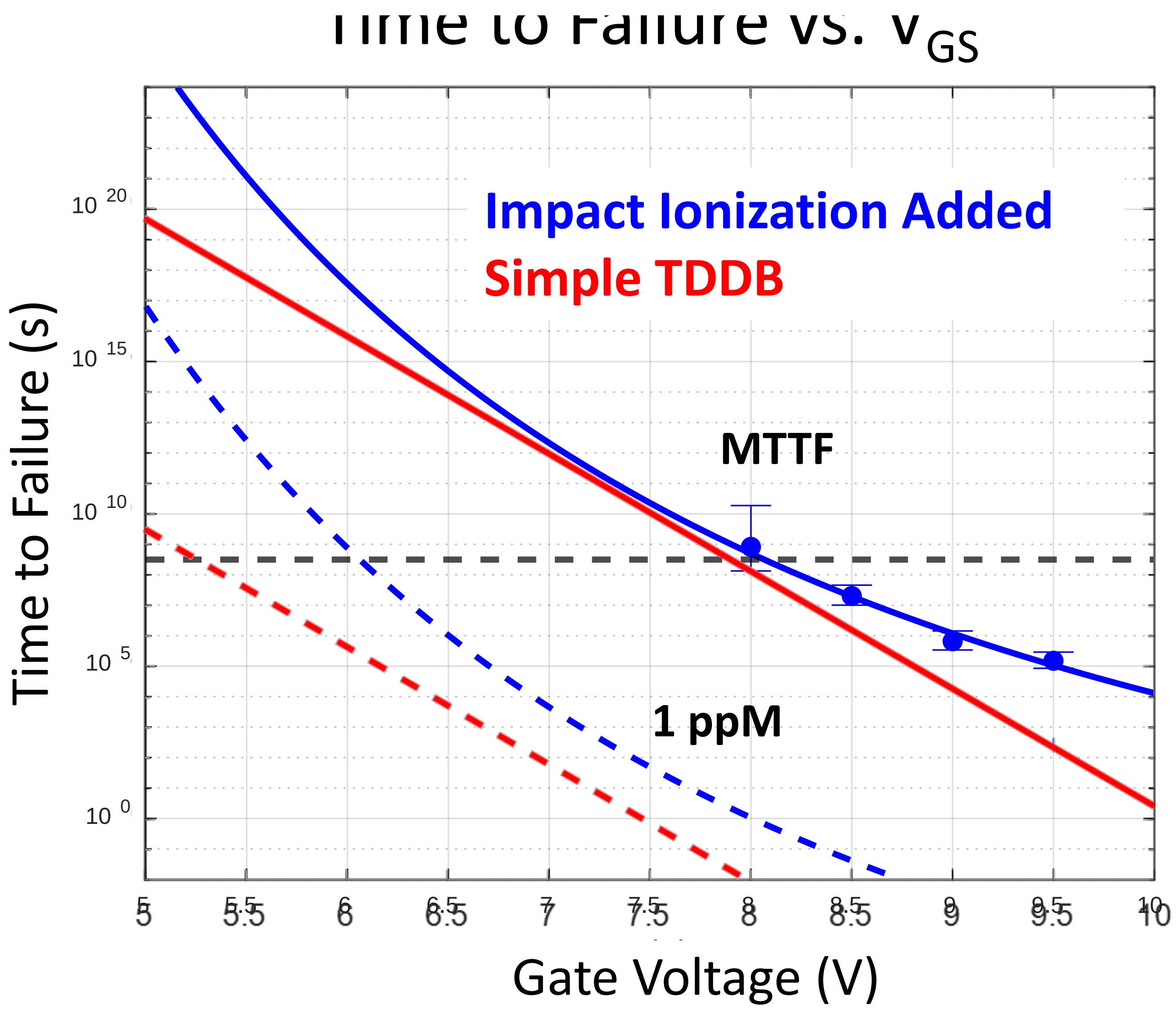




$$MTTF(V_{GS},\Delta T) = \frac{A}{(1-c\Delta T)} exp\left[\left(\frac{B}{V_{GS}+V_0}\right)^m\right]$$

$m = 1.9$
$V_0 = 1.0$ V
$B = 57.0$ V
$A = 1.7\times10^{-6}$ s
$c = 6.5\times10^{-3}$ K^{-1}

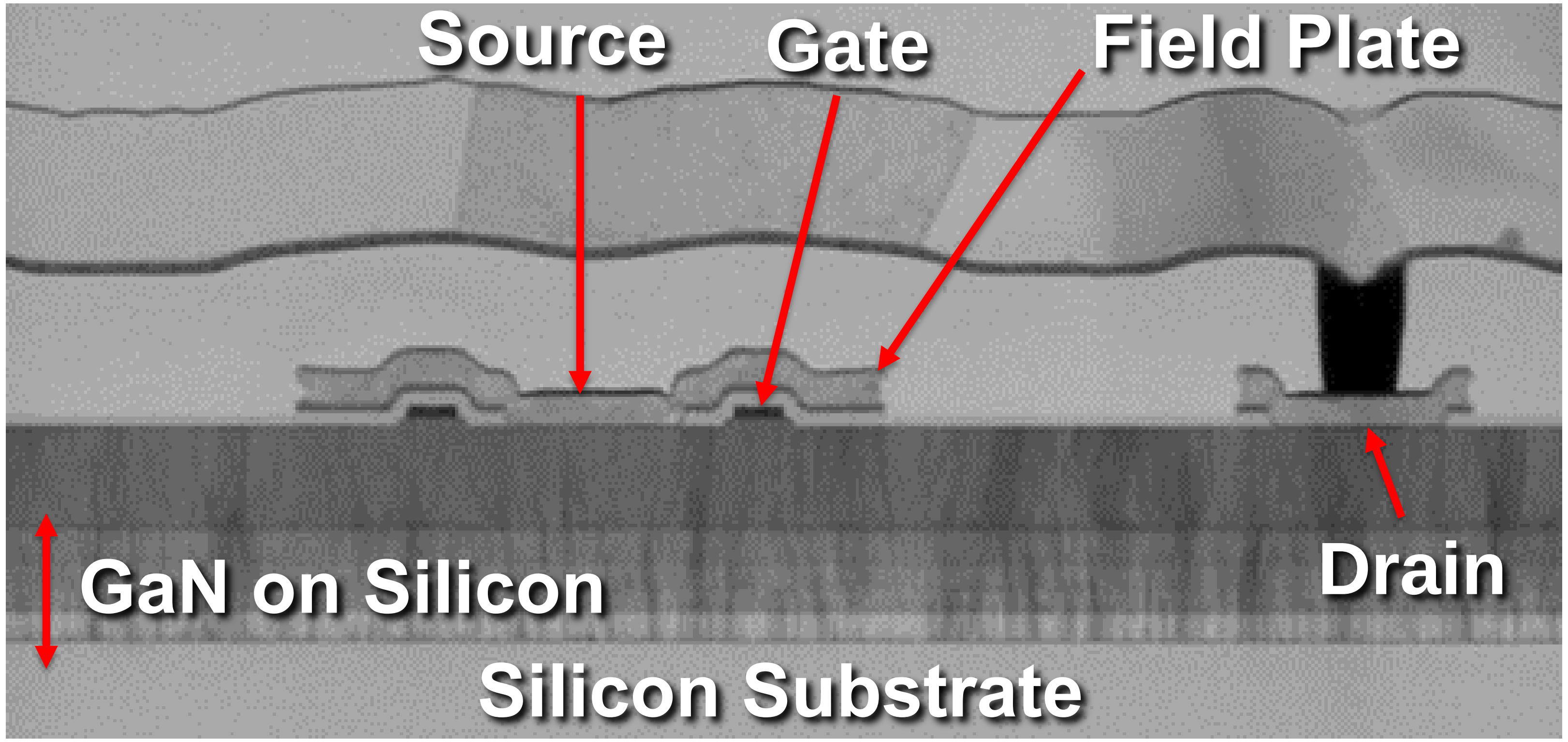
TDDB vs. Impact Ionization Models



Stress – Voltage

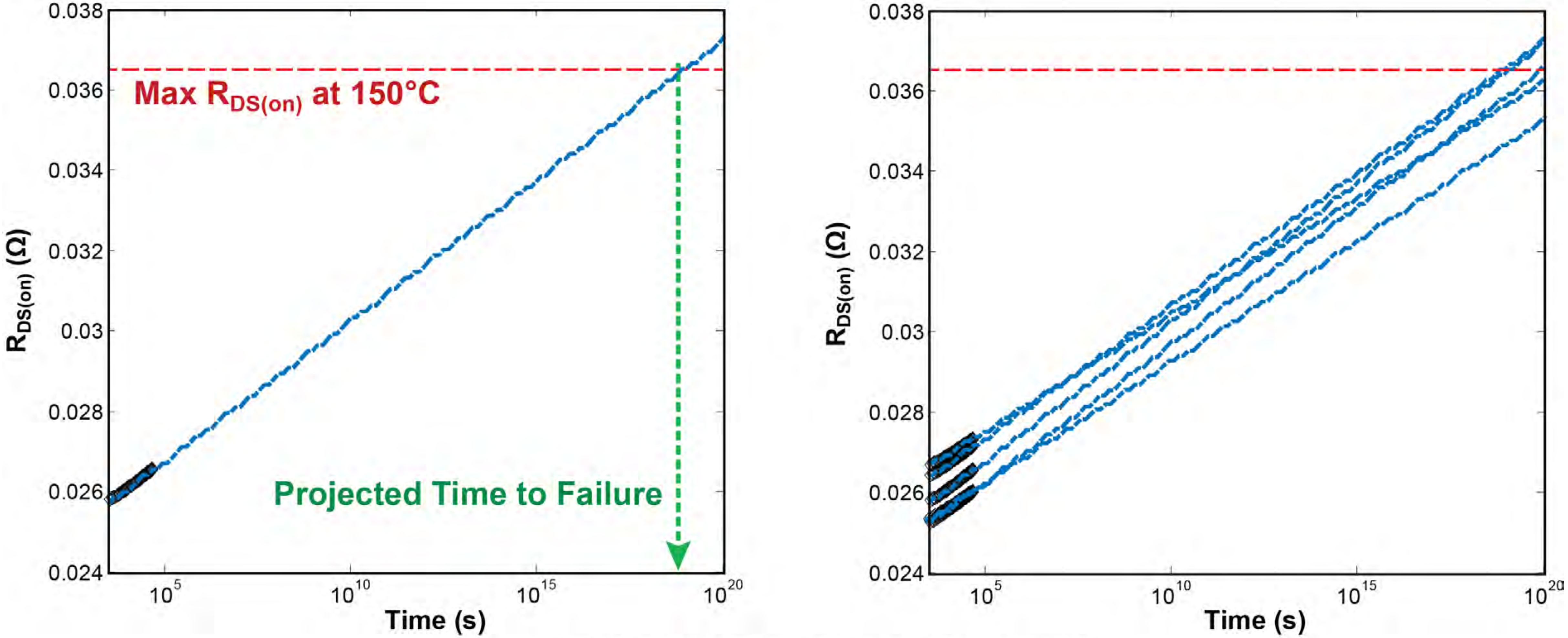
Drain-Source

Drain-Source Voltage Stress



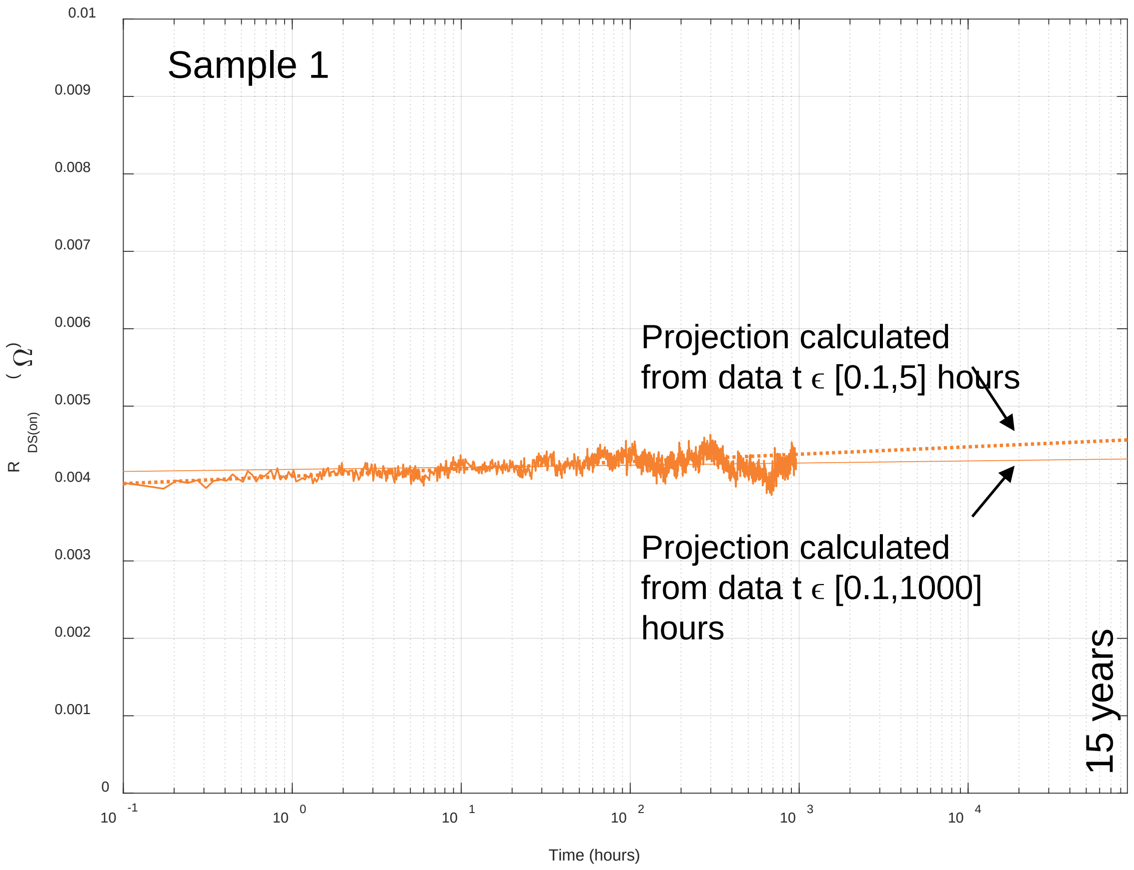
Characterizing $R_{DS(on)}$ Shift in Time

120 V overstress at 150°C (100 V Rated Device)



$$R(t) = R_0\,(\alpha + \beta \ln[t])$$

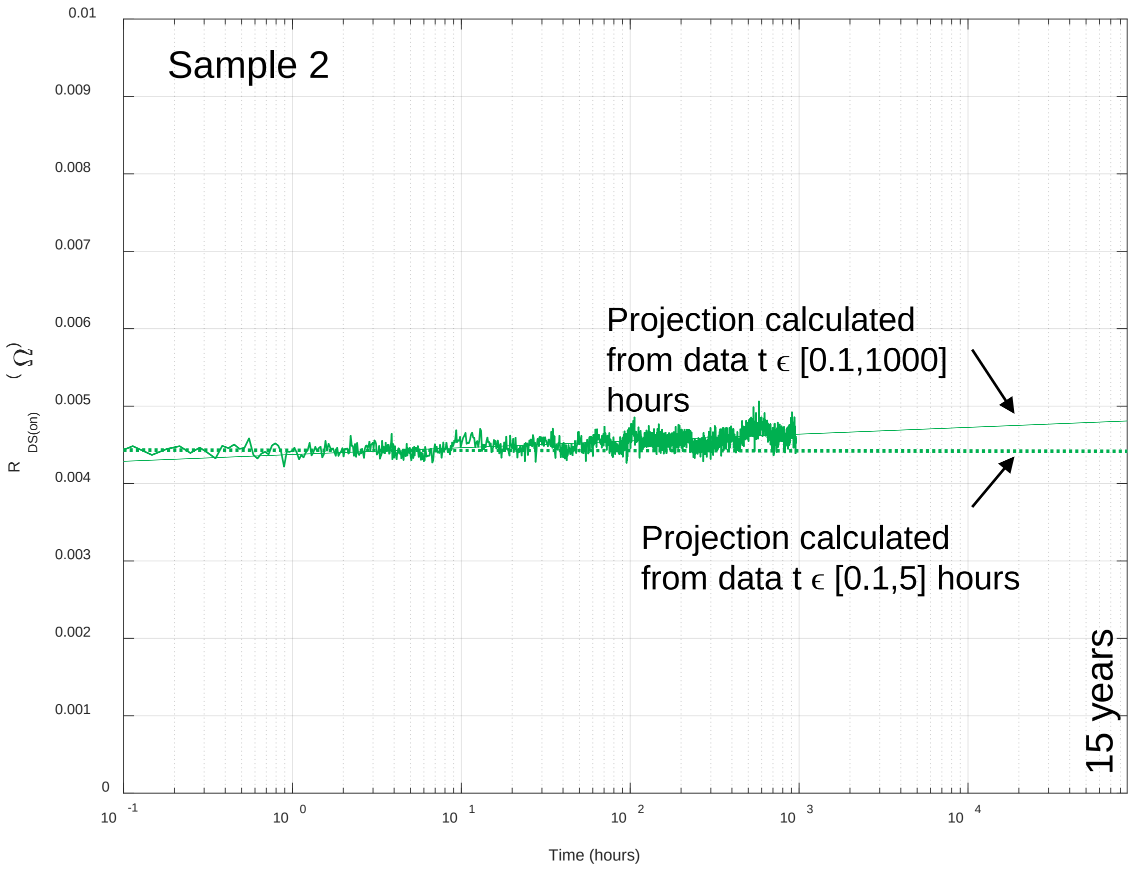
$R_{DS(on)}$ Projection Analysis


Sample 1

Projection calculated from data t ϵ [0.1,5] hours

Projection calculated from data t ϵ [0.1,1000] hours

15 years

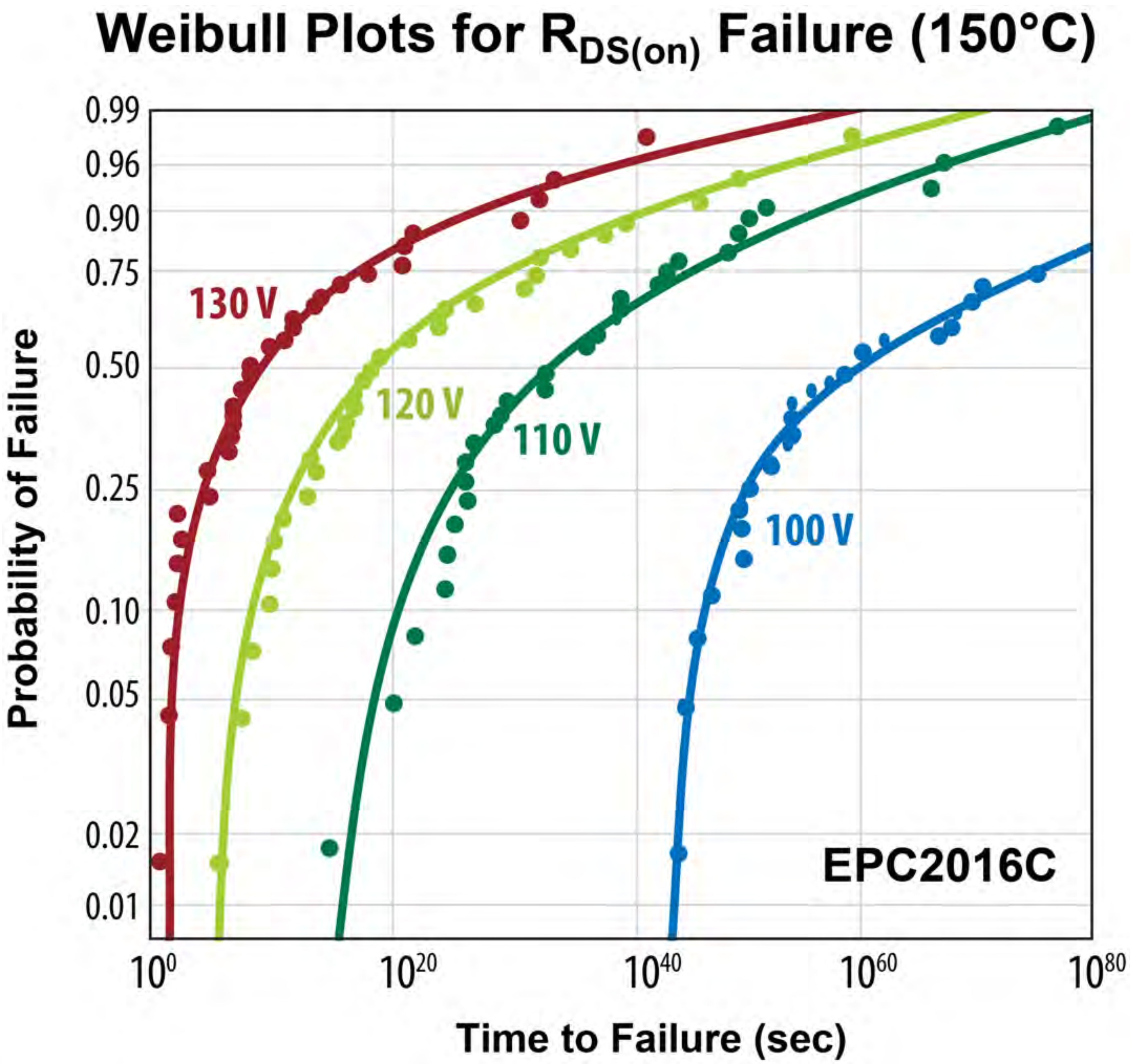

Sample 2

Projection calculated from data t ϵ [0.1,1000] hours

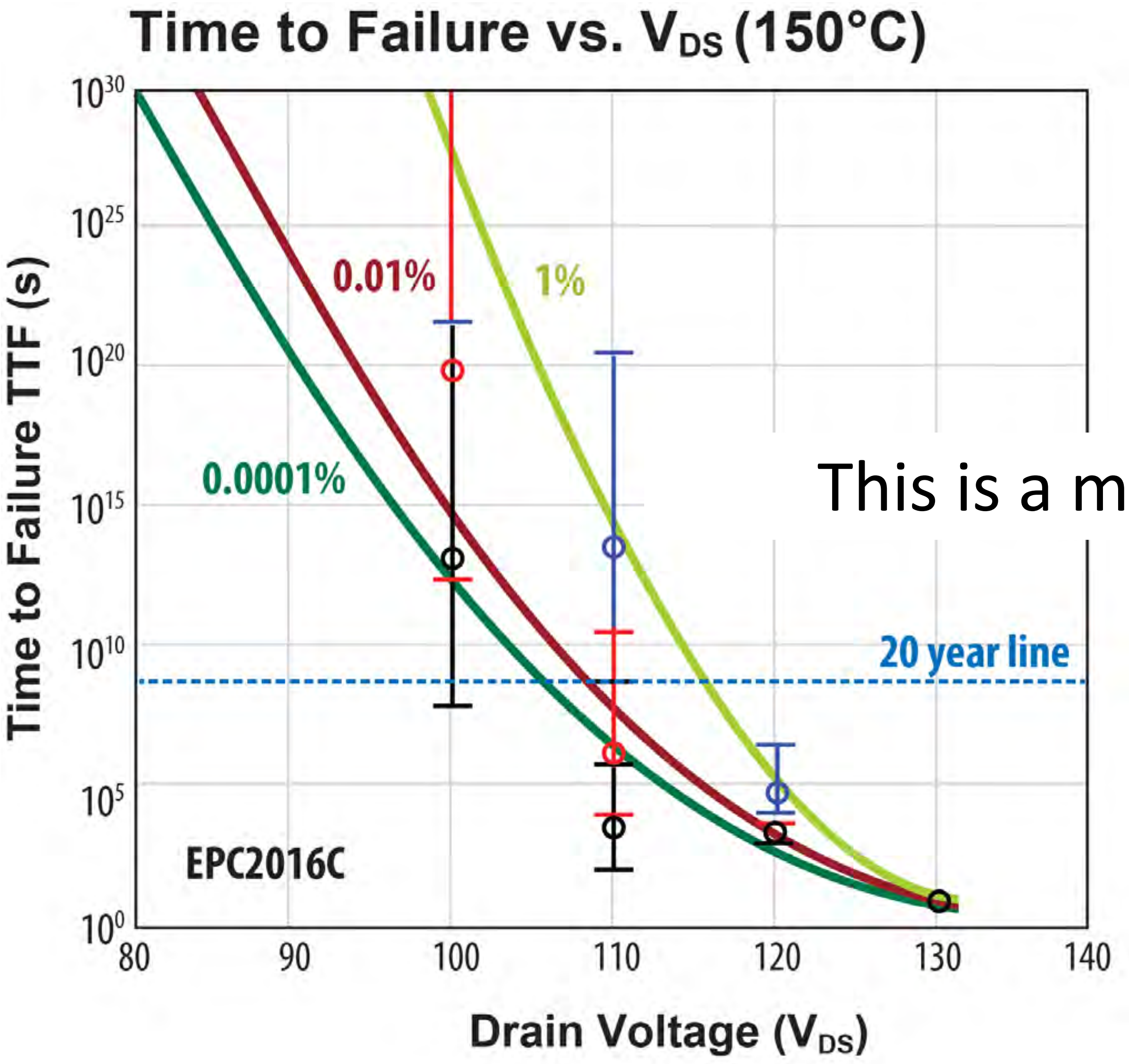
Projection calculated from data t ϵ [0.1,5] hours

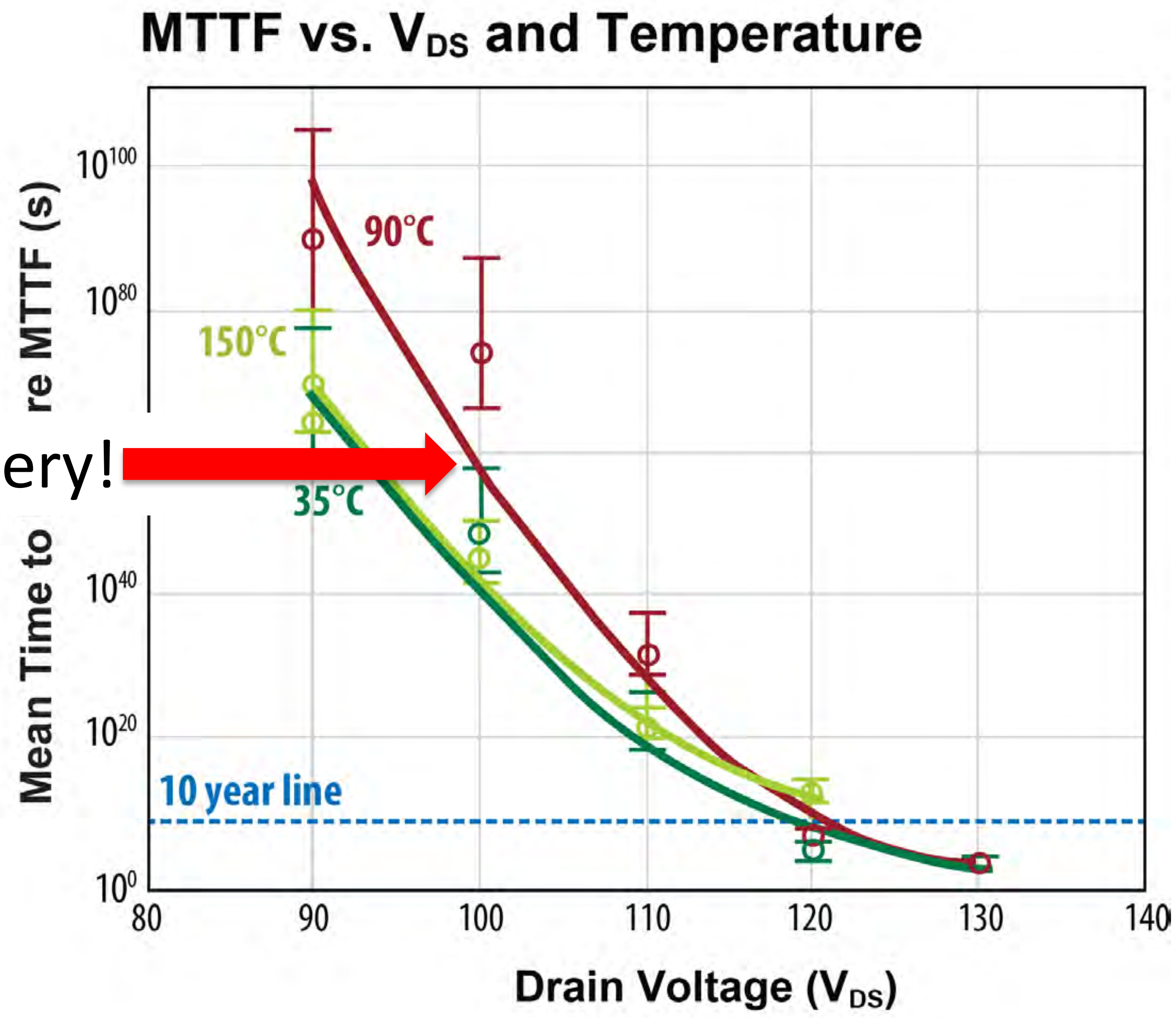
15 years

Drain Stress Weibull Fits



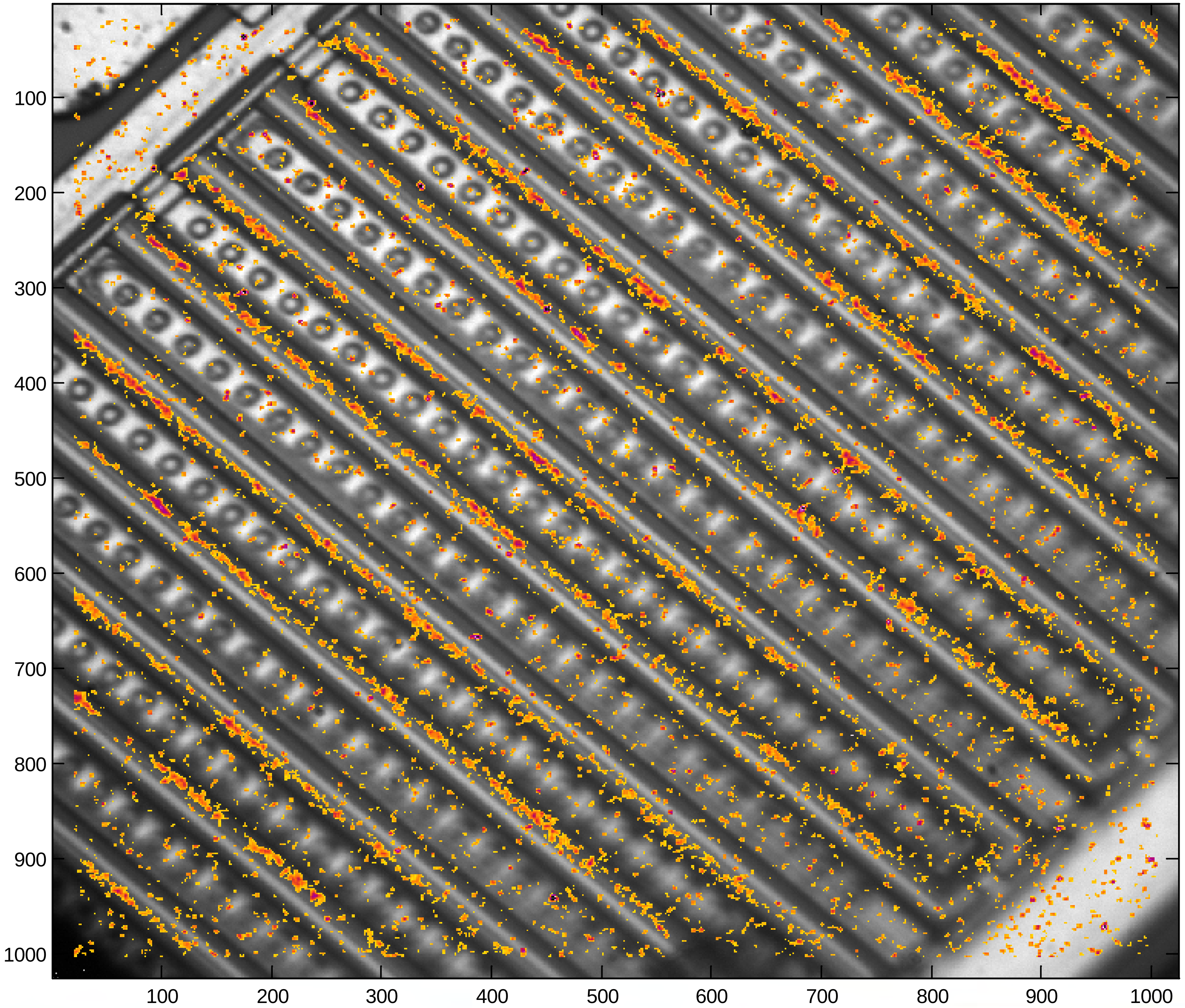
Device Robustness vs. V_{DS}



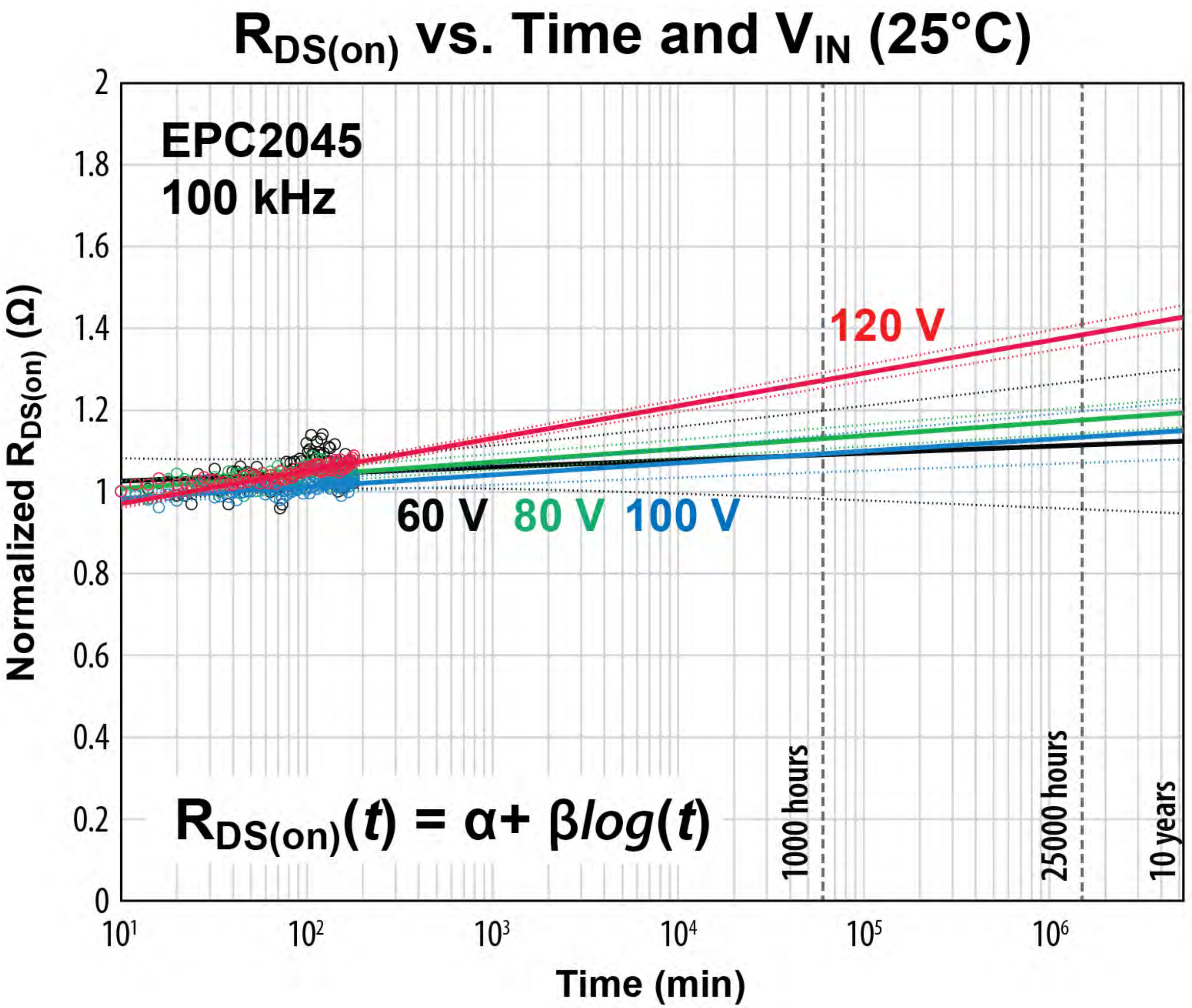


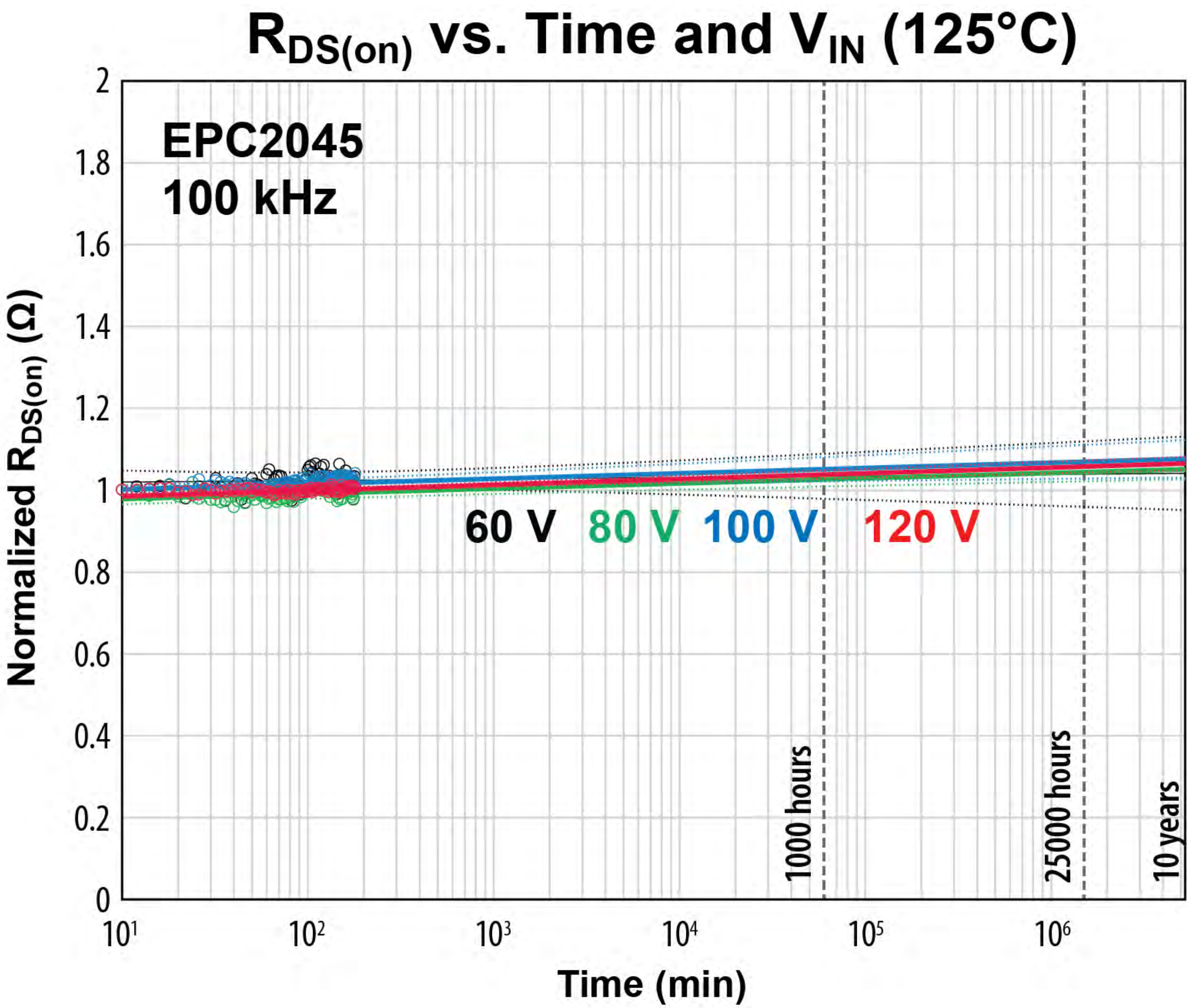
This is a mystery!

Physics of $R_{DS(on)}$ Shift – Hot Carrier Emission

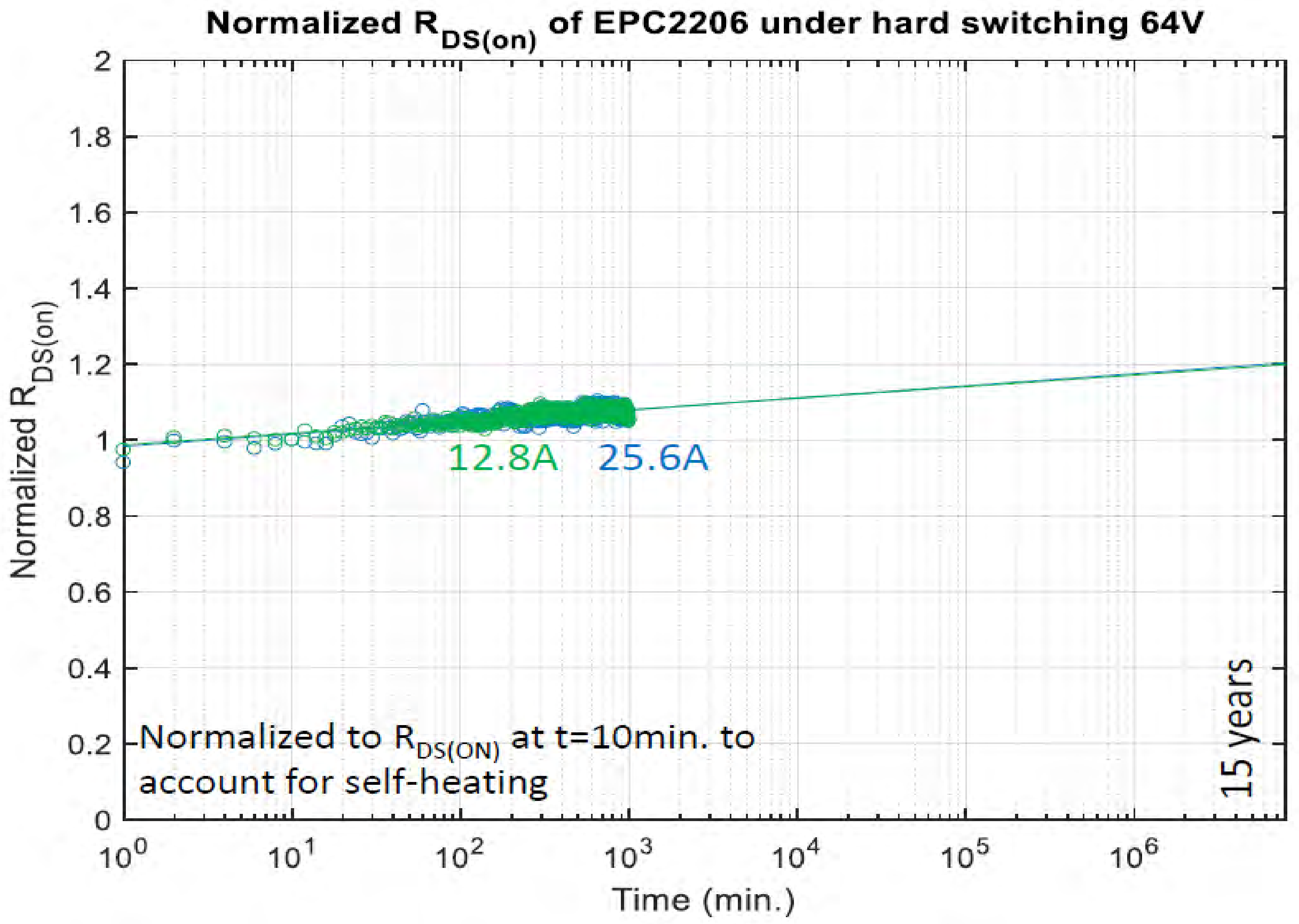


Hard-Switching: Effect of V_{IN}

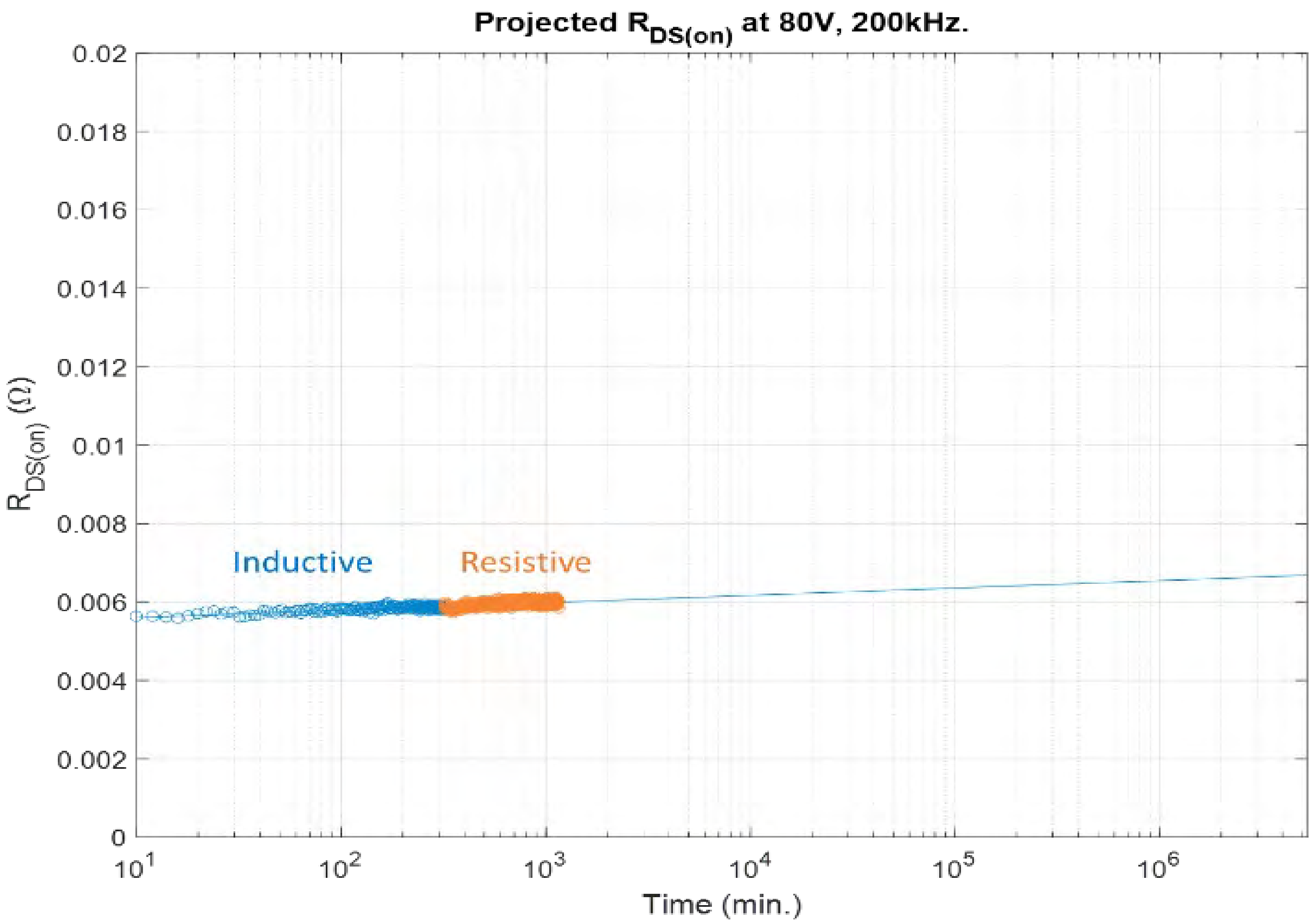




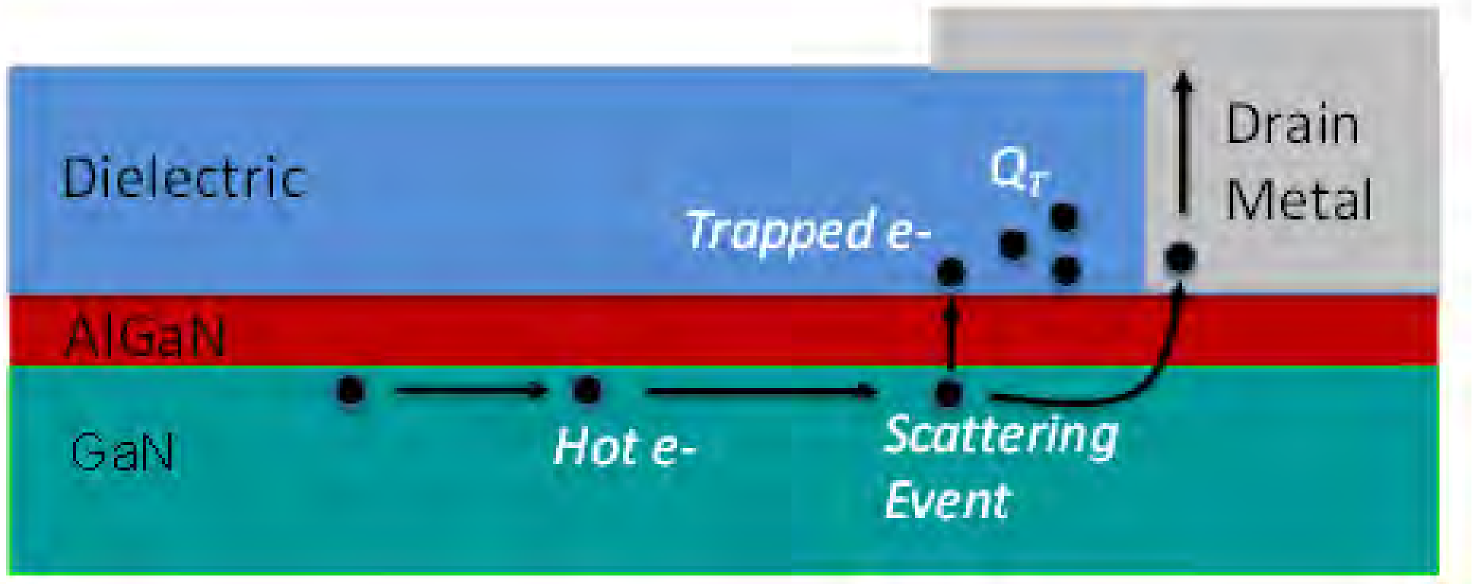
Impact of Switched Current

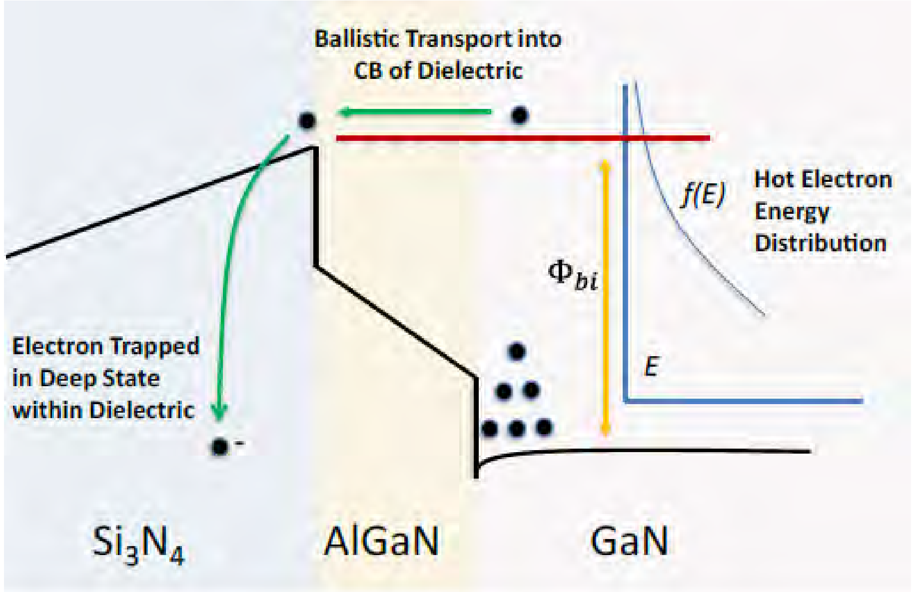


Inductive vs. Resistive Switching



Hot Carrier Trapping Mechanism





Hot Carrier Trapping Model

$$f(E)dE \propto E e^{-E/qF\lambda} dE$$

$$\frac{dQ_S}{dt} = A \int_{\Phi_{bi}+\beta Q_S}^{\infty} f(E)dE = A \int_{\Phi_{bi}+\beta Q_S}^{\infty} E e^{-E/qF\lambda} dE$$

$$\frac{dQ_S}{dt} = B \exp\left(-\frac{\beta Q_S}{qF\lambda}\right)$$

$$Q_S\,(t) = \frac{qF\lambda}{\beta} \log\left(1 + \frac{B\beta}{qF\lambda} t\right)$$

$$R(t) = R_0 + \frac{C}{Q_P - Q_S} = R_0 + \frac{C}{Q_P - \frac{qF\lambda}{\beta} \log\left(1 + \frac{B\beta}{qF\lambda} t\right)}$$

$$R(t) \approx R_0 + \frac{C}{Q_P}\left[1 + \frac{qF\lambda}{Q_P\beta} \log\left(1 + \frac{B\beta}{qF\lambda} t\right)\right]$$

$$\tau_{LO} \propto exp\left(\frac{\hbar\omega_{LO}}{kT}\right)$$

$$\lambda = v_{th}\tau_{LO} \propto A\sqrt{kT} exp\left(\frac{\hbar\omega_{LO}}{kT}\right)$$

$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF \exp\left(\frac{\hbar\omega_{LO}}{kT}\right) \sqrt{T} \log(t)$$

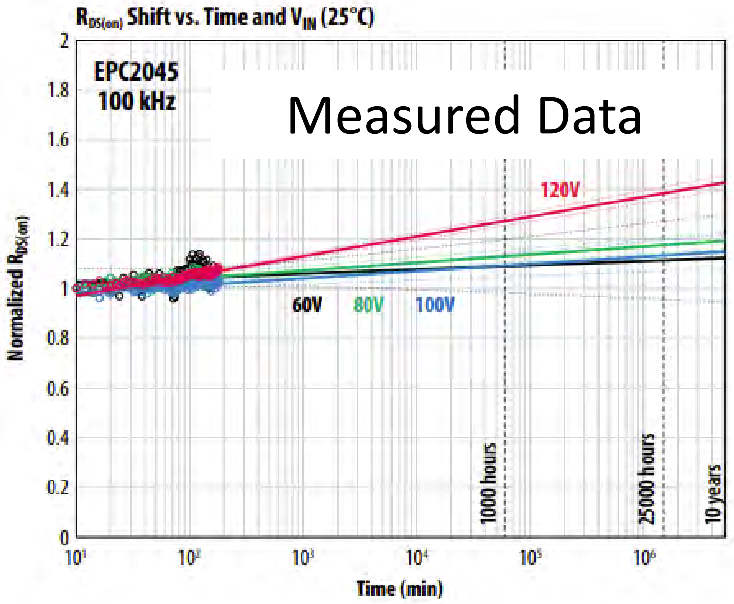
Putting it All Together – Hot Carrier Trapping Model

$$\frac{\Delta R}{R} = \frac{R(t) - R(0)}{R(0)} \approx a + bF \exp\left(\frac{\hbar\omega_{LO}}{kT}\right)\sqrt{T}\log(t)$$

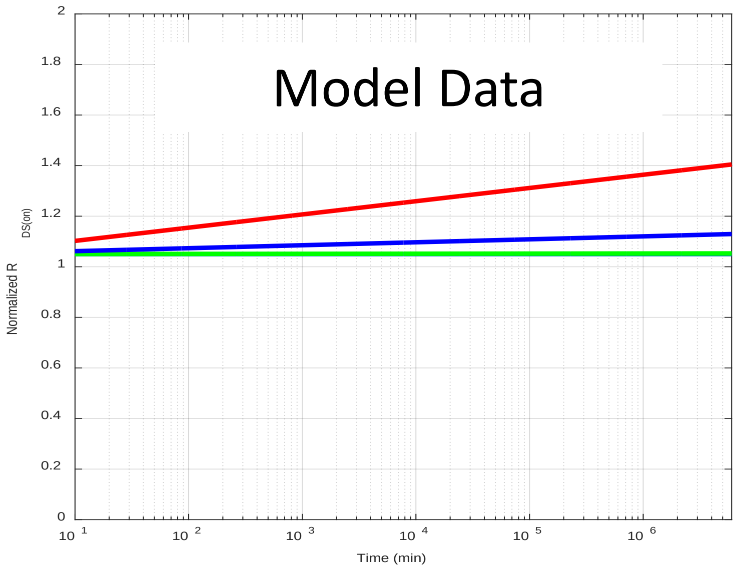
$$= a + b\left[\frac{V_{DS}}{1 + exp[-\alpha(V_{DS} - V_{FD})]}\right]^2 exp\left(\frac{2\hbar\omega_{LO}}{kT_l}\right)\log(t)$$

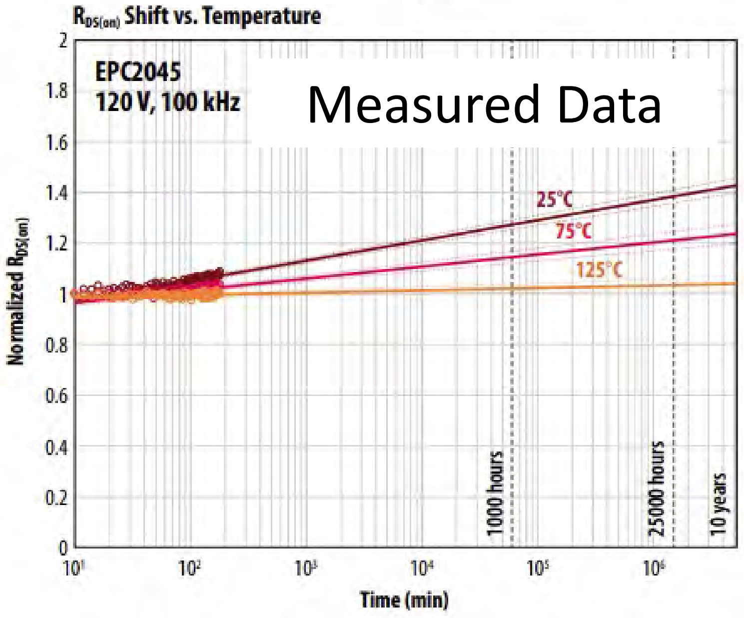
a = 0.02 (unitless)
b = 1.9E-8 (V^{-2})
$\hbar\omega_{LO}$ = **92** meV
V_{FD} = 100V (appropriate for Gen5 100V products only)
α = 0.1 (V^{-1})
t = time in min

Model vs Measurement

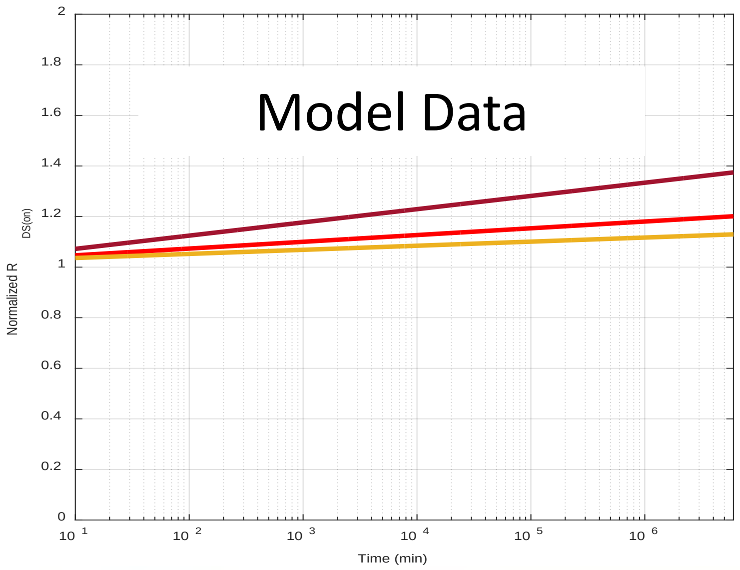


$R_{DS(on)}$ Shift vs. Time and V_{IN} (25°C)





$R_{DS(on)}$ Shift vs. Temperature

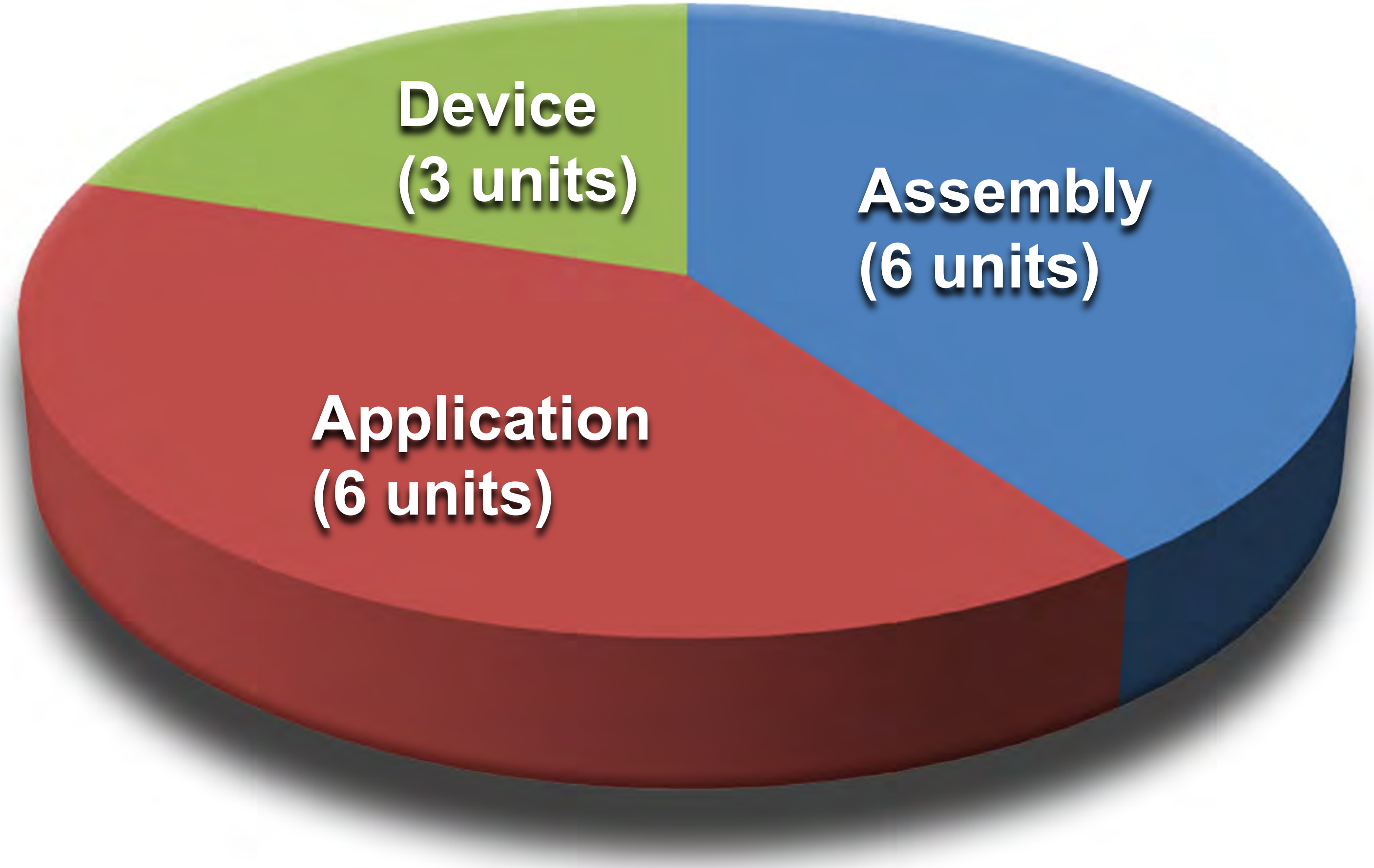


Field Results

eGaN FET Reliability

Field Failures by Category

1/1/2017– 12/31/2020



Proven Reliability – 226 billion device hours in the field since January 1, 2017 with only 3 device failures.

EPC
EFFICIENT POWER CONVERSION


EPC eGaN FET Die Attachment Tutorial

How To GaN Video Series

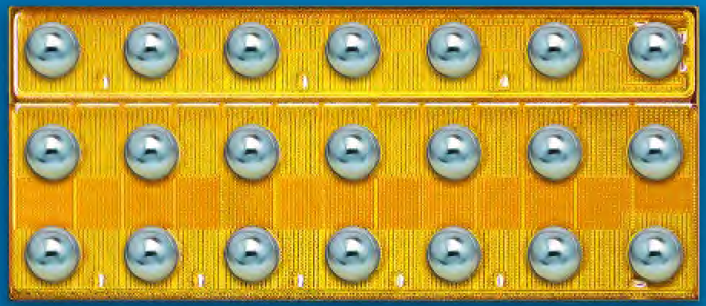

GaN Transistors for Efficient Power Conversion

Third Edition

Alex Lidow
Michael de Rooij
Johan Strydom
David Reusch
John Glaser

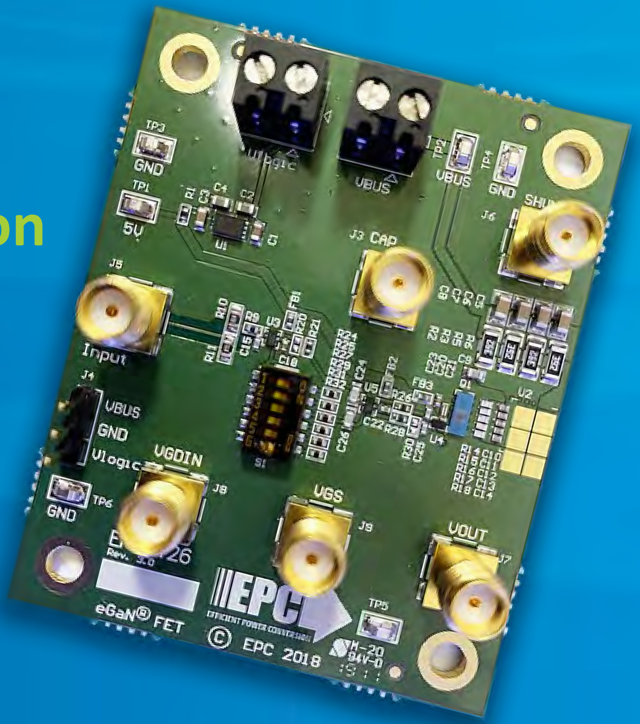
WILEY

3rd Edition Textbook



eGaN® FETs and ICs

Evaluation Kits



epc-co.com

Next Webinar