Thermal Performance of EPC eGaN® FETs

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Thermal resistance is a major factor in determining the capabilities of discrete power devices. From a device's thermal characteristics both the maximum power dissipation and maximum current can be derived for user applications. While the thermal performance of traditional silicon MOSFETs is well understood, measuring the thermal performance of eGaN® FETs requires some further explanation. This Applications Note investigates the testing method and results of thermal resistance measurements on eGaN FETs.

Thermal Measurement Method

EPC's eGaN FETs are gallium nitride based enhancement-mode high electron mobility transistors (HEMT). They behave much like silicon power MOSFETs. A positive bias on the gate relative to the source causes a field effect which attracts electrons that complete a bi-directional channel between the drain and the source. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region, and once again, giving it the capability to block voltage. Table 1 shows an overview of EPC's eGaN FET characteristics.

Users of traditional silicon MOSFETs recognize that there are three temperature sensitive parameters that have been employed as indicators of device junction temperature (T_J). However, the eGaN FET has some limitations. The first limitation is that there is no intrinsic body diode that can be used to evaluate junction temperature. EPC's eGaN FETs do not have the parasitic bipolar junction that is common to silicon MOSFETs, and the reverse conduction of these eGaN FETs has a different mechanism. With 0 V gate to source, reverse conduction occurs, but the source-drain voltage virtually does not vary with temperature. The second limitation is that gate threshold voltage ($V_{GS(TH)}$) is very low and the slope of $V_{GS(TH)}$ over temperature is rather flat when compared to silicon MOSFETs. This means that $V_{GS(TH)}$ cannot be used easily because of practical instrumentation limitations. The remaining temperature sensitive parameter is device on-resistance ($R_{DS(on)}$) and, therefore, becomes the parameter of choice for the measurement of junction temperature.

Part Number	LGA Package (mm)	Mode Ch	V_{DS}	V_{GS}	Max $R_{DS(on)}$ (mΩ) @5V	Q_G @5V	Q_{GS} Typ	Q_{GD} Typ	Vth Typ	Q_R	I_D
EPC1014	1.7 x 1.1	EN	40	6	16.0	3.0	1.0	0.6	1.4	0	10
EPC1015	4.1 x 1.6	EN	40	6	4.0	11.6	3.8	2.2	1.4	0	33
EPC1009	1.7 x 1.1	EN	60	6	30.0	2.4	0.8	0.6	1.4	0	6
EPC1005	4.1 x 1.6	EN	60	6	7.0	10.0	3.0	2.5	1.4	0	25
EPC1007	1.7 x 1.1	EN	100	6	30.0	2.7	0.8	1.0	1.4	0	6
EPC1001	4.1 x 1.6	EN	100	6	7.0	10.5	3.0	3.3	1.4	0	25
EPC1013	1.7 x 0.9	EN	150	6	100.0	1.7	0.4	0.7	1.4	0	3
EPC1011	3.6 x 1.6	EN	150	6	25.0	6.7	1.5	2.8	1.4	0	12
EPC1012	1.7 x 0.9	EN	200	6	100.0	1.9	0.4	0.9	1.4	0	3
EPC1010	3.6 x 1.6	EN	200	6	25.0	7.5	1.5	3.5	1.4	0	12

Table 1: Summary of eGaN FET Electrical Characteristics

Table data subject to change. Please refer to the Product section on www.epc-co.com.

$R_{DS(on)}$ is an excellent indicator of junction temperature; the drawback being calibration of $R_{DS(on)}$ as a function of T_J is a time consuming procedure and requires excellent instrumentation techniques. However, the main advantage of using $R_{DS(on)}$ as a temperature sensitive parameter is that one is actually measuring the heat rise in the exact physical location where the heat is being generated; this is not true for either the body diode V_{SD} or $V_{GS(TH)}$ testing.

There are two steps for calibrating the $R_{DS(on)}$ temperature sensitive parameter. The first step involves calculating the apparent $R_{DS(on)}$ as a function of temperature which involves turning the Device-Under-Test (DUT) "ON" with a high gate voltage so that the device is saturated. For the eGaN FET being evaluated, gate to source voltage (V_{GS}) is +5 Volts. Then the drain to source is biased by a low current, typically 0.3 to 1 Amperes, depending upon die size and associated $R_{DS(on)}$. This calibration current needs to be high enough to get good V_{DS} resolution without simultaneously heating the junction significantly. With these biasing conditions in place, the DUT is placed into an environmental chamber with Kelvin connections to the drain and source along with an appropriate current viewing resistor, typically 0.01 Ω. The environmental chamber temperature is stepped in approximately +25°C increments between +25°C and +125°C, and data is taken, creating a table similar to Table 2. Apparent $R_{DS(on)}$ is calculated from V_{DS} / I_D.

From Table 2, "Table Curve®" Software is used to evaluate the data and create a mathematical function, similar to:

$$y = \exp(a + bx) \quad (1)$$
where x = temperature and $y = R_{DS(on)}$

The second step is to evaluate $R_{DS(on)}$ as a function of drain current (I_D) at +25°C, since $R_{DS(on)}$ is also modulated by I_D. A curve tracer can be used for this task; it is these author's experience though that a curve tracer's pulse time is too long and can create heating within the DUT at higher currents. Therefore, a special $R_{DS(on)}$ vs. I_D test fixture was constructed that can take $R_{DS(on)}$ data in the tens of microseconds. Typically this test is a single point test taken at the DUT's pulse current rating defined in datasheet; this assures that the DUT remains within the saturated area of the output characteristics curve.

A straight line approximation is then made between the high current and low current values at +25°C, using the general equation: $y = mx + c$. Table 3 demonstrates an example output for this function, where $x = I_D$.

Using the formulas derived from the two data sets and subtracting ($R_{DS(on)}$ as a function of I_D) from (apparent $R_{DS(on)}$ as a function of T_J) we get the true $R_{DS(on)}$ as a function of T_J. Note however, $R_{DS(on)}$ as a function of T_J at 25°C minus $R_{DS(on)}$ as a function of I_D at 25°C equals zero. Therefore to correct for this offset, $R_{DS(on)}$ at +25°C must be added back into the equation in order to satisfy all values of T_J.

$$R_{DS(on)} = (R_{DS(on)} @ T_J) - (R_{DS(on)} @ I_D) + (R_{DS(on)} @ 25°C) \quad (2)$$

From the above mathematically generated curve, calculation of thermal resistance R_θ is straight forward. Thermal resistance is given by the general equation:

$$R_\theta = \frac{\Delta T_J}{P_D} \quad (3)$$

The change in junction temperature (ΔT_J) is the temperature at the FET junction at the end of the power pulse minus the starting junction temperature.

$$\Delta T_J = T_{Power\text{-}Pulse} - T_{Ambient} \quad (4)$$

The change in junction temperature ΔT_J is calculated from $R_{DS(on)}$ at the end of the power pulse P_D. Using the values for a and b, derived in equation 1:

$$\Delta T_J = \left(\frac{LN(R_{DS(on)}) - a}{b} \right) - T_{Ambient} \quad (5)$$

It has been demonstrated that thermal resistance is not constant for all junction temperatures; typically these values decrease for lower junction temperatures. Therefore, in order to approximate real world applications manufacturers specify thermal resistance values at or close to data sheet $T_{J(MAX)}$ values. For EPC's eGaN FETs, the $T_{Power\text{-}Pulse}$ temperature is typically +125°C +/- 5°C.

Once the testing procedures for R_θ, and its cousin, thermal impedance, Z_θ, have been established, EPC's eGaN FETs can be evaluated for thermal performance several ways. The following section describes three thermal specifications that are used for these devices.

Temperature °C	Drain-Source Voltage mV	Apparent $R_{DS(on)}$ Calculation Ω
24.9	14.4	0.0180
54.5	17.2	0.0215
79	19.6	0.0245
102	22.08	0.0276
130.2	25.68	0.0321

Table 2: An example data table of $R_{DS(on)}$ vs. Temperature of EPC1010

$R_{DS(on)}$ vs. I_D Curve fit	
c =	0.01803
m =	0.000298
I_D	$R_{DS(on)}$
1	0.01833
2	0.01863
5	0.01953
10	0.02101
20	0.02399
40	0.02995

Table 3: An example data table of $R_{DS(on)}$ vs. I_D of EPC1010

About The Authors

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$R_{\theta JB}$: Thermal Resistance – Junction to Solder Bump

$R_{\theta JB}$ is perhaps the most important thermal specification since it will be used by the majority of applications. As seen in Figure 1, $R_{\theta JB}$ is the thermal resistance from the device junction to the bottom of the solder bumps without consideration of the type or size of the mounting circuit board. Therefore, if the end user knows the thermal characteristics and environment of the application, thermal resistances of all the sub-parts can be added algebraically in order to arrive at the total thermal resistance of the total system.

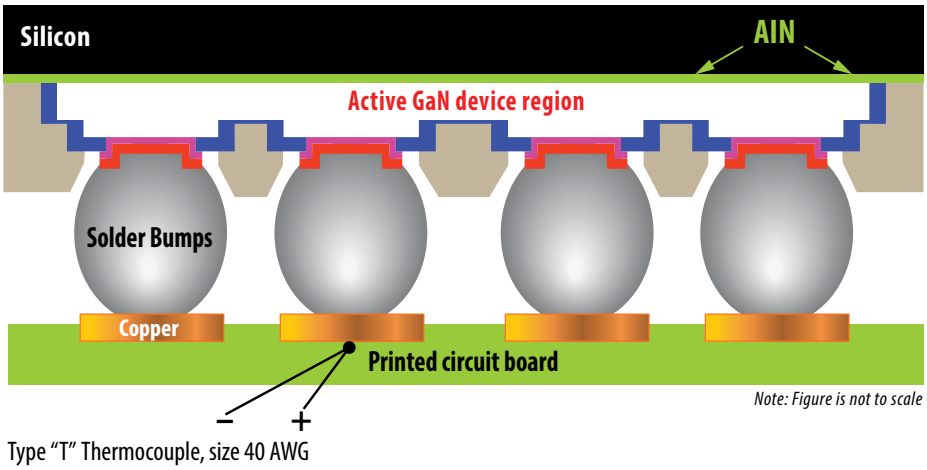

Figure 1: $R_{\theta JB}$ is the thermal resistance from the device junction to the bottom of the solder bumps without consideration of the type or size of the mounting circuit board.

$R_{\theta JC}$: Thermal Resistance – Junction-to-Case

$R_{\theta JC}$ is given for those situations where the end user wishes to add additional heat-sinking to the top of the eGaN FET. Figure 2 shows a typical test set up for measuring $R_{\theta JC}$.

The water cooled heat-sink in Figure 2 is temperature regulated by a re-circulating heater-chiller so that +25°C is constantly maintained. The "QFN board" is a very small and simple test circuit board allowing for electrical connections to the DUT. The thermally non-conductive "Shim Spacer" was added to very small devices to prevent device tilting and alignment problems. The 10 Ω resistor prevents possible gate oscillations since the leads between the DUT and the test circuitry are on the order of 0.3 meters in length. All power leads have Kelvin connections back to the instrumentation in order to eliminate the IxR drops in the power leads. The thermal interface material between the DUT and the water cooled heat sink is water with a small amount of surfactant added in order to increase surface wetting. The DUT system is held in place by pneumatic pressure. The thermocouple monitors heat dissipated through the solder bumps and circuit board in order to only evaluate the heat removed by the water cooled heat sink, thus calculating a true $R_{\theta JC}$.

$R_{\theta JA}$: Thermal Resistance – Junction-to-Ambient

$R_{\theta JA}$ (junction to ambient thermal resistance) is one way of specifying the thermal resistance with the device mounted onto a 1 square inch circuit board. Figure 3 shows the circuit board layout used for the thermal resistance measurement. The DUT is mounted onto a single sided, 2 ounce FR-4 circuit board with an area of 1 square inch (645.16 mm^2). One-half square inch is connected to the source, and one-half square inch is connected to the drain through the device's solder bars.

$R_{\theta JA}$ is most useful for those situations where the end user wants to mount the eGaN FET onto the application's circuit board with no additional heat sinking. During device characterization the DUT is suspended in the center of a one-cubic-foot (0.02832 cubic-meters) closed box, in still air, at 25°C starting temperature. The DUT is biased "ON" for 1000 seconds at a junction temperature of +125°C. $R_{\theta JA}$ is then calculated according to equation 3.

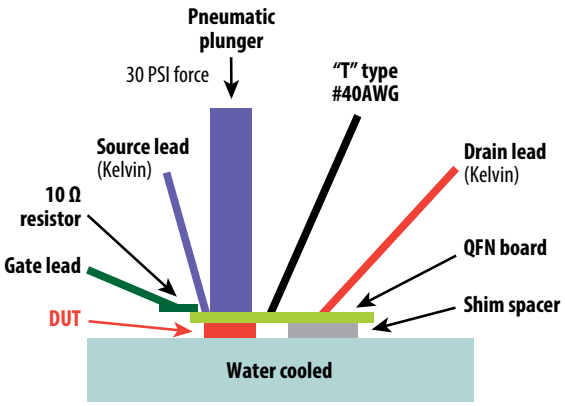

Figure 2: A typical test set up for measuring $R_{\theta JC}$

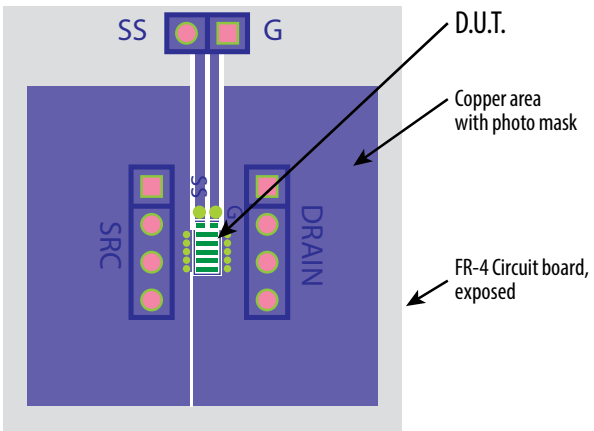

Figure 3: Circuit board layout for $R_{\theta JA}$ measurement with 1 in^2 copper area. Half of the Cu is connected to the source and the other half is connected to the drain.

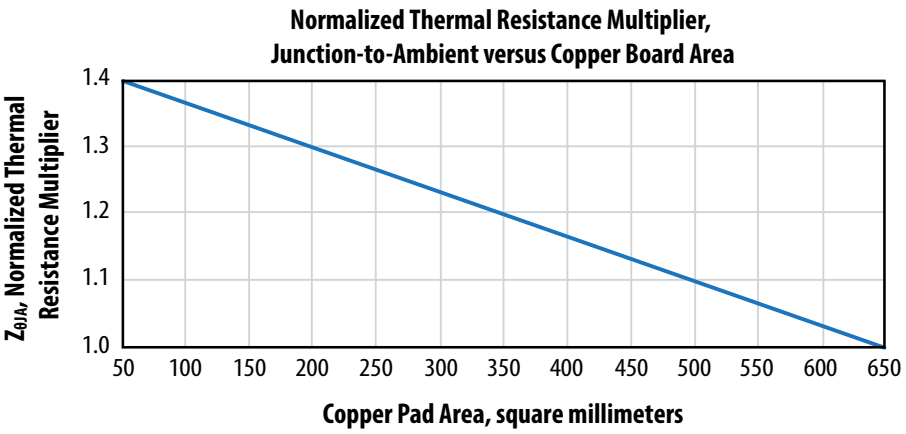

Figure 4: Thermal resistance as a function of decreasing copper pad area, normalized to 645.16 mm^2.

Part Number	Side 1 mm	Side 2 mm	Die Area mm^2	$R_{\theta JC}$ °C/Watt	$R_{\theta JB}$ °C/Watt	$R_{\theta JA}$ °C/Watt
EPC1001	1.6	4.1	6.56	1.56	15	54
EPC1007	1.1	1.7	1.87	6.5	32	80
EPC1010	1.6	3.6	5.76	1.8	16	56
EPC1012	0.9	1.7	1.53	8.2	36	85
EPC1014	1.1	1.7	1.87	6.5	32	80
EPC1015	1.6	4.1	6.56	1.56	15	54

Table 4: Thermal Resistance Summary

Since applications are not necessarily designed around a perfect one-square-inch (645.16 square millimeters) circuit board, Figure 4 demonstrates the increasing thermal resistance as a function of decreasing copper pad area, normalized to 645.16 square millimeters (1 square inch).

Measurement Results

Table 4 lists the various thermal resistances, $R_{\theta JC}$, $R_{\theta JB}$, and $R_{\theta JA}$, as related to their device parts numbers. The thermal resistance values for EPC1010 and EPC1012 were measured and the thermal resistance values for other part numbers were scaled as approximations. Figure 5 shows the normalized $Z_{\theta JB}$ Curve set for EPC's product line. During device characterization it was found that the normalized thermal impedance curves ($Z_{\theta JB}$) were nearly identical for both the EPC1010 and EPC1012.

Conclusions

Surface mount transistors such as the eGaN FET can be physically mounted several ways. Depending upon the user's application the method of device mounting has significant impact on power dissipation and maximum current capability. The limiting factor in all these device parameters is controlling maximum junction temperature of the discrete device. The best known method for measuring junction temperature for eGaN FETs is through characterizing and measuring changes in $R_{DS(on)}$. This application note has shown an acceptable methodology and the resulting thermal resistances results for various devices.

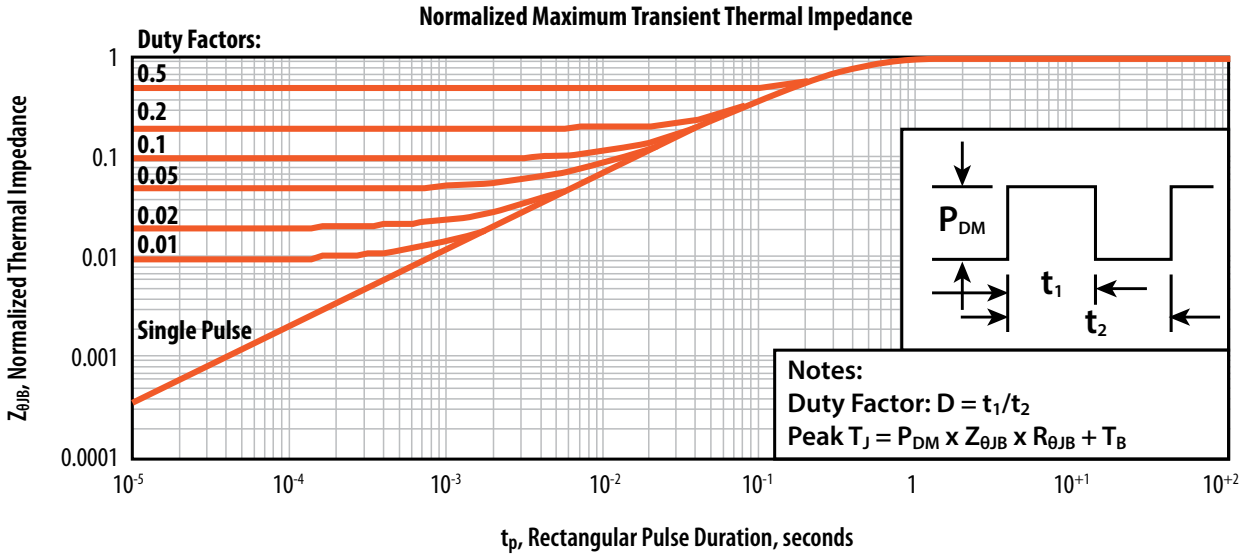

Figure 5: Normalized $Z_{\theta JB}$ Curve set for EPC's product line.