EPC eGaN® FETs Reliability Testing: Phase 11

Alejandro Pozo Ph.D., Shengke Zhang Ph.D., Ricardo Garcia, John Glaser Ph.D., Zhikai Tang Ph.D., and Robert Strittmatter Ph.D., Efficient Power Conversion Corporation, El Segundo, CA

The rapid adoption of Efficient Power Conversion (EPC) Corporation's eGaN® devices in many diverse applications calls for continued accumulation of reliability statistics and research into the fundamental physics of failure in GaN devices. This Phase 11 reliability report adds to the growing knowledge base published in the first ten reports [1-10] and covers several key new topics.

Because GaN is a relatively new semiconductor technology compared to traditional Si MOSFETs, many customers request additional testing beyond AEC-Q101 standards, as well as a deeper understanding of the unique mechanisms that could lead to device failures. In this report, several examples of this kind of additional testing are presented.

Gallium nitride (GaN) power devices have been in volume production since March 2010 [11] and have established a remarkable field reliability record. This article will discuss the strategy used to achieve this track record that relied upon tests forcing devices to fail under a variety of conditions to create stronger and stronger products for the industry.

NEED FOR ADDITIONAL STANDARD QUALIFICATION TESTING

Why test-to-fail in addition to standard qualification testing?

Standard qualification testing for semiconductors typically involves stressing devices at-or-near the limits specified in their data sheets for a prolonged period of time, or for a certain number of cycles. The goal of qualification testing is to have zero failures out of a relatively large group of parts tested.

This type of testing is inadequate since it only reports parts that passed a very specific test condition. By testing parts to the point of failure an understanding of the amount of margin between the data sheet limits can be developed, and more importantly, an understanding of the intrinsic failure mechanisms can be found. By knowing the intrinsic failure mechanisms, the root cause of failure, and the device's behavior over time, temperature, electrical or mechanical stress, the safe operating life of a product can be determined over a more general set of operating conditions (For an excellent description of this methodology for testing semiconductor devices see reference [12]).

Key Stress Conditions and Intrinsic Failure Mechanisms for GaN Power Devices

What are the key stress conditions encountered by GaN power devices and what are the intrinsic failure mechanisms for each stress condition?

As with all power transistors, the key stress conditions involve voltage, current, temperature, and humidity, as well as various mechanical stresses. There are, however, many ways of applying these stress conditions. For example, voltage stress on a GaN FET can be applied from the gate terminal to the source terminal (V_{GS}), as well as from the drain terminal to the source terminal (V_{DS}). For example, these stresses can be applied continuously as a DC bias, they can be cycled on-and-off, or they can be applied as high-speed pulses. Current stress can be applied as a continuous DC current, or as a pulsed current. Thermal stresses can be applied continuously by operating devices at a predetermined temperature extreme for a period of time, or temperature can be cycled in a variety of ways.

By stressing devices with each one of these conditions to the point of generating a significant number of failures, an understanding of the primary intrinsic failure mechanisms for the devices under test can be determined. To generate failures in a reasonable amount of time the stress conditions typically need to significantly exceed the data sheet limits of the product. Care needs to be taken to make certain the excess stress condition does not induce a failure mechanism that would never be encountered during normal operation. To make certain this is not the case, the failed parts need to be carefully analyzed to determine the root cause of their failure. Only by verifying the root cause can a true understanding of the behavior of a device under a wide range of stress conditions be developed.

Stressor	Device/ Package	Method	Intrinsic Failure Mechanism	Evidence
Voltage	Device	HTGB	Dielectric failure (TDDB)	This Report
			Threshold shift	
		HTRB	Threshold shift	This Report
			$R_{DS(on)}$ shift	
		ESD	Dielectric rupture	[2,3,6,7,8,9,10]
Current	Device	DC Current (EM)	Electromigration	In Progress
			Thermomigration	In Progress
Current + Voltage (Power)	Device	SOA	Thermal Runaway	This Report
		Short Circuit	Thermal Runaway	This Report
Voltage Rising/Falling	Device	Hard-switching reliability	$R_{DS(on)}$ shift	This Report
Current Rising/Falling	Device	Pulsed Current (Lidar reliability)	None found	This Report
Temperature	Package	HTS	None found	[6,7,8,9]
Humidity	Package	MSL1	None found	[3,4,5,6,7,8,9,10]
		H3TRB	None found	[1,2,3,4,5,6,7,8,9,10]
		AC	None found	[4,5,6,7,8,9]
		uHAST	None found	[10]
Thermo-mechanical	Package	TC	Solder Fatigue	[1,2,3,4,5,6,7,8,9,10]
		IOL	Solder Fatigue	[7,8,9,10]
Mechanical	Package	Bending force test	Delamination	In Progress
		Die shear	Solder Strength	This Report
		Package force	Film Cracking	This Report

Table 1: Stress Conditions and Intrinsic Failure Mechanisms for eGaN FETs

FOCUS AND STRUCTURE OF THIS REPORT

In this Phase 11 report the focus is on the areas highlighted in the right-hand column of Table 1. The first topic will discuss the intrinsic failure mechanisms impacting the gate electrode of eGaN devices. This is perhaps the simplest analysis with the clearest conclusions, and therefore was selected to go first in this report.

The second section discusses the intrinsic mechanisms underlying dynamic $R_{DS(on)}$. The topic of dynamic $R_{DS(on)}$ has garnered much attention from design engineers, reliability experts, and academics. In this section, the key mechanisms are separated and how the understanding of these mechanisms can be used to create more robust devices is shown.

Section 3 focuses on the safe operating area (SOA) of eGaN devices. This subject has been studied extensively in silicon-based power MOSFETs, where a secondary breakdown mechanism is observed that limits their utility under high drain bias conditions [13]. Several eGaN products were tested exhaustively throughout their data sheet SOA, and then taken to failure to probe the safety margins. In all cases, the data shows that eGaN FETs will not fail when operated within the data sheet SOA.

In Section 4, eGaN devices are tested to destruction under short-circuit conditions. The purpose is to determine how long and what energy density they withstand before catastrophic failure. The information is vital to industrial power and motor drive engineers needing to include short-circuit protection in their designs. The data demonstrates that failure is thermally limited, and withstand time exceeds 10 µs at recommended gate drive.

eGaN devices have been extensively applied in light detection and ranging (lidar) equipment used on autonomous cars, truck, robots, and drones. The fast switching speed, small size, and high pulsed current capabilities of eGaN devices add to a lidar system's ability to "see" at a greater distance with higher resolution. Lidar systems push the limits on dynamic voltage and current (di/dt and dv/dt) beyond anything experienced in silicon. In Section 5, a custom test system to assess eGaN reliability over long-term lidar pulse stress conditions is described. To date, devices have now passed over four trillion pulses (a typical automotive lifetime) without either failure or significant parametric drift.

In Section 6 the subject of mechanical force testing of eGaN's wafer level chip scale (WLSC) package is presented. Test-to-fail results for die shear (in-plane force) demonstrate robustness that exceeds MIL-STD-883E recommendations. In addition, backside pressure (out of plane) tests show the package is capable of 400 psi without failure.

Section 7 provides a brief update on field reliability statistics.

SECTION 1: VOLTAGE/TEMPERATURE STRESS ON THE GATE

Figure 1 is an example of a Weibull plot of gate failures in an EPC2212 [14] eGaN® FET from Efficient Power Conversion (EPC). The horizontal axis shows the time to failure. The vertical axis shows the cumulative failure probability for different stress conditions applied to the gate.

The plot on the left has different voltages at room temperature and the plot on the right shows two different voltages applied at 120°C. Note that this device has a data sheet maximum gate voltage rating of 6 V, yet very few devices are failing even after many hours at 8 V.

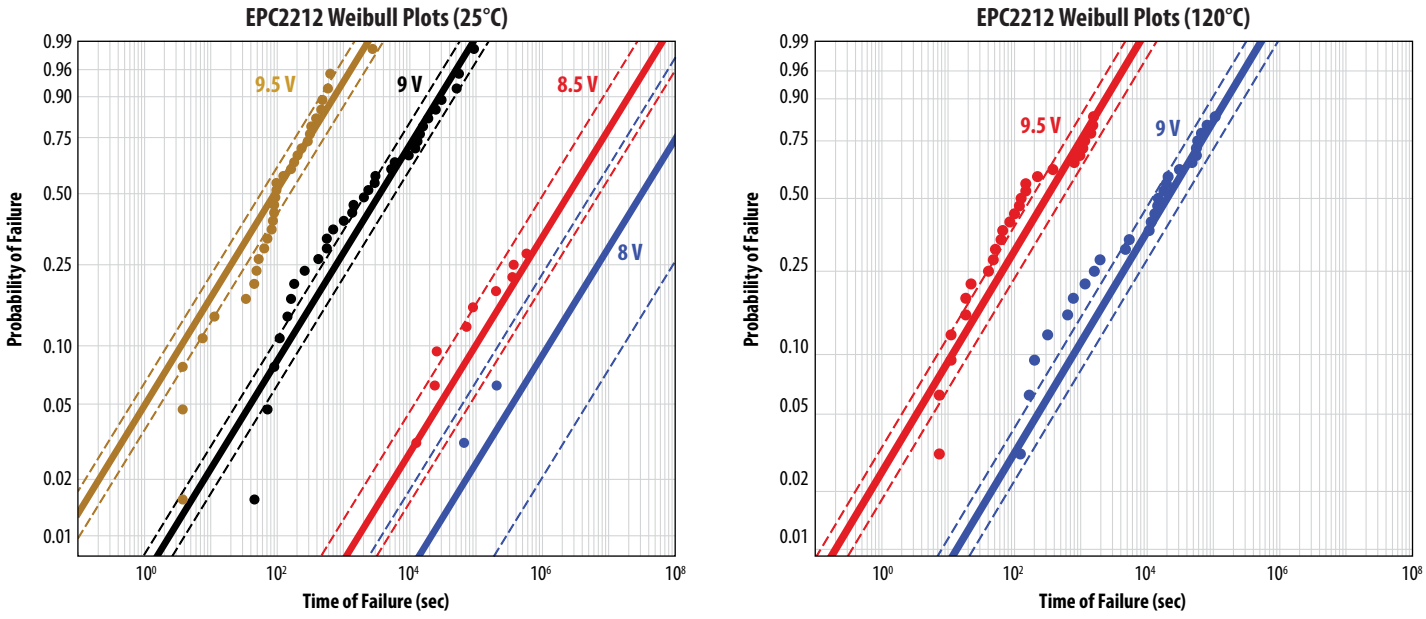


Figure 1: Weibull plots of gate-to-source failures of EPC2212. Note that very few failures occur even at 8 V V_{GS}, yet the device has a maximum V_{GS} rating of 6 V. The data on the left is at 25°C and the data on the right is at 120°C.

In Figure 2 these data have been translated into failure rates. On the left is the mean time to failure (MTTF) for these same devices versus V_{GS} at both 25°C and 120°C. On the right is a graph that shows the various probabilities of failure versus V_{GS} at 25°C. Note that the failure rate is not very sensitive to temperature but is very sensitive to V_{GS}.

Looking at the graph on the right, with a V_{GS} of 6 V DC (The absolute maximum allowed voltage for this part) one could expect between 10 and 100 parts per million (ppm) failures in 10 years. The recommended gate drive voltage, however, is 5.25 V and the expected failure rate at that voltage is less than 1 ppm in 10 years.

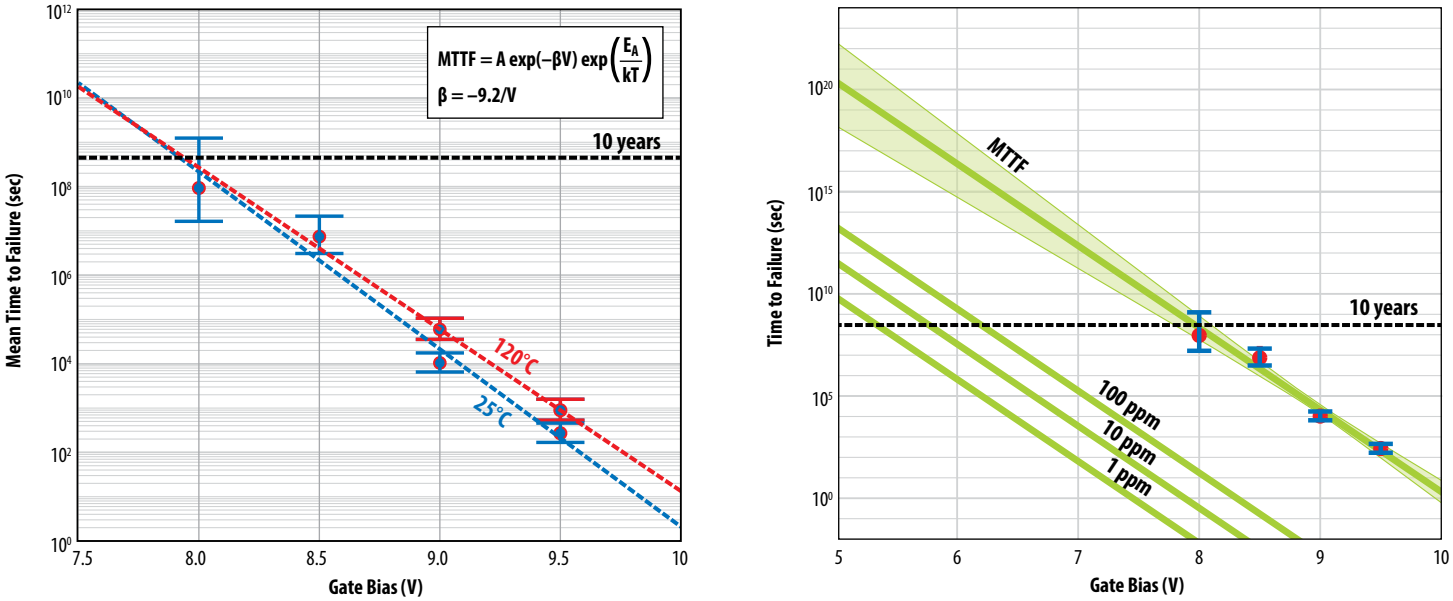


Figure 2: On the left is the mean time to failure (MTTF) for EPC2212 eGaN FETs versus V_{GS} at both 25°C and 120°C. On the right is a graph that shows the various probabilities of failure versus V_{GS} at 25°C.

These conclusions are only valid if the primary failure mechanism is the same under all these conditions. In order to confirm this, failure analysis was performed on the failed parts and a uniform result was found, as shown in Figure 3. Referring to the image in Figure 3, the yellow circle shows that the failure site is between the gate metal and the metal 1 layer.

In the case of the EPC2212, these two layers are separated by a silicon nitride layer. It is this silicon nitride layer that failed, not any of the GaN layers beneath. Knowing this failure mechanism and understanding that it is consistent with time-dependent dielectric failure mechanisms (TDDB) commonly found in dielectric layers in most semiconductors, the probability data in Figure 2 to predict failure rates due to gate voltage stress within data sheet limits can be used with confidence.

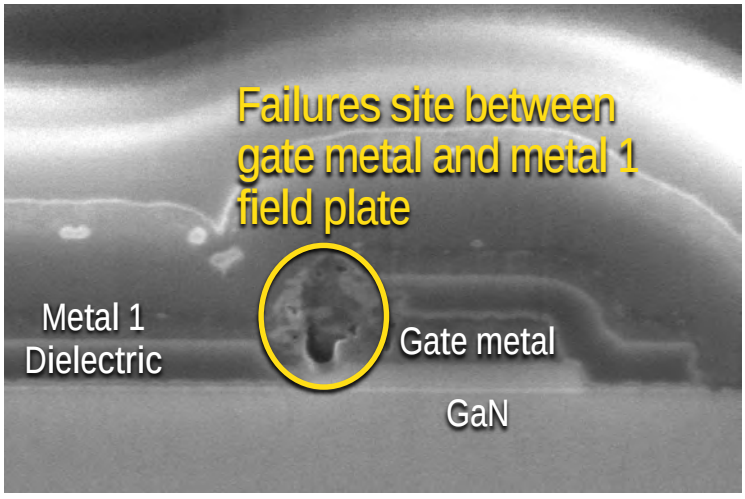


Figure 3: Scanning electron microscopy (SEM) image of the gate region of an EPC2212 eGaN FET. The yellow circle shows the failure site is between the gate metal and the metal 1 layer.

SECTION 2: VOLTAGE/TEMPERATURE STRESS ON THE DRAIN

This same methodology can be applied to every other stress condition. For example, one common concern among GaN transistor users is dynamic on-resistance. This is a condition whereby the on-resistance of a transistor increases when the device is exposed to high drain-source voltage (V_{DS}). The traditional way to test for this condition is to apply maximum-rated DC V_{DS} at maximum rated temperature (typically 150°C). If there are no failures after a certain amount of time – usually 1000 hours – the product is considered good.

The mechanism causing the on-resistance to increase is the trapping of electrons in trap-states near the channel. As the trapped charge accumulates, it depletes electrons from the two-dimensional electron gas (2DEG) in the ON state, leading to an increase in $R_{DS(on)}$. By applying DC V_{DS} at maximum temperature, the electrons available to be trapped come from the drain-source leakage current, I_{DSS}. In order to accelerate trapping, devices can be taken to voltages above their rated maximum, as shown in Figure 4 for a fourth-generation, 100 V-rated EPC2212 eGaN FET. The data was fit by 3-parameter Weibull.

In Figure 5 these data have been translated into time-to-fail graphs versus voltage and temperature. On the right side of the graph is shown the time for 1 ppm failures (0.0001%) at the maximum rated V_{DS} is over 10 years. What is unusual, however, is that the graph on the left shows that the failure rates are not very sensitive to temperature and that the failure rates, although extraordinarily low under all conditions, are lower at 90°C than at either 35°C or 150°C. It will be shown later in this article that this can be explained by understanding that the primary failure mechanism is hot electron trapping.

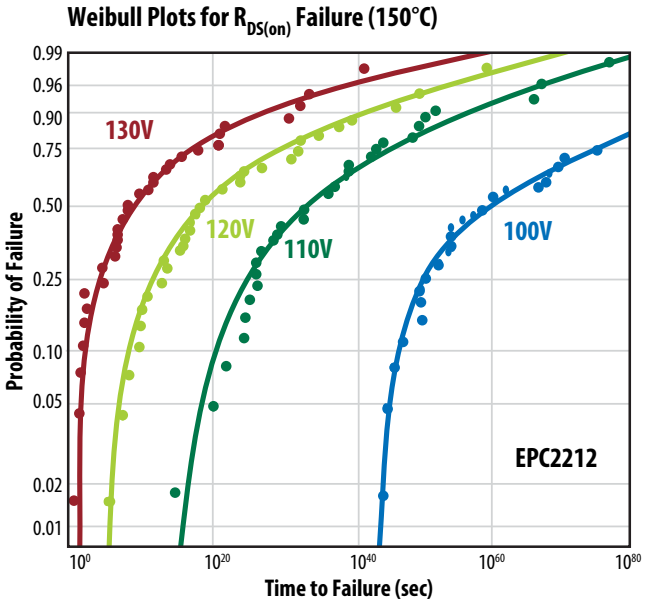
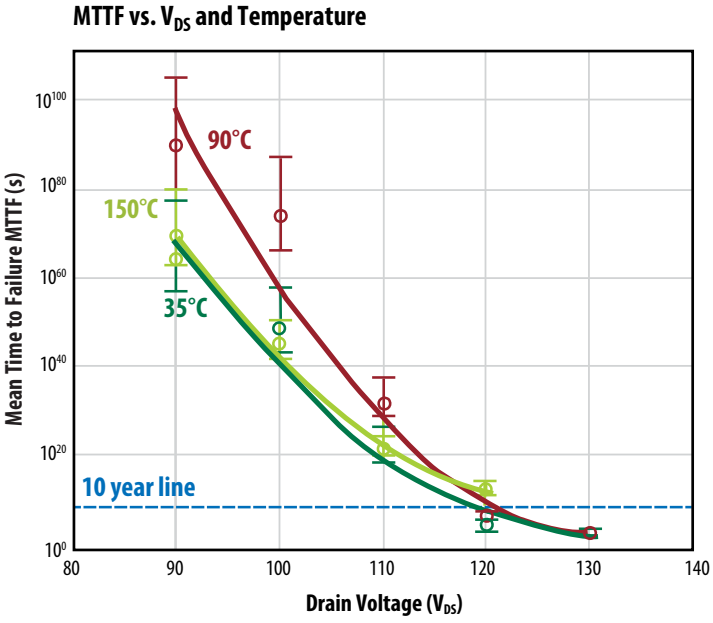


Figure 4: Weibull plot of EPC2212 eGaN FETs stressed under DC bias at various voltages. A failure is defined as exceeding data sheet limits.



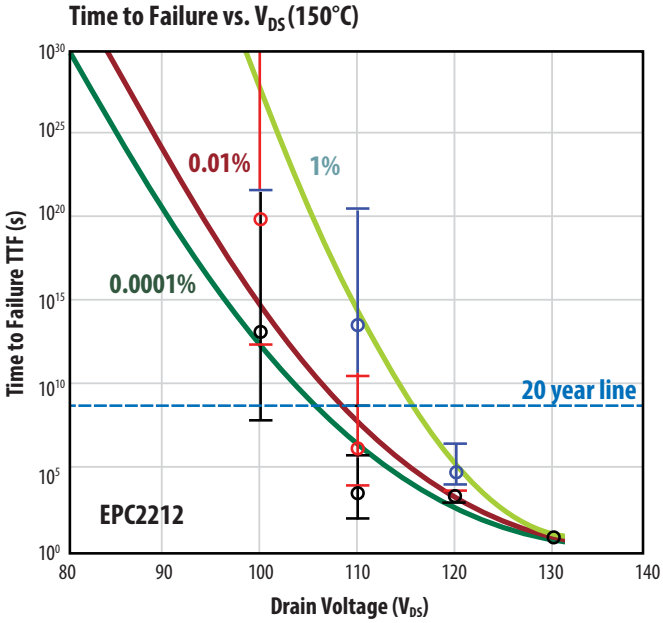


Figure 5: The data in Figure 4, as well as similar data taken at different temperatures, is translated into predictions of failure rates over time, temperature, and voltage.

Figure 6 is a magnified image of an EPC2212 eGaN FET showing thermal emissions in the 1–2 µm optical range. Emissions in this part of the spectrum are consistent with hot electrons and their location in the device is consistent with the location of the highest electric fields when the device is under drain-source bias.

Knowing that hot electrons in this region of the device are the source of trapped electrons. A better understanding of how to minimize the dynamic on-resistance can be achieved with improved designs and processes. By understanding the general behavior of hot electrons, their behavior over a wider range of stress conditions can be generalized.

In addition, by providing more hot electrons, the trapping mechanism can be accelerated. To do this, the circuit shown in Figure 7 that pushes high I_{DSS} through the device at maximum rated V_{DS} was created. In other words, instead of just using the leakage current generated by DC bias at high temperatures as the source of electrons that can get trapped, orders of magnitude more trapping candidates by making a switching circuit such as shown in Figure 7 can be generated. This circuit is one of the proposed hard switching topologies by JEDEC JEP173 [15].

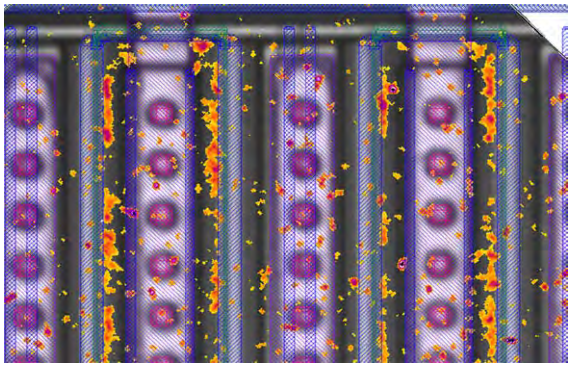


Figure 6: A magnified image of an EPC2212 eGaN FET showing light emission in the 1–2 µm wavelength range (SWIR) that is consistent with hot electrons. The SWIR emission (red-orange) has been overlaid on a regular (visible wavelength) microscope image.

Figure 7: Hard switching circuit consistent with JEDEC JEP173 [15]

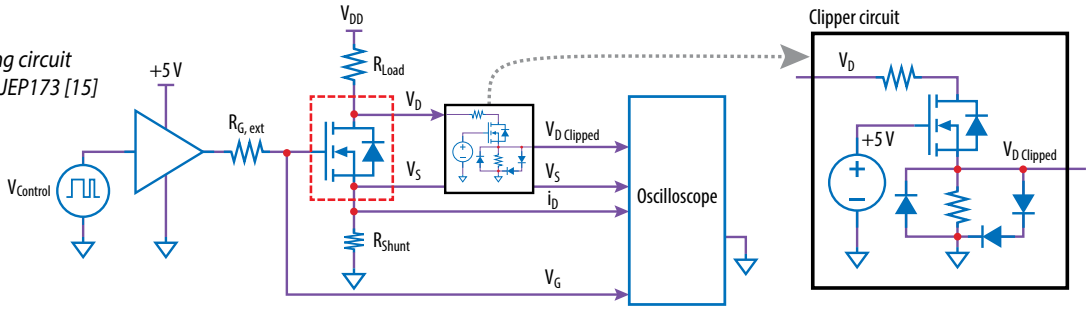


Figure 8 shows how the $R_{DS(on)}$ of a fifth-generation EPC2045 eGaN FET [16] increases over time at various voltage stress levels and temperatures. On the left, the devices were tested at 25°C at voltages from 60 V to 120 V (EPC2045 has a $V_{DS(max)}$ of 100 V). The horizontal axis is time measured in seconds, with the right side ending at 10 years.

The graph on the right shows the evolution of $R_{DS(on)}$ when biased at 120 V at different temperatures. The counter-intuitive result shows that the on-resistance increases faster at lower temperatures. This is consistent with hot carrier injection because hot electrons travel further at lower temperatures and therefore can get to different layers where they are more prone to become trapped. This suggests that traditional testing methods, whereby a device is tested at maximum voltage and temperature, may not be enough to determine the reliability of a device.

The results in Figure 5 as well can now be better understood. As the device is heated under DC bias, the leakage current increases. The shorter travel distance of the hot carriers, however, counters this increase in available electrons such that the $R_{DS(on)}$ increase over time decreases from room temperature to 90°C, but then starts increasing at higher temperatures – another counter-intuitive result.

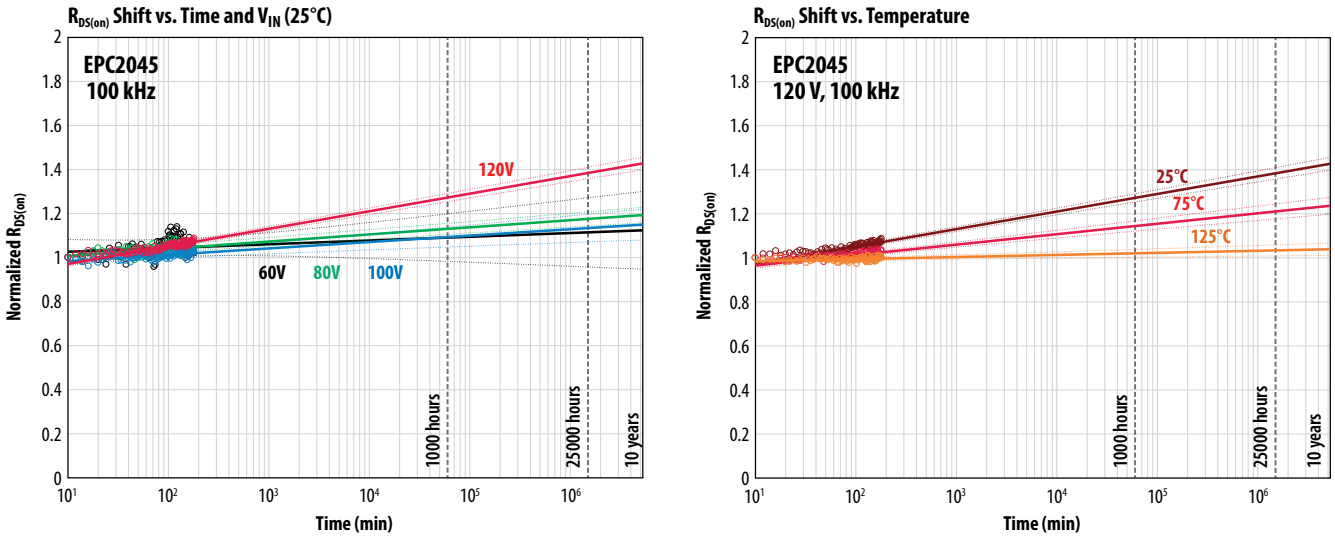


Figure 8: The $R_{DS(on)}$ of a fifth-generation EPC2045 eGaN FET over time at various voltage stress levels and temperatures. On the left, the devices were tested at 25°C at voltages from 60 V to 120 V. The graph on the right shows the evolution of $R_{DS(on)}$ at 120 V at various temperatures.

SECTION 3: SAFE OPERATING AREA

Safe operating area (SOA) testing exposes the eGaN FET to simultaneous high current (I_D) and high voltage (V_{DS}) for a specified pulse duration. The primary purpose is to verify the FET can be operated without failure at every point (I_D, V_{DS}) within the data sheet SOA graph. It is also used to probe the safety margins by testing to fail outside the safe zone.

During SOA tests, the high-power dissipation within the die leads to a rapid rise in junction temperature and the formation of strong thermal gradients. For sufficiently high power or pulse duration, the device simply overheats and fails catastrophically. This is known as thermal overload failure.

In Si MOSFETs, another failure mechanism known as secondary breakdown (or Spirito effect [13]) has been observed in SOA testing. This failure mode, which occurs at high V_D and low I_D, is caused by an unstable feedback between junction temperature and threshold V_{TH}. As the junction temperature rises during a pulse, V_{TH} drops, which can cause pulse current to rise. The rising current, in turn, causes temperature to rise faster, thereby completing a positive feedback loop that leads to thermal runaway and ultimate failure. A goal of this study is to determine if the Spirito effect exists in eGaN FETs.

EPC designed and built a custom Safe Operating Area test system for eGaN FETs. The system is described in detail in Appendix C. In brief, the circuit works similar to a curve tracer. The gate bias on the device under test (DUT) is set before the pulse and is used to modulate the ultimate pulse current. The drain voltage is then pulsed onto the drain by means of a p-channel control FET for a specified pulse duration.

For DC, or long-duration pulses, the SOA capability of the FET is highly dependent on the heat sinking of the device. This can present a huge technical challenge to assess the true SOA capability, often requiring specialty water-cooled heatsinks. However, for short pulses (< 1 ms), the heat sinking does not impact SOA performance. This is because on short timescales, the heat generated in the junction does not have sufficient time to diffuse to any external heatsink. Instead, all of the electrical power is converted to raising the temperature (thermal capacitance) of the GaN film and nearby silicon substrate. As a result of these considerations, SOA tests were conducted at two pulse durations: 1 ms and 100 µs.

Figure 9 shows the SOA data of 200 V EPC2034C. In this plot, individual pulse tests are represented by points in (I_D, V_{DS}) space. These points are overlaid on the data sheet SOA graph. Data for both 100 µs and 1 ms pulses data are shown together. Green dots correspond to 100 µs pulses in which a part passed, whereas red dots indicate where a part failed. A broad area of the SOA was interrogated without any failures (all green dots), ranging from low V_{DS} all the way to $V_{DS;max}$ (200 V). All failures (red dots) occurred outside the SOA, indicated by the green line in the data sheet graph. The same applies to 1 ms pulse data (purple and red triangles): all failures occurred outside of the data sheet SOA.

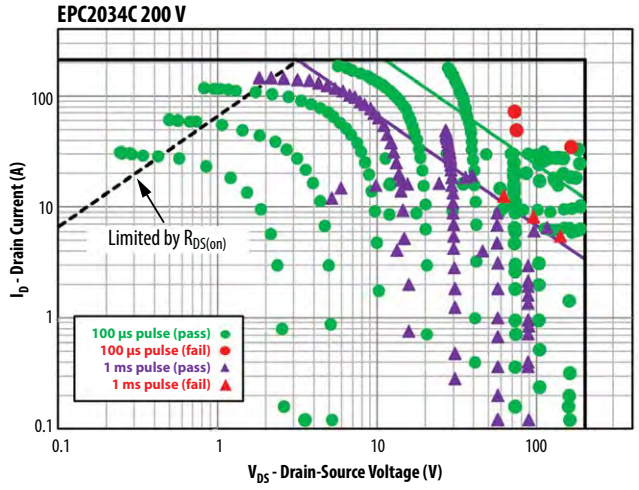


Figure 9: EPC2034C SOA plot. The "Limited by $R_{DS(on)}$" line is based on data sheet maximum specification for $R_{DS(on)}$ at 150°C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that all failures occur outside the data sheet SOA region.

Figure 10 provides SOA data for three more parts, AEC EPC2212 (4th generation automotive 100 V), EPC2045 (5th generation 100 V), and EPC2014C (4th generation 40 V). In all cases, the data sheet safe operating area has been interrogated without failures, and all failures occur outside of SOA limits, often well outside the limits.

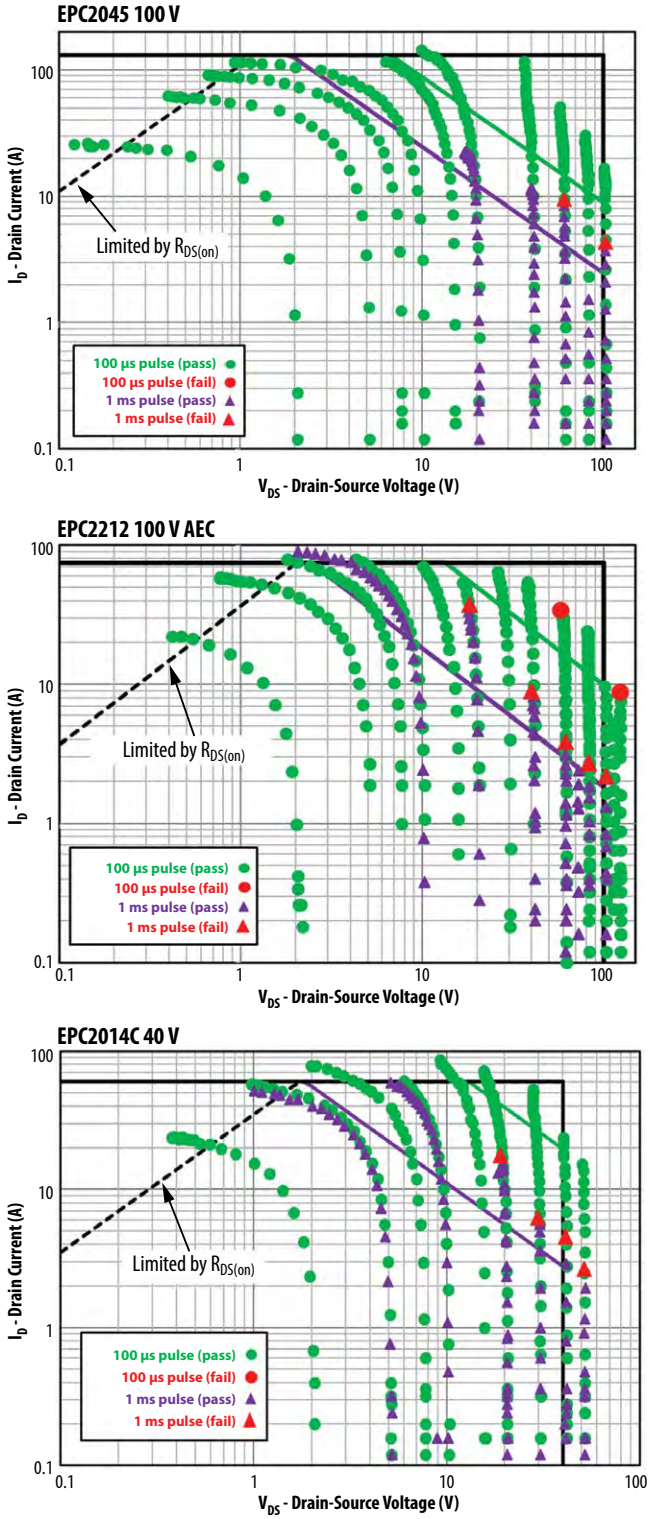


Figure 10: SOA results for EPC2045, EPC2212, EPC2014C. Measurements for 1 ms (purple triangles) and 100 µs (green dots) pulses are shown together. Failures are denoted by red triangles (1 ms) or red dot (100 µs). Note that for all parts, all failures occur outside the data sheet SOA region.

The data sheet SOA graph is generated with finite element analysis, using a thermal model of the device including all relevant layers along with their heat conductivity and heat capacity. Based on transient simulations, the SOA limits are determined by a simple criterion: for a given pulse duration, the power dissipation must be such that the junction temperature does not exceed 150°C before the end of the pulse. This criterion results in limits based on constant power, denoted by the 45° green (100 µs) and purple (1 ms) lines in the SOA graph. This approach leads to a data sheet graph that defines a conservative safe operating zone, as evidenced by the extensive test data in this study. In power MOSFETs, the same constant power approach leads to an over-estimate of capability in the high voltage regime, where failure occurs prematurely due to thermal instability (Spirito effect).

However, from the perspective of the physics of failure, it is evident from Figure 10 that in certain cases the eGaN FETs can survive well outside of the nominal safe zone, but the operating margin decreases at higher drain-source bias and longer pulse durations. To gain deeper knowledge of the mechanisms at play, EPC plans to conduct further test-to-fail studies at higher V_{DS} (beyond data sheet max) and longer pulse durations. These studies will require the addition of device heat-sinking to get meaningful results. The measurement technology is continuing to be refined and failed devices are being dissected to look for intrinsic failure mechanisms.

While the exact physics of failure may still be unknown, the main outcome of this study is clear – *eGaN FETs will not fail when operated within their data sheet SOA*.

SECTION 4: SHORT CIRCUIT ROBUSTNESS TESTING

Short-circuit robustness refers to the ability of a FET to withstand unintentional fault conditions that may occur in a power converter while in the ON (conducting) state. In such an event, the part will experience the full bus voltage combined with a current that is limited only by the inherent saturation current of the transistor and the circuit parasitic resistance, which varies with the application and location of the fault. If the short-circuit state is not quenched by protection circuitry, the extreme power dissipation will ultimately lead to thermal failure of the FET. The goal of short-circuit testing is to quantify the "withstand time" the part can survive under these conditions. Typical protection circuits (e.g. de-saturation protection for IGBT gate drivers) can detect and react to over-current conditions in 2-3 µs. It is therefore desirable, if the eGaN FET can withstand unclamped short-circuit conditions, for about 5 µs or longer.

The two main test circuits used for short-circuit robustness evaluation are [17]:

- Hard-switched fault (HSF): gate is switched ON (and OFF) with drain voltage applied
- Fault under load (FUL): drain voltage is switched ON while gate is ON

For this study, EPC tested parts in both fault modes and found no significant differences in the withstand time. Therefore, the focus will be on FUL results for the remainder of this discussion. However, it is important to note that from HSF testing, eGaN FETs did not exhibit any latching or loss of gate control that can occur in silicon-based IGBTs [17]. This result was expected given the lack of parasitic bipolar structures with the eGaN devices. Until the time the FETs fail catastrophically, the short-circuit can be fully quenched by switching the gate LOW, an advantageous feature for protection circuitry design. Full details of the test methodology are provided in Appendix D.

Two representative eGaN FETs were tested:

(i) EPC2203 (80 V): 4th generation automotive grade (AEC) device

(ii) EPC2051 (100 V): 5th generation device

These devices were chosen because they are the smallest in their product families. This simplified the testing owing to the high currents required for short-circuit evaluation. However, based on simple thermal scaling arguments, the withstand time is expected to be identical for other in-family devices. EPC2203 results cover EPC2202, EPC2206, EPC2201 and EPC2212; EPC2051 covers EPC2045 and EPC2053.

Figure 11 shows fault under load data on EPC2203 for a series of increasing drain voltages. With V_{GS} at 6 V (the data sheet max), and a 10 µs drain pulse, the device did not fail all the way up to V_{DS} of 60 V. Under these conditions, over 3 kW is dissipated in a 0.9 mm x 0.9 mm die. At the higher V_{DS}, the current is seen to decay over time during the pulse. This is a result of rising junction temperature within the device and does not signify any permanent degradation.

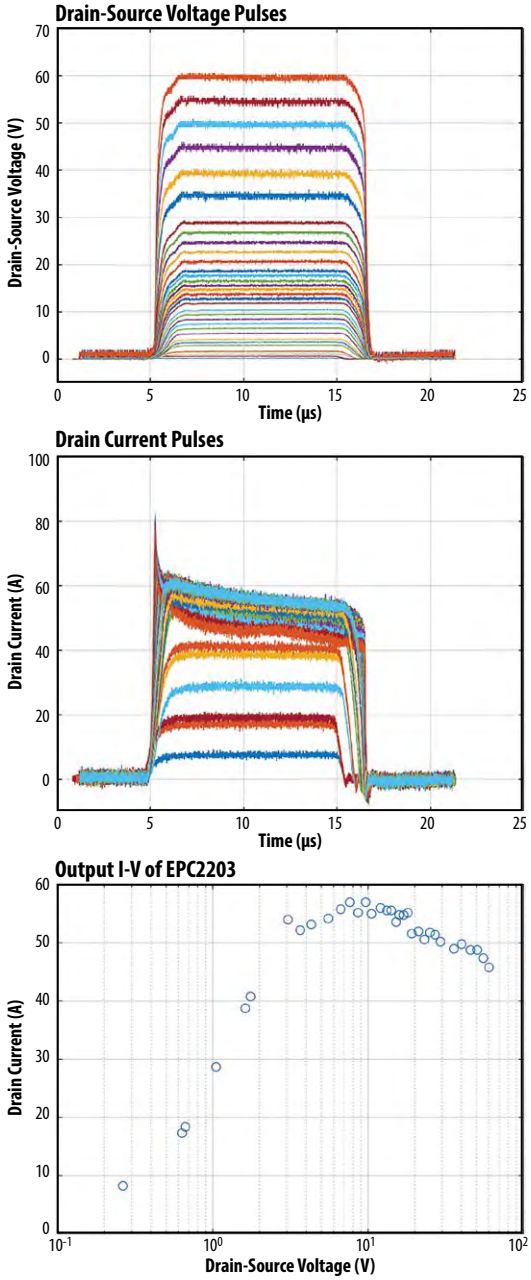


Figure 11: EPC2203 fault under load test waveforms for a series of increasing drain voltages. Drain pulse is 10 µs and V_{GS} = 6 V. The device did not fail for this pulse width. (top) V_{DS} vs. time. V_{DS} is Kelvin sensed directly at the device terminals. (bottom) I_{DS} vs. time. Note that I_{DS} decreases over time due to self-heating. (middle) Resulting output curve for this test sequence. Drain current is reported as the average current during the pulse. Drain current rolls over in the saturation region owing to device heating at higher V_{DS}.

Using a longer pulse duration (25 µs), the parts eventually fail from thermal overload. Representative waveforms are shown in Figure 12. The time of failure is marked by the abrupt sharp rise in drain current. After this event, the devices are permanently damaged. The withstand time is measured from the beginning of the pulse to the time of failure.

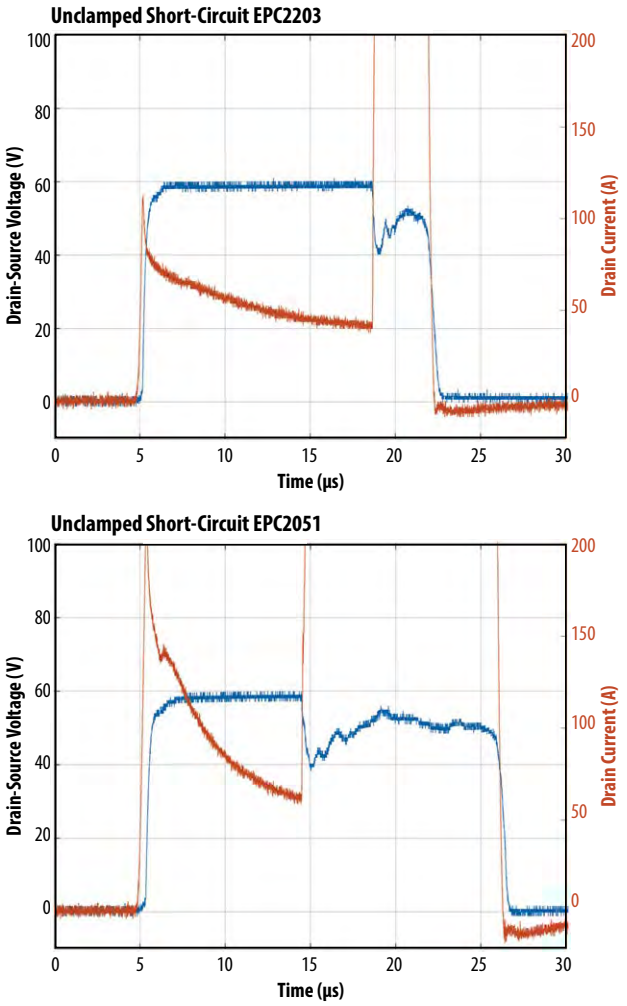


Figure 12: Fault under load test waveforms for a typical EPC2203 (top) and EPC2051 (bottom) at V_{DS} = 60 V, V_{GS} = 6 V and a 25 µs drain pulse. The abrupt rise in drain current marks the time of catastrophic thermal failure.

To gather statistics on the withstand time, cohorts of eight parts were tested to failure using this approach. Table 2 summarizes the results. EPC2203 was tested at both 5 V (recommended gate drive) and 6 V ($V_{GS(max)}$), with mean withstand time of 20 µs and 13 µs respectively. Note that the part survives less time at 6 V because of the higher saturation current. EPC2051 exhibited a slightly lower time-to-fail (9.3 µs) compared with the EPC2203 at 6 V. This is expected because of the more aggressive scaling and current density of 5th generation products. However, in all cases, the withstand time is comfortably long enough for most short-circuit protection circuits to respond and prevent device failure. Furthermore, the withstand time showed small part-to-part variability.

The lower rows in Table 2 provide pulse power and energy relative to die size. To gain insight into the relationship between these quantities and the time to failure, time-dependent heat transfer was simulated to determine the rise in junction temperature ΔT_J during the short-circuit pulse. The results are shown in Figure 13. The intense power density during the pulse leads to rapid heating

Short-circuit pulse V_{DS} = 60 V	EPC2203 (Gen 4)		EPC2051 (Gen 5)	
	V_{GS} = 6 V	V_{GS} = 5 V	V_{GS} = 6 V	V_{GS} = 5 V
Mean TTF (µs)	13.1	20.0	9.33	21.87
Std. dev. (µs)	0.78	0.37	0.21	2.95
Min. TTF (µs)	12.1	19.6	9.08	18.53
Avg pulse power (kW)	3.211	2.554	5.516	3.699
Energy (mJ)	43.36	50.24	50.43	77.34
Die area (mm²)	0.9025		1.105	
Avg power/area (kW/mm²)	3.558	2.830	4.99	3.35
Energy/area (mJ/mm²)	48.05	55.67	45.64	69.99

Table 2: Short-circuit withstand time statistics for EPC2203 and EPC2051. Statistics derived from eight parts in each condition. Withstand times are tightly distributed around mean value. Average pulse power and energy correspond to a typical part within the population.

in the GaN layer and nearby silicon substrate. Because the pulse is short and heat transfer is relatively slow, only a small thickness of semiconductor (<~100 µm in depth) can help to absorb the energy. The temperature grows as the square root of time (characteristic of heat diffusion), and linearly with the pulse power. As can be seen in Figure 13, for EPC2203, both the 5 V and 6 V conditions fail at the same junction temperature rise of ~850°C. The same is true for EPC2051, where both conditions fail at the same ΔT_J of ~1050°C. Three important conclusions stem from these results:

1. For a given device, the time to failure is inversely proportional to the power dissipation squared (P-2). This applies for short-circuit and SOA pulses of duration < ~1 ms.
2. The intrinsic failure mode resulting from high power pulses is directly linked to the junction temperature exceeding a certain critical value.
3. Wide bandgap eGaN devices can survive junction temperatures (> 800 °C) that are totally inaccessible to silicon devices owing to free-carrier thermal runaway.

Further analysis is required to determine the exact mechanism of failure. Nonetheless, the experimental results presented in this study demonstrate the outstanding short-circuit capability of eGaN FETs, allowing users to design their systems and short-circuit protection schemes with ample safety margins.

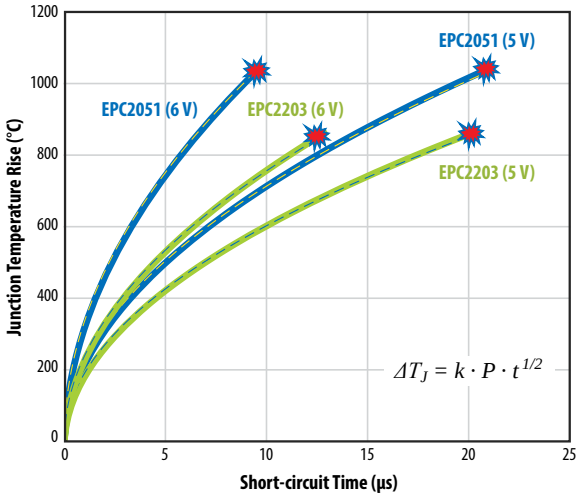


Figure 13: Simulated junction temperature rise vs time during the short-circuit pulses for both EPC2051 and EPC2203 at both 5 V and 6 V V_{GS}. Measured failure times are indicated by red markers. Note that EPC2203 fails catastrophically at a ΔT_J of around 850°C, whereas EPC2051 fails around 1050°C. The simulated ΔT_J is well fit by a simple square root dependence on time (heat diffusion), as shown in the equation. P denotes the average power per unit area, and k = 6.73 x 10^{-5} K/W $s^{1/2}$.

SECTION 5: SHORT CURRENT PULSE RELIABILITY (LIDAR APPLICATION)

eGaN FETs are widely adopted in lidar circuits for autonomous vehicles, where they offer several key benefits:

- Faster switching for shorter pulses and better range resolution
- Smaller footprint which enables high power density, low inductance and compact solutions
- Higher efficiency at higher pulse repetition rate

In a lidar application, the GaN device experiences short high current pulses, on the order of 1–5 ns, which drive a laser diode to generate narrow optical pulses. The peak currents are usually substantially greater than 50% of the FET pulse current rating. The pulse duty cycle is typically low, and the pulse repetition frequency is in the range of 10 to 100 kHz. When not being pulsed, the part is in the OFF state, exposed to a certain drain bias.

This stress condition is somewhat unusual for a power device, making it difficult to predict lifetime in operation by projecting conventional DC reliability tests such as HTGB or HTRB. Even GaN-specific tests, like the hard-switching reliability testing discussed in Section 2, do not effectively emulate the stress conditions in a lidar circuit. From the standpoint of physics of failure, the simultaneous high current and voltage during a pulse raises concerns about hot-carrier effects, potentially leading to V_{TH} or $R_{DS(on)}$ shifting within the device. In addition, the cumulative effect of repetitive high current pulses raises the specter of electro-migration leading to degradation of the solder joints.

To address these concerns in this developing market, EPC initiated a novel test method in collaboration with key lidar customers. This lidar reliability testing is part of EPC's Beyond AEC Initiative, a series of GaN specific stress tests that go beyond the conventional reliability tests developed for MOSFETs as part of AEC-Q101 standard.

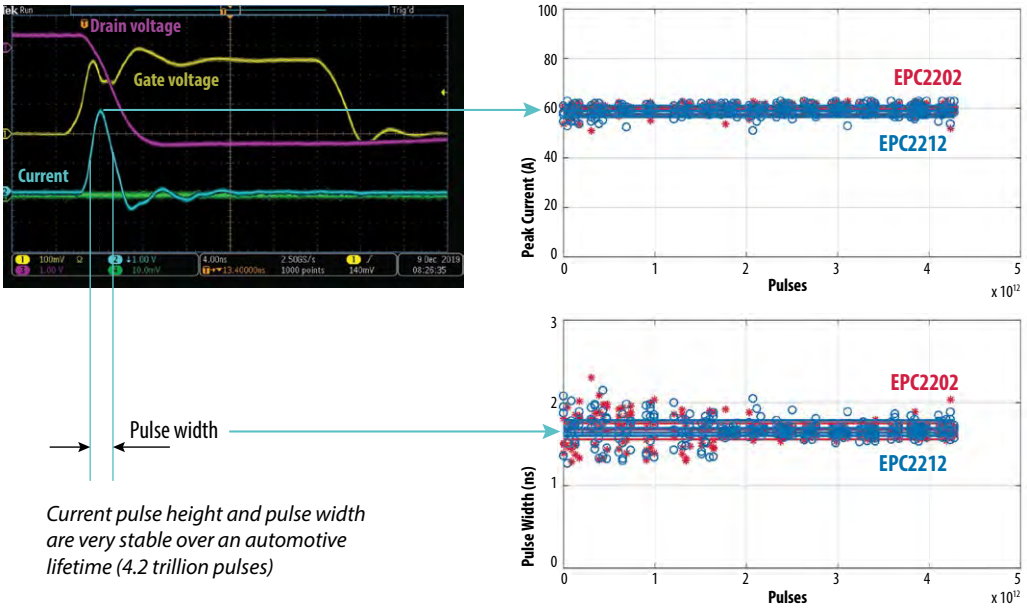
The concept is to stress parts in an actual lidar circuit for a total number of pulses commensurate with their ultimate mission profile. The mission profiles for automotive lidar vary from customer to customer. A typical automotive profile would call for a 15-year life, with two hours operation per day, at 100 kHz pulse repetition frequency (PRF). This corresponds to approximately four trillion total lidar pulses. Some worst-case scenarios might call for 10–12 trillion pulses in service life. By testing a population of devices to the end of their full mission profile, this test method directly demonstrates the lifetime of eGaN devices in a lidar mission. Note that this direct approach obviates the need for an acceleration factor or activation energy of dubious validity. It also removes the need to somehow project lifetime estimates from standard reliability tests to the unique stress conditions of lidar.

To achieve the large number of pulses, parts are stressed continuously at a PRF much higher than in typical Lidar circuits. The test circuit is based on EPC's popular EPC9126 lidar application board [18]. Experimental details are provided in Appendix B. For this study, two popular AEC grade parts were put under test: EPC2202 (80 V) and EPC2212 (100 V). Four parts of each type were tested simultaneously. During the stress, two key parameters are continuously monitored on every device: (i) peak pulse current and (ii) pulse width. These parameters are both critical to the range and resolution of the lidar system.

Figure 14 shows the results over the first 4.2 trillion pulses. Note that there is no observed degradation or drift in either the pulse width or height. The cumulative number of pulses corresponds to a typical automotive lifetime. While this is an indirect monitor of the health of the eGaN device, it indicates that no degradation mechanisms have occurred that would adversely impact circuit performance.

To gain better visibility into the eGaN device parametric stability over time, the test system interrupts lidar stress every six hours to measure the device threshold V_{TH} and $R_{DS(on)}$. After this brief parametric measurement, the parts are returned quickly to lidar stress mode. The results are shown in Figure 15. Both of these parameters show excellent stability over the duration of the test. The stability indicates that lidar stress is relatively benign to eGaN devices.

Short current pulse (lidar) testing of eGaN devices shows they are very reliable in this application over a typical automotive lifetime. As of the publishing of this report, no failure modes or parametric degradation have been observed. Moving forward, EPC plans to continue testing this cohort to failure to identify any possible wear out mechanisms. In addition, a larger population of parts will be put on test to improve statistical confidence in these results.



Current pulse height and pulse width are very stable over an automotive lifetime (4.2 trillion pulses)

Figure 14: Long-term stability of pulse with (bottom right) and pulse height (top right) over 4.2 trillion lidar pulses. Data for 4 EPC2202 (red) devices and 4 EPC2212 (blue) devices are overlaid in the plots. Note the excellent stability of these key parameters over total number of pulses corresponding to a typical automotive lifetime.

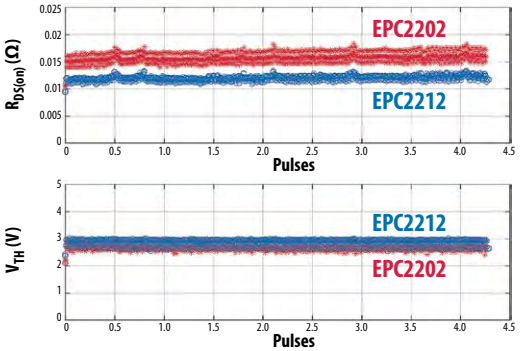


Figure 15: Long-term stability of $R_{DS(on)}$ and V_{TH} during lidar reliability testing. These parameters are measured at six-hour intervals on every part by briefly interrupting the lidar stress. Note that V_{TH} is inferred by measuring $R_{DS(on)}$ at a series of gate voltages. Data for four EPC2202 (red) devices and four EPC2212 (blue) devices are overlaid in the plots. Note the excellent stability of these key parameters over total number of pulses corresponding to a typical automotive lifetime.

SECTION 6: MECHANICAL STRESS

6.1 Die shear test

The purpose of die shear test is to evaluate the integrity of the solder joints used to attach eGaN devices to PCBs. This determination is based on the in-plane force at which, when applied to a mounted device, the die shears off from the PCB. All testing followed the military test standard, MIL-STD-883E, Method 2019 [19].

Figure 16 shows the test results of four selected EPC eGaN FETs. Ten parts were tested for each product. The smallest die tested is EPC2036/EPC2203 [20-21], which only has four solder balls with a diameter of 200 µm and a die area of 12.6 x 10^{-4} in^2. As expected, this product turned out to have the least shear strength, however, it exceeds the minimum force requirement specified by the MIL standard, as shown in Figure 16. The largest die tested was EPC2206 [22], a land grid array (LGA) product with die area of 216 x 10^{-4} in^2. EPC2206 exceeds the minimum force requirement more than a factor of ten. Within the size spectrum, two additional products were tested: EPC2212 (100 V LGA) [14] and EPC2034C [23] (200 V BGA). Both products surpassed the minimum force significantly.

In Figure 16, the results show that all wafer-level-packaged EPC products are mechanically robust against environmental shear stress under the most stringent conditions.

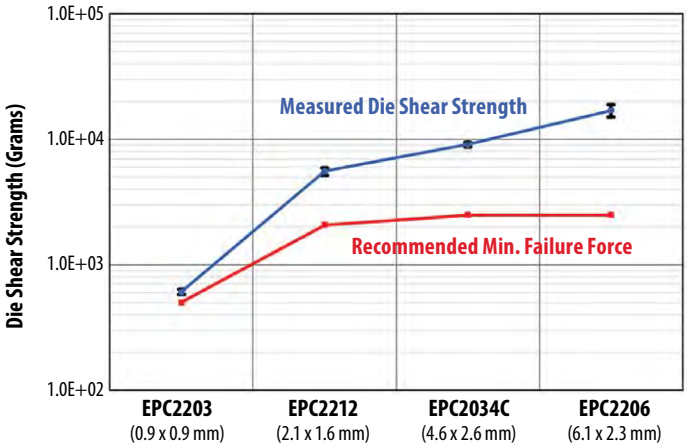


Figure 16: Various die sizes and solder configurations of eGaN FETs were tested to failure while measuring the shear strength. The results are shown with black dots. The red stars show the minimum recommended die shear strength under MIL-STD-883E, Method 2019.

6.2 Backside pressure test

Another critical aspect of the mechanical robustness of eGaN devices is how well they handle backside pressure. This is an important consideration for applications that require backside heatsinking to the die. It is also important to determine the safe pick-and-place place force during assembly.

EPC performed backside pressure tests up to 400 psi, where the pressure is calculated by the force applied divided by the die area. Figure 17 shows the laboratory pressure tester that was employed. The pressure was applied directly to the backside of the die using a loading speed of 0.6 mm/min. Before and after the pressure test, parametric testing was performed to determine pass or fail. Subsequently, the parts were exposed to humidity-bias testing (H3TRB) at 60 V_{DS}, 85°C, and 85% relative humidity for 300 hours. H3TRB is effective to determine if there were any latent failures caused by mechanical damage (internal cracking) from the pressure test.

Figure 17: Pressure test instrument. The tester head lowers to the backside of the devices using a constant loading speed of 0.6 mm/min until the predetermined force is sensed by the gauge. The DUTs are surface mounted on a FR4 test coupon that is secured on the testing stage.

EPC2212 (100 V, LGA) and EPC2034C (200 V, BGA) were tested and both passed 400 psi. The data is included in Table 3. These results show that eGaN FETs have enough margin to handle backside pressure that is normally used at a PCB assembly house. Though these parts survived 400 psi, EPC recommends limiting maximum backside pressure to 50 psi or less.

Product	Sample Size	Die Area	Backside Pressure	Force Applied	Failures in Parametric Test after Pessure Test	Failures after 300 hours H3TRB test
EPC2212 (LGA)	16	2.1 x 1.6 mm	400 psi	9.3 N (2.1 lbs)	0/16	0/16
EPC2034C (BGA)	16	4.6 x 2.6 mm	400 psi	33.0 N (7.4 lbs)	0/16	0/16

Table 3: Small and relatively large eGaN devices were tested under high backside pressure with no mechanical failures, and no failures after stress testing under temperature, humidity, and bias.

SECTION 7: FIELD RELIABILITY UPDATE

All the reliability testing and test-to-fail projects are intended to create a continuously improving family of products based on GaN-on-Si technology that are robust under a wide variety of actual field operating experience. Figure 18 shows the field experience over a period of more than three years and 123 billion hours of operation – most of which are on vehicles or used in telecommunication base stations. Over that extended time only three parts failed. These three parts failed due to a manufacturing defect (extrinsic defect) that has since been eliminated. This result is unmatched by silicon power devices.

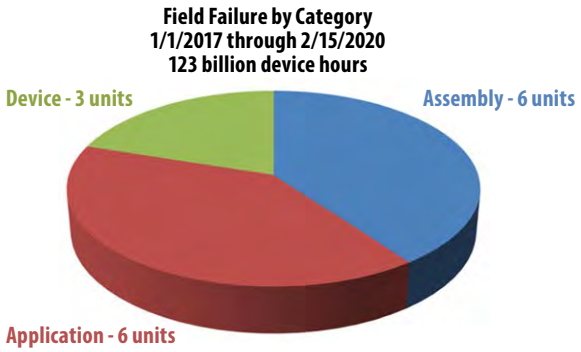


Figure 18: Field experience over a period of more than three years and 123 billion hours of operation shows that only three parts failed. These three parts failed due to a manufacturing defect (extrinsic defect) that has since been eliminated.

CONCLUSIONS

eGaN® devices have been in volume production for over 10 years and have demonstrated very high reliability in both laboratory testing and customer applications, such as lidar for autonomous cars, 4G base stations, vehicle headlamps, and satellites to name just a few. EPC continues to pursue aggressive test-to-fail testing to isolate intrinsic failure mechanisms and their behavior over all stress conditions. This information is being used to build more robust, higher performance, and lower cost products for power conversion applications.

APPENDIX A: LIDAR RELIABILITY TEST SYSTEM

Figure A.1 shows a picture of the lidar reliability test system. Devices are assembled onto a specialized lidar daughterboard. These boards are loaded into a motherboard which can stress up to eight parts simultaneously. Pulse height and width are recorded in the oscilloscope by means of relay switching each individual part in a round robin manner. Data is logged using a PC.

As shown in Figure A.2, the test circuit on the daughterboard operates in two distinct modes: (i) lidar mode and (ii) parametric mode.

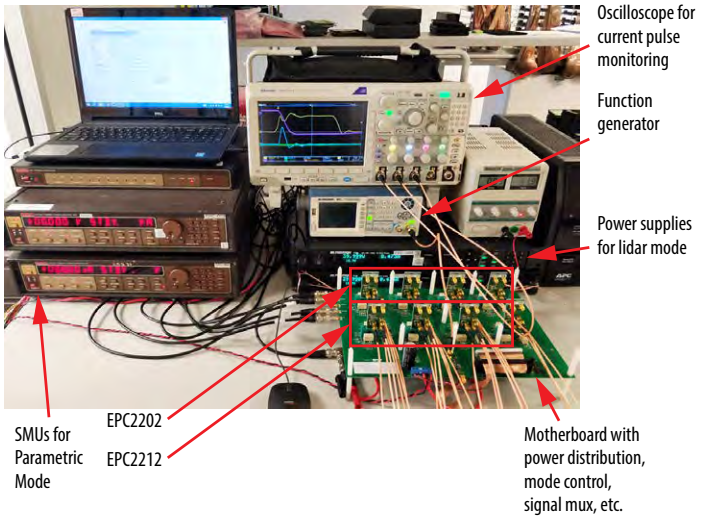


Fig A.1: Lidar reliability test system

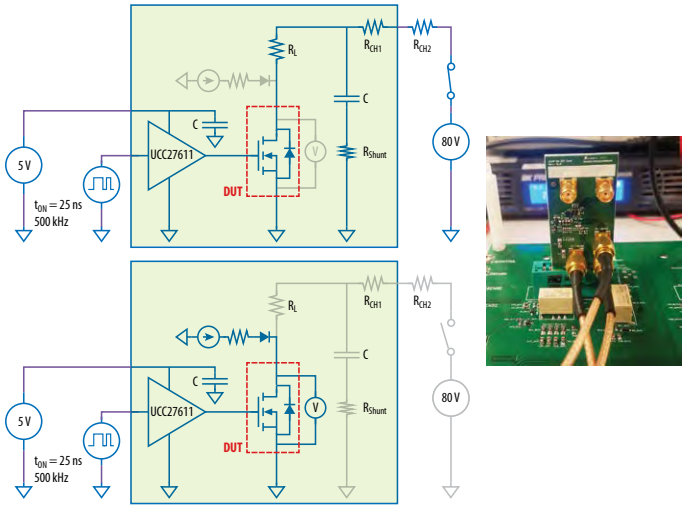


Figure A.2: Lidar test circuit: (Top-left) Lidar mode (Bottom-left) Parametric mode. Daughterboard picture (Right).

The lidar-mode circuit is based on EPC's EPC9126 lidar application board. The gate is pulsed for about 25 ns, discharging capacitor C through RL, which emulates the impedance of a laser diode in an actual lidar circuit. After the gate pulse, the part is switched off and capacitor C is re-charged to the bus voltage, holding there until the next gate pulse. The operating conditions were as follows:

- Bus voltage: 80 V (drain voltage when part is not pulsed)
- Current pulse height: > 50 A peak
- Pulse width: ~2 ns
- Pulse repetition rate: 500 kHz

Note that these conditions were set to achieve maximum stress on the eGaN FET. Typical commercial lidar circuits operate at lower PRF and typically with lower bus voltage or current pulse height.

Figure A.3 shows typical switching waveforms. The combined high current and high voltage set the stage for hot carrier dynamics, which can lead to V_{TH} shift or dynamic $R_{DS(on)}$. However, the switching locus in lidar is milder than in a typical hard-switching convertor owing to the inductance of the laser diode which throttles the current rise.

The lidar mode of the test system runs continuously in blocks of six-hour duration. Between blocks, the circuit is briefly switched into parametric mode as depicted in the bottom of Figure A.2. During parametric mode, the $R_{DS(on)}$ of each part is measured at a series of gate voltages from 4 V up to 6 V. This allows the system to regularly monitor the $R_{DS(on)}$ at 5 V_{GS} directly. Also, by fitting the dependence of $R_{DS(on)}$ on V_{GS}, the high current V_{TH} of the part can be extracted. Note that this definition of V_{TH} differs from the data sheet definition which measures V_{TH} at low drain current. Both V_{TH} and $R_{DS(on)}$, along with the lidar pulse width and pulse height, could provide valuable insight into possible degradation mechanisms during long term lidar stress.

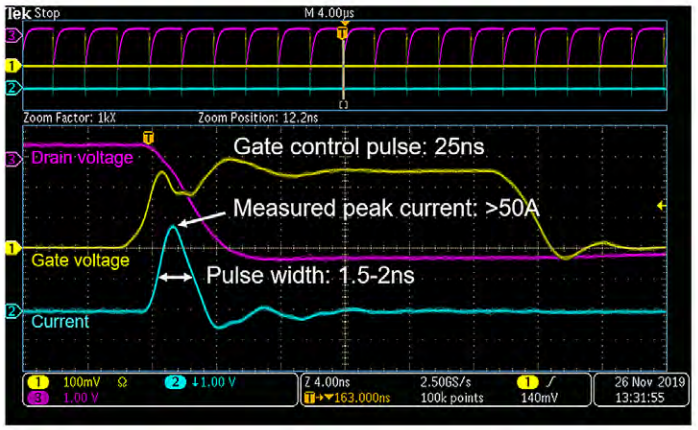


Figure A.3: Typical lidar mode pulse waveforms.

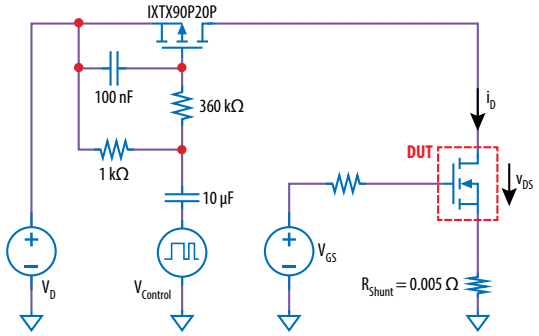
APPENDIX B: SOA TEST SYSTEM

Figure B.1 shows the circuit schematic and timing signals for the safe operating area test system. Drain (V_D) and gate (V_{GS}) biases are set at the beginning of the test and allowed time for settling. The gate voltage is set (typically in the range of 1–3 V) to achieve a desired I_D during the subsequent pulse. The drain pulse is applied to the device under test (DUT) by means of a 44 mΩ p-channel FET triggered through a capacitively-coupled gate biasing network. The bias network is tuned to provide soft transitions to prevent high di/dt and inductive over-shoot on the DUT. During the pulse, drain current (I_D) is monitored through a small current sense resistor. The drain and source voltages at the DUT are Kelvin sensed to remove the effects a parasitic resistance in the test circuit. A gate-to-source capacitor is installed close to the DUT to maintain nominal V_{GS} during the high current pulse. All signals are captured in an oscilloscope and post processed for analysis.

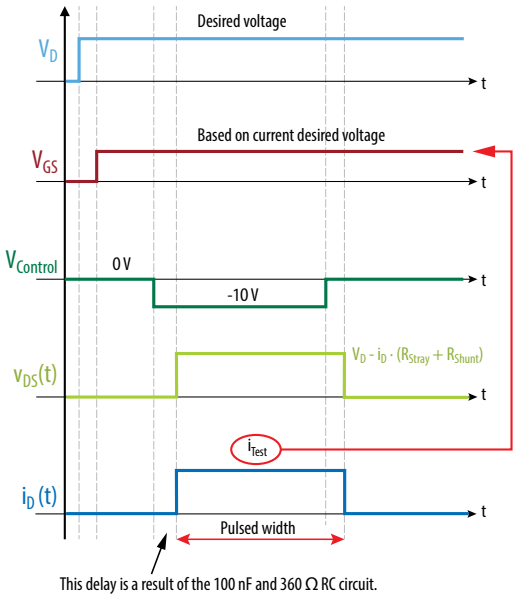
Owing to the high-gain bandwidth product of eGaN FETs, special care had to be taken to avoid oscillations in the test circuit during the pulse. In particular, common source inductance was found to be detrimental, which necessitated the use of special low inductance current sense resistors.

In addition, a small ferrite bead installed in series with the gate close to the DUT was found to reduce oscillation significantly.

Figure B.1: Safe operating area test system: (Left) Schematic of the SOA test circuit (Right) Waveforms showing bias settings and pulse timing.



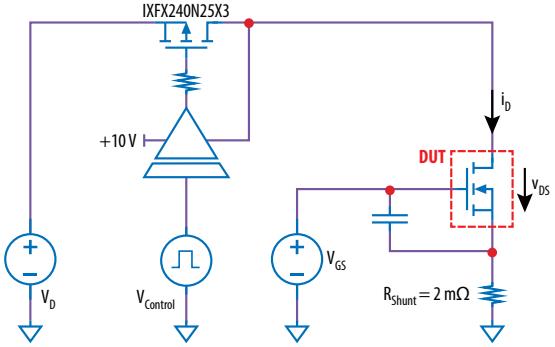
V_D: Drain bias (DC voltage)
V_{GS}: Gate bias (DC voltage)
$V_{Control}$: P-channel FET control (Pulsed)



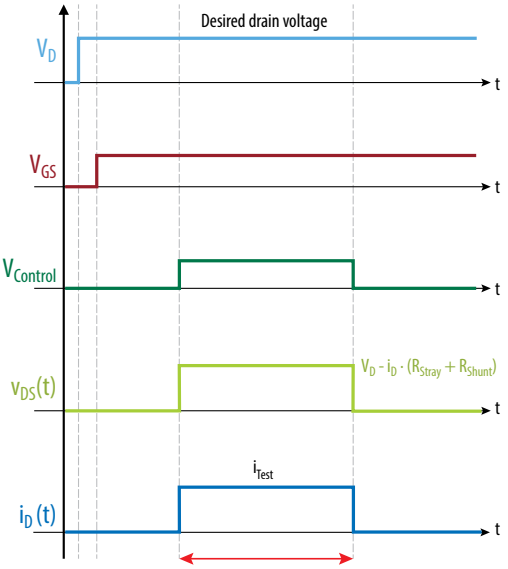
APPENDIX C: SHORT CIRCUIT TEST SYSTEM

Figure C.1 shows the circuit schematic and timing signals for the short-circuit (fault under load) test system. Drain (V_D) and gate (V_{GS}) biases are set at the beginning of the test and allowed time for settling. The drain pulse is applied to the DUT by means of a 4 mΩ n-channel FET triggered by an isolated high-side gate driver. During the pulse, drain current (I_D) is monitored through a small current sense resistor. The drain and source voltages at the DUT are Kelvin sensed to remove the effects a parasitic resistance in the test circuit. A gate-to-source capacitor is installed close to the DUT to maintain nominal V_{GS} during the high current pulse. All signals are captured in an oscilloscope and post-processed for analysis.

Fig C.1: Short-circuit test system: (Left) Schematic of the fault under load test circuit (Right) Waveforms showing bias settings and pulse timing



V_D: Drain bias (DC voltage)
V_{GS}: Gate bias (DC voltage)
$V_{Control}$: N-channel FET control (Pulsed)
i_D: Current Kelvin-sensed across R_{Shunt}
v_{DS}: Drain-Source voltage Kelvin-sensed



References:

[1] Yanping Ma, "EPC GaN Transistor Application Readiness: Phase One Testing", http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_relreport_030510_finalfinal.pdf

[2] Jean-Paul Clech, "Solder Reliability Solutions: A PC-Based Design-For-Reliability Tool," EPSI Inc., 1996

[3] Yanping Ma, "EPC GaN Transistor Application Readiness: Phase Two Testing," http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Two_Rel_Report.pdf

[4] Yanping Ma, "EPC GaN Transistor Application Readiness: Phase Three Testing," http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Three_Rel_Report.pdf

[5] Yanping Ma, "EPC GaN Transistor Application Readiness: Phase Four Testing," http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Four_Rel_Report.pdf

[6] Yanping Ma, "EPC GaN Transistor Application Readiness: Phase Five Testing," http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Five_Rel_Report.pdf

[7] Robert Strittmatter, Chunhua Zhou, and Yanping Ma, "EPC eGaN FETs Reliability Testing: Phase Six Testing," http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase6.aspx

[8] Chris Jakubiec, Robert Strittmatter, and Chunhua Zhou, "EPC eGaN FETs Reliability Testing: Phase Seven," http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase7.aspx

[9] Chris Jakubiec, Rob Strittmatter, and Chunhua Zhou, "EPC eGaN FETs Reliability Testing: Phase Eight," http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase8.aspx

[10] Chris Jakubiec, Rob Strittmatter, and Chunhua Zhou, "EPC eGaN FETs Reliability Testing: Phase Nine," http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase9.aspx

[11] Alejandro Pozo, Shengke Zhang, and Rob Strittmatter, "EPC eGaN FETs Reliability Testing: Phase Ten," http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase10.aspx

[12] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, J. Glaser, *GaN Transistors for Efficient Power Conversion*, 3rd Edition, J. Wiley 2020.

[13] Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications, Third edition: May 2015, Editor: ZVEI Robustness Validation Working Group, Eds. Published by ZVEI – Zentralverband Elektrotechnik – und Elektronikindustrie e.V. Available at https://www.zvei.org/fileadmin/user_upload/Presse_und_Medien/Publikationen/2015/mai/Handbook_for_Robustness_Validation_of_Semiconductor_Devices_in_Automotive_Applications__3rd_edition_/Robustness-Validation-Semiconductor-2015.pdf

[14] P. Spirito, G. Breglio, V. d'Alessandro, and N. Rinaldi, "Analytical Model For Thermal Instability Of Low Voltage Power MOS and S.O.A. In Pulse Operation," 14th International Symposium On Power Semiconductor Devices &ICS; Santa Fe, NM; 4–7 June 2002; pp. 269–272

[15] Efficient Power Conversion Corporation, "EPC2212 – Automotive 100 V (D-S) Enhancement Mode Power Transistor," EPC2212 data sheet. 2019 [Revised August 2019]. Available from: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/epc2212_datasheet.pdf

[16] Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices, Version 1.0, JEDEC Standard JEP173, 2019.

[17] Efficient Power Conversion Corporation, "EPC2045 – Enhancement Mode Power Transistor," EPC2045 data sheet. 2019 [Revised August 2019]. Available from: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/epc2045_datasheet.pdf

[18] S. Mishra, "Fault current limiting and protection circuit for power electronics used in a Modular Converter." Master's Thesis, University of Tennessee, 2008. https://trace.tennessee.edu/utk_gradthes/468

[19] "Development Board EPC9126/EPC9126HC Quick Start Guide EPC2212/EPC2001C 100 V High Current Pulsed Laser Diode Driver," https://epc-co.com/epc/Portals/0/epc/documents/guides/EPC9126xx_qsg.pdf

[20] MIL-STD-883E (Method 2019), "DEPARTMENT OF DEFENSE TEST METHOD STANDARD: MECHANICAL TESTS- DIE SHEAR STRENGTH," May 3, 2018, https://landandmaritimeapps.dla.mil/Downloads/MilSpec/Docs/MIL-STD-883/std883.pdf

[21] EPC, "EPC2036 eGaN FET Datasheet," https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2036_datasheet.pdf

[22] EPC, "EPC2203 eGaN FET Datasheet," https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2203_datasheet.pdf

[23] EPC, "EPC2206 eGaN FET Datasheet," https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2206_datasheet.pdf

[24] EPC, "EPC2034C eGaN FET Datasheet," https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2034C_datasheet.pdf