EPC eGaN® FETs Reliability Testing: Phase 8

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Including this document, Efficient Power Conversion (EPC) Corporation has published a series of eight reliability reports covering all released products. Product specific detailed stress test results have been compiled and reported millions of actual device hours. In addition to product qualification stress testing, due diligence is necessary in other areas of reliability such as field experience, failures over device operational lifetime, and board level reliability. The first section of this report will summarize field reliability experience of eGaN® devices. The second section will report on stress testing over the lifetime of the product, and the last section will cover board level reliability. The appendix contains cumulative product specific stress test data from previous published reliability reports, as well as data collected after the Phase 7 report was released.

PART I: FIELD RELIABILITY EXPERIENCE

A summary of eGaN® FET and IC field application reliability was presented in the Phase 7 report. Excellent field reliability was demonstrated with the accumulation of over 17 billion device operation hours combined with a very low failure rate below 1 FIT (failures per billion hours). In this report we provide additional details as to why eGaN® devices are performing with excellent reliability in end user applications, as well as examine areas of improvement along the learning curve of using a maturing, yet disruptive technology.

eGaN® Technology Reliability Advantage

Several decades of industry experience manufacturing power FETs and ICs in silicon, has resulted in very high yielding and reliable devices at the wafer and die level. However, encapsulating the die with a package in order to protect the device from the environment introduces several additional mechanical and thermal interfaces, thus increasing the number of potential failure modes in the field. EPC has eliminated the need for a conventional plastic package by developing chip-scale devices that are environmentally sealed while in wafer form. The advantages of chip-scale power devices include: reduced thermal resistance, smaller form factor, elimination of package inductance and resistance, lower cost to manufacture, and ultimately higher reliability.

For packaged devices a significant percentage of power FET and IC field failures are due to thermo-mechanical stress either during the manufacturing process or during actual operation in the field. Wire bonds, die attach, mold compound, lead frames, and substrates all introduce potential failure modes. EPC chip-scale devices eliminate these variables that have plagued traditional packaged devices in the field. In addition, EPC devices are covered with glass passivation layers which protect against moisture ingression and have the benefit of unlimited shelf life with a Moisture Sensitivity Level 1 (MSL1) rating. Considering the simplicity of eGaN® chip-scale packages as compared to traditional power packages, the excellent field reliability experience to date is not surprising.

Field Failures Examined

EPC performs a thorough root cause analysis of all returned field failures. A total of 127 field failures have been investigated as of June 2016. Of the 127 field failures, 37 devices passed electrical testing with no anomalies detected, and were therefore classified as good units. Figure 1 below shows the breakdown of all field returns grouped into root cause categories. The next three sections will go into more details describing the types of field failures that have been analyzed, as well as recommendations to prevent such issues in the field.

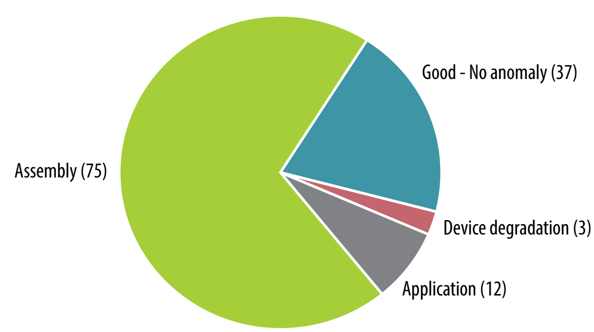


Figure 1: Field failure breakdown by root cause category.

Assembly Failures

EPC has pioneered the adoption of chip-scale packages for high power and high voltage applications whereas this form factor was previously reserved for low power and voltage applications. Applications incorporating or displacing traditional power packages with eGaN® chip-scale packages can present a learning curve for reliable board level assembly. The chip-scale fine pitch solder geometry (400 µm – 1000 µm), relatively low standoff height (~ 100 µm), and exposed die require proper assembly techniques. Device assembly and handling accounted for the highest number of field returns, with 75 units recorded in this category.

Improper control of the amount of solder paste and flux released during assembly, together with inadequate rinsing and curing of the flux, made up 36 of the field failure units in this category. Flux that has not been properly rinsed and dried can accumulate in the areas between the solder balls, and has the potential to catalyze the formation of dendrites which can create conductive leakage paths and lead to device failures. To avoid this common problem, it is advised to rinse all residual flux underneath the die, and perform a high temperature dry curing step before applying any power to the device. Figure 2 shows dendrites connecting two terminals within uncured flux.

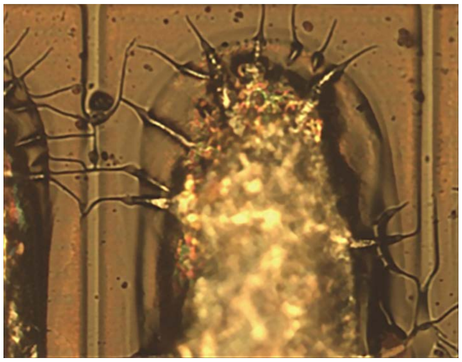


Figure 2: eGaN® FET showing dendrite formation due to residual flux.

Die tilt issues can arise due to poor stencil design resulting in uneven solder paste volume release over the PCB pads. Vibration during assembly, reflow profile, and PCB solder mask design are other factors that can contribute to tilted die.

Figure 3 below shows an example of a poor assembly versus a properly mounted eGaN® device as shown in figure 4. EPC provides solder stencil, PCB land pattern, and solder standoff height recommendations for each device in the respective datasheets. Optimizing solder standoff height can help to provide additional space for rinsing of residual flux, and also can reduce thermo-mechanical stresses by adding compliance to the solder joints, thus improving overall temperature cycling performance.

Figure 3: Tilted die trapping residual solder flux.

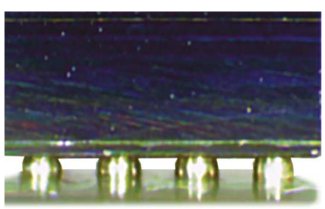


Figure 4: Properly mounted device.

Die corner chipping was found to be the cause of failure for 27 units in the field. A consequence of eliminating molded plastic surrounding the die, chip-scale devices have the die exposed to the environment. As a first step to insure that each device is mechanically acceptable upon receipt by the customer, EPC has automated optical inspection tools in production to screen out any mechanical damage prior to tape and reel and shipment. Device assembly by the customer using automated tools such as pick and place must be programmed and aligned to avoid mechanical damage such as corner chipping or die cracks. In the 27 failures due to chipping, it was found that the PCB placement tool inserting components around the eGaN® device did not have adequate clearance to avoid hitting and damaging the die. Figure 5 below shows an example optical microscope image of a field failure due to die chipping.

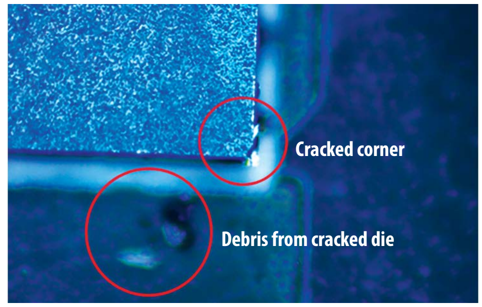
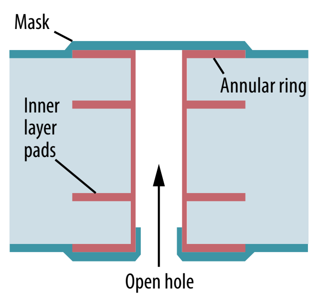


Figure 5: eGaN® Field failure showing die corner chipping caused by inadequate clearance of pick and place tool while placing components adjacent to the eGaN® FET.

Twelve failures were found to be related to inadequate amount of solder paste on the PCB pads during device assembly. The root cause was determined to be vias near solder pads that had not been "tented" during the PCB manufacturing. Tenting uses a layer of solder mask to cover the via opening and prevent a path along which solder could flow. An uncovered via adjacent to a pad can pull the solder paste down inside the via during high temperature reflow, leaving a lower volume of solder paste on the solder pad available to make contact with the device solder balls. Figure 6 shows a diagram of a tented via, and an example optical image of a PCB where the vias have been left uncovered.



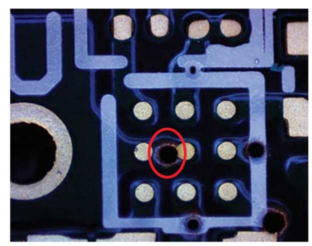


Figure 6: (a) Diagram of via with solder mask tent covering. (b) PCB showing uncovered via.

Solder paste type, solder stencil, solder flux, board cleanliness, via design, solder mask, and solder joint standoff height are key parameters that must be understood to ensure assembly and board level reliability of eGaN® devices. EPC has published assembly guides and videos on their website to help customers with proper assembly and rework: Assembly Resources

Application Failures

eGaN® devices have much faster switching speeds and lower parasitic capacitances as compared with silicon power devices. End user applications need to be designed accordingly to accommodate faster edge rates and inadvertent voltage transients.

For a total of 12 field failures, the root cause was related to a circuit design issue. Eleven of the field failures were damaged due to the electrical overstress resulting from voltage overshoot in a circuit layout that had too much parasitic inductance. Transient overvoltage can lead to device degradation observed as increased leakage currents or on state resistance, as opposed to DC overstress conditions which typically show up as completely inoperable devices.

The very low capacitance and extremely fast switching edge rates of eGaN® devices requires careful layout of PCBs to minimize common source inductance (CSI), the inductance in the gate-to-source loop, and power loop inductance (See figure 7). Figure 8 demonstrates the impact on switching waveform overshoot in a high frequency application, by reducing loop inductance of the PCB layout from 1.6 nH to 0.4 nH. The peak transient voltage due to the high frequency power loop inductance is reduced from 100% to 30% of the steady state value respectively.

Similarly, increased common source inductance and non-optimal resistance in the gate drive circuit can result in voltage overshoots and ringing that can cause device failures. Optimization of the gate drive resistance and reduction of the gate loop inductance results in significantly less voltage overshoot as seen in figure 9 below.

For guidelines on optimizing PCB layout using eGaN® FETs refer to the following EPC publication: **Optimizing PCB Layout**

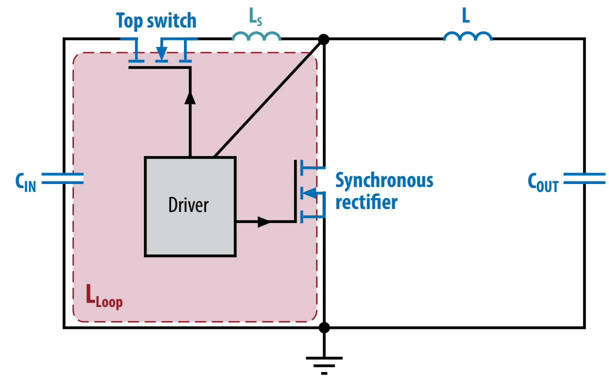
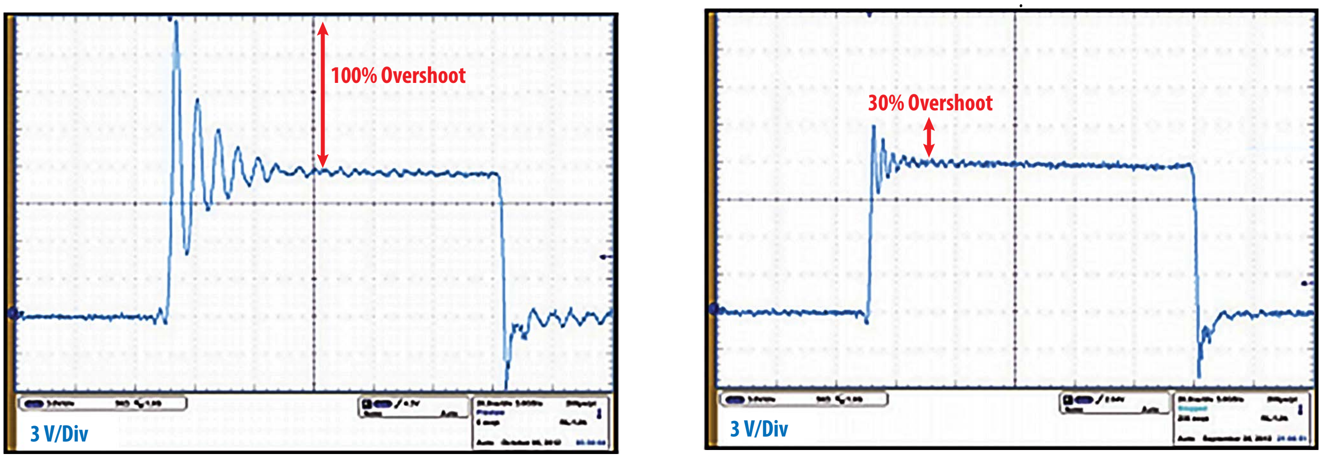
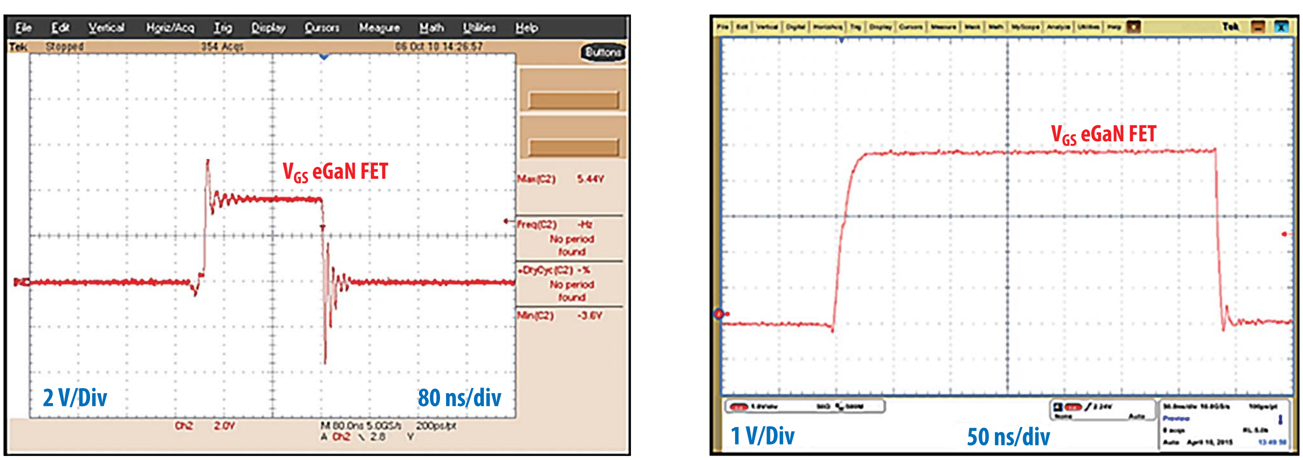


Figure 7: Synchronous rectifier showing parasitic inductances (L_S is common source inductance) (L_{Loop} is high frequency power loop inductance) (LLoop is high frequency power loop inductance)



(a) (b)

Figure 8: (a) High frequency switching waveform of eGaN® FET design with power loop inductance L_{Loop} = 1.6 nH
(b) High frequency switching waveform of eGaN® FET design with power loop inductance L_{Loop} = 0.4 nH
EPC eGaN® FET EPC2015 Synchronous Rectifier Circuit (V_{IN} = 12 V, V_{OUT} = 1.2 V, F = 1 MHz)



(a) (b)

Figure 9: (a) Non-optimized gate drive circuit
(b) Optimized gate drive circuit
EPC eGaN® FET EPC2010 Synchronous Rectifier Circuit

Intrinsic Device Failures

Intrinsic device failures account for only 3 units, however it is equally important that root cause is determined. Based on these 3 field failure units together with over 17 billion device hours, the calculated FIT rate is approximately 0.24 FITS (60% confidence interval).

Dynamic $R_{DS(on)}$ is a mechanism that can adversely affect previous generation GaN devices, as a result of carrier trapping in the basic material layers. The on state resistance of a GaN FET can shift when subjected to high drain voltage over long periods of time due to the activation of these traps that can sequester electrons that would otherwise be used for conduction. This phenomenon must be understood both by the FET manufacturer and the end user to design in sufficient guard band to accommodate. EPC has ongoing efforts to improve the material properties that reduce carrier trap concentrations, and thus limit the dynamic $R_{DS(on)}$ to a negligible effect. See published Phase 6 and 7 reliability reports on the EPC website for further analysis: **eGaN® FET Reliability**

Overall field reliability experience of eGaN® devices has been demonstrated to be as good as, or better than any comparable traditional power devices in the market. EPC engineers continue to work with customers to close the knowledge gap in the remaining few areas where field issues arise from using state of the art technology such as power chip-scale GaN.

PART II: EARLY LIFE FAILURE & WEAR-OUT CAPABILITY

It is important that device stochastic failure rates are well understood throughout the entire product life cycle including early life, normal life, and end of life wear-out. Early life and end of life typically have higher failure rates, as opposed to normal life operation with relatively low constant failure rates. Infant mortality is examined by Early Life Failure Testing (ELFR), while electromigration (EM) is a wear-out type failure mechanism that generally manifests much later in the operational lifetime.

Early Life Failure Rate

Early life failure rate testing and objectives were first presented in the Phase 7 reliability report. The premise for evaluating ELFR is to test large sample populations under relatively short durations (typically 48 hrs). This report continues to build upon these results, and includes a larger set of statistical data to evaluate and gain confidence in eGaN® device reliability. Both gate and drain-source structures have been stressed under ELFR conditions. As the number of units tested increases, the estimated failure rates resulting from ELFR testing become more accurately predictable. As of this report a total of 13,199 units have been ELFR tested, with no failures. The high volume EPC2016C 100 V device was selected as the test vehicle. Table 1 summarizes the ELFR test conditions and results.

Electromigration

Electromigration (EM) is the displacement of atoms in a conductor due to the momentum of electron charge (i.e. current) flowing. Device metal lines and connecting vias are susceptible to EM as they carry current over long periods of device operation, and the current density can become high. Figure 10 illustrates an example effect of electromigration on a metal conductor line (note: example is not an EPC product). As a result, the metal line will form voids or an accumulation of atoms (extrusion or hillock), each of which can lead to different failure modes. Voids in the metal line will lead to increased resistance, which is the main parameter monitored during EM testing. The composition of the conductor (e.g. copper, aluminum, tungsten, etc.) and geometry influence the EM capability. For example, grain boundary formation in aluminum tends to be a weak point for EM and can be improved by adding copper.

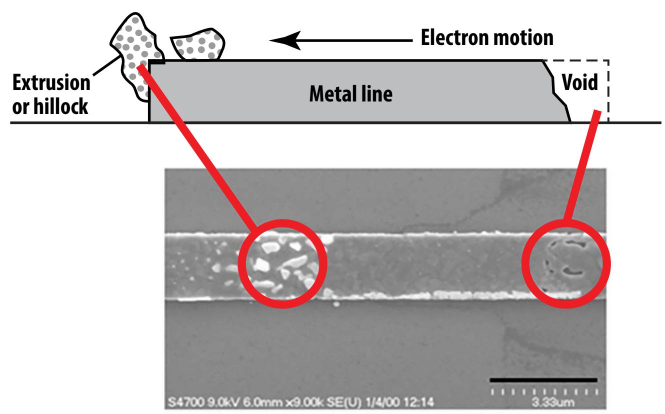


Figure 10: Effects of electromigration on a metal conductor via scanning electron microscope: voids and atom accumulation observed [from 18].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	ELFR (upper bound 60% confidence)
HTRB_ELFR	**EPC2016C**	100	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	1610 x 1 1621 x 1 1614 x 1 1121 x 1 800 x 3	48	110 ppm
HTGB_ELFR	**EPC2016C**	100	M (2.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	1615 x 1 1578 x 1 1640 x 1	48	190 ppm

Table 1. ELFR Results (HTGB & HTRB)

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
EM	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, I = 20 A	0	30 x 1	1000

Table 2. Electromigration test results EPC2016C

Electromigration testing is often performed by using a specific set of test structures such as isolated metal lines or vias. EPC has done the EM testing at a system board level, with the die solder mounted to a device under test (DUT) card printed circuit board. Figure 11 shows an example DUT card with an eGaN® chip-scale FET mounted in the center. EM test die were created to provide dedicated conductive paths thru the solder bumps, metal layers, and vias.

The devices tested were EPC2016C, which have a continuous current rating of 18 amps (T_A = 25°C, θ_{JA} = 13.4). All devices were stressed at 20 amps, 150°C, for 1000 hours. The resistance was monitored over the duration of the test and remained stable, indicating the devices were capable to withstand the applied EM stress conditions. Table 2 summarizes the test conditions and results.

Figure 11: EPC2016C DUT card.

EPC is continuing to study both infant mortality and end of life wear-out capability of eGaN® devices. This report showed early life failure rate and electromigration stress testing capability for the EPC2016C, with very good results. Future reliability reports will demonstrate ongoing testing of eGaN® device capability over a wider range of devices and stress conditions, while also investigating the limits of what stresses the devices can withstand.

PART III: BOARD LEVEL RELIABILITY & THERMO-MECHANICAL CAPABILITY

Thermo-mechanical testing of EPC chip-scale packages is also performed with the die solder mounted to individual PCB DUT cards. The common industry practice of FET and IC suppliers is to perform stress testing in two separate runs, one at the component level and the other at the board level with the devices solder mounted. Stress tests are then selected to target either component or board level reliability. EPC test conditions have the advantage where all stress tests are performed with devices solder mounted to PCB's, so that component and board level reliability are simultaneously evaluated for each test. Tests such as pre-conditioning to evaluate moisture and solder reflow temperature capability are inherently included in all stress tests of EPC devices. EPC board level reliability logs many hours of elevated temperature and humidity data from tests such as HTGB, HTRB, HTS, and H3TRB. Additional stress tests targeted for board level reliability are Temperature Cycling (TC) and Intermittent Operating Life (IOL).

Intermittent Operating Life

Intermittent Operating Life (IOL) capability for several products was presented in the Phase 7 reliability report, as well as new data included in the appendix of this report. IOL is a cyclic temperature stress test where the devices are heated by applying power until a predefined junction temperature is reached, and power is subsequently removed to cool the device back to ambient. EPC has started experiments to investigate accelerated IOL stress conditions, and thus work toward developing predictive models for lifetime based on number of thermal cycles to failure. The approach is to create theoretical lifetime models based on calculated strain energy on the solder joints during the thermal cycles, together with testing devices to failure using several different peak profile temperatures.

The thermo-mechanical shear strain in the solder joints during cyclic temperature stress testing can be estimated by the following equation [from 19]:

$$\varepsilon = \Delta\alpha * \Delta T(DNP/t)$$

where ε is the shear strain in the solder joint, Δα is the CTE mismatch between the die and the PCB, ΔT is maximum temperature change during a cycle, DNP is the distance of the solder joint from the neutral point of the die, and *t* is the solder joint standoff height. As a result of this strain, the solder joints will experience stress, and will undergo a certain amount of plastic creep deformation depending on the strain, temperature, and cycle time. Four cyclic temperature profiles were tested with junction temperature differences during each cycle of: delta_T_j = 100°C, delta_T_j= 125°C, delta_T_j = 138°C, and delta_T_j =150°C (EPC80xx: 2.1 mm x 0.9 mm). For each temperature profile, the cyclic stress-strain energy density was calculated using the methods described in "Acceleration Factors and Thermal Cycling Test Efficiency for Lead-Free SN-AG-CU Assemblies" [20]. Figure 12 shows an example of the modeled stress-strain in a solder joint corresponding to a delta_T_j = 150°C temperature profile. The X and Y axes show the contributions of shear strain and shear stress at the solder joints as the device is transitioned thru the temperature cycle. The area inside of the loop represents the total plastic (creep) strain energy density per cycle. Compared to other metrics of solder damage, the strain energy has been shown to be the most dependable metric for predicting solder fatigue lifetime.

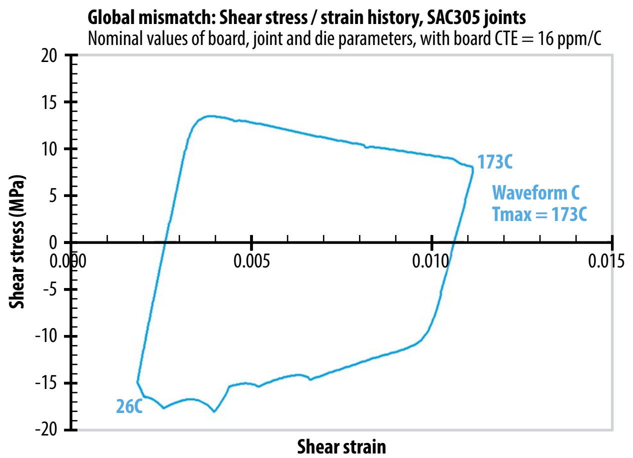


Figure 12. Calculated solder joint strain energy density during IOL cycle delta_T_j = 150°C (EPC80xx: 2.05 mm x 0.85 mm).

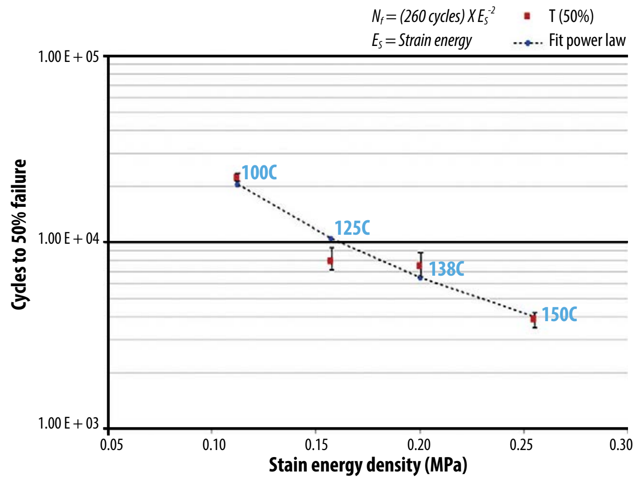


Figure 13. IOL thermal model: number of cycles to failure versus solder joint strain energy density (error bars represent 67% confidence).

The IOL test for each temperature condition was performed until 50% of the population failed, and the strain energy density was calculated for each condition. The number of IOL cycles to 50% failure versus the calculated strain energy density is plotted in figure 13. A power law curve (exponent of -2) was found to give the best fit to the data, resulting in the following general equation to predict number of cycles to fail (N_f):

$$N_f = (260 \text{ cycles}) \times E_S^{-2}$$

where E_s is the strain energy.

A preliminary model is now established for thermal-mechanical stress testing of solder joints that can be used to estimate number of thermal cycles to failure. The strain energy density for various die sizes, bump configurations, and CTE material mismatches can be similarly calculated and entered into the model to provide an estimate of number of cycles to failure. EPC is continuing to test additional products in a similar fashion to extend the data set and further validate these results.

Temperature Cycling

EPC is performing a design of experiment (DOE) using TC stress to evaluate a range of devices over various solder ball arrays and die sizes. The objective is to compare TC capability relevant to solder ball outline, die size, and, similar to what was done in IOL, a predictive model for lifetime versus number of thermal cycles can be created. The model established in the IOL testing should also be applicable for TC or any cyclic thermal stress tests. Table 3 below shows the device types and test conditions of the TC DOE matrix. Temperature cycling is performed in a thermal chamber with the device unbiased, -40°C to +125°C, and 5 minute dwell times. The next reliability report will include the results and subsequent lifetime estimates.

EPC has collected a large amount of thermal-mechanical data that shows chip-scale packages are very reliable at the board level. Customers can improve board level reliability of eGaN® devices by maximizing solder bump standoff height, minimizing CTE mismatch, and providing good conductive cooling paths from the solder bumps to the PCBs.

Stress Test	Part Number	Ball Array	Pitch (x/y) um	Die Size (mm x mm)	Test Condition	Sample Size (sample x lot)
TC	EPC2036	2 x 2	450 / 450	S (0.95 x 0.95)	-40°C to +125°C	32 x 1
TC	EPC2040	2 x 3	400 / 400	S (0.95 x 1.35)	-40°C to +125°C	32 x 1
TC	EPC2106	3 x 3	450 / 450	M (1.35 x 1.35)	-40°C to +125°C	32 x 1
TC	EPC2103	5 x 15	400 / 450	XL (6.10 x 2.35)	-40°C to +125°C	32 x 1
TC	EPC2033	5 x 5	1000 / 500	XL (2.65 x 4.65)	-40°C to +125°C	32 x 1
TC	EPC80xx	2 x 4	450 / 450	S (2.05 x 0.85)	-40°C to +125°C	32 x 1

Table 3. Temperature cycle DOE matrix

APPENDIX: PRODUCT QUALIFICATION STRESS TEST SUMMARY

EPC's eGaN® FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature
- High temperature storage (HTS): Parts are subjected to heat at the maximum rated temperature
- Temperature cycling (TC): Parts are subjected to alternating high- and low temperature extremes
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to humidity under high temperature with a drain-source voltage applied
- Unbiased autoclave (AC or Pressure Cooker Test): Parts are subjected to pressure, humidity, and temperature under condensing conditions
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Electrostatic discharge (ESD): Parts are subjected to ESD under human body (HBM), machine (MM), and charged device (CDM) models.
- Intermittent operating life (IOL): Parts are subjected to an on/off cyclic DC power pulse which heats the device junction to a predefined temperature, and subsequently to an off state junction temperature.

The stability of the devices is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN® FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) standards [1] when possible.

Parts were mounted onto FR5 (high Tg FR4) or polyimide adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 or SAC405 solder [2] no clean flux was used in mounting the part onto an adaptor card.

Summary of Statistical Stress Results

Table 4 summarizes reliability tests results and provides a composite statistical estimator of the failure rate. A combined total of over 8 million device-hours have been accumulated with zero failures. Since there are no failures, the statistic represents the worst case upper bound with 60% confidence. These upper bound values are limited only by the sample size, and will continue to drop as EPC continues to collect reliability data. For some stress tests where appropriate, both failures in time (FIT) and mean time to failure (MTTF) are calculated. These calculations assume an acceleration factor AF = 1. Therefore, operating under less stringent use conditions will yield an even lower projected rate of failure. For other stress tests, the failure rate (in ppm) is provided, along with the associated stress time period.

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (hrs)	Upper Bound Failure Statistic (60% Confidence)	Notes
HTRB	1831	0	2832000	323 FIT (MTTF = 353 yrs)	V_{DS} = 80% $V_{DS;max}$
HTGB	1848	0	3003000	305 FIT (MTTF = 374 yrs)	$V_{GS} \geq 5.5V$
TC	1040	0	1301500	NA	$\Delta T \geq 100°C$
H3TRB	552	0	552000	1660 FIT (MTTF = 69 yrs)	—
ELFR_HTRB	8366	0	401568	110 ppm	First 48 hrs
ELFR_HTGB	4833	0	231984	190 ppm	First 48 hrs
IOL	385	0	150150	NA	—
All Tests	**18855**	**0**	**8472202**		

Table 4. Summary of Composite Upper Bound Failure Statistics

High Temperature Reverse Bias

As part of the standard qualification samples were subjected to 80% of the rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [3]. The part types on stress testing covered the full voltage range of 40 – 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 x 2	3000
HTRB	EPC2010	200	L (3.55 x 1.63)	T = 150°C, V_{DS} = 160 V	0	77 x 2	3000
HTRB	EPC2012C	200	M (1.71 x 0.92)	T = 150°C, V_{DS} = 160 V	0	77 x 1	1000
HTRB	EPC2014C	40	M (1.70 x 1.09)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, V_{DS} = 80 V	0	77 x 3	2000
HTRB	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2023	30	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 24 V	0	77 x 1	1000
HTRB	EPC2024	40	XL (6.10 x 2.35)	T = 150°C, V_{DS} = 32 V	0	60 x 1	1000
HTRB	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, V_{DS} = 64 V	0	77 x 1	1000
HTRB	EPC2032	100	XL (4.65 x 2.65)	T = 150°C, V_{DS} = 80 V	0	77 x 2	1000
HTRB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{DS} = 48 V	0	77 x 1	1000
HTRB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{DS} = 80 V	0	77 x 1	1000
HTRB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 32 V	0	77 x 1	2000
HTRB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{DS} = 40 V	0	77 x 3	1000

Table 5. High Temperature Reverse Bias Test. Note: EPC800x results are applicable to all products in the EPC8000 series.

High Temperature Gate Bias

Parts were subjected to 5.75 V or 5.5 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A108 [3]. The part types on stress testing covered the full voltage range of 40 – 300 V.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2010	200	L (3.55 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	3000
HTGB	EPC2012C	200	M (1.71 x 0.92)	T = 150°C, V_{GS} = 5.75 V	0	77 x 1	1000
HTGB	EPC2014C	40	M (1.70 x 1.09)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	2000
HTGB	EPC2015C	40	L (4.11 x 1.63)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	3000
HTGB	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 3	2000
HTGB	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2023	30	XL (6.10 x 2.35)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2032	80	XL (4.65 x 2.65)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2035	60	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2036	100	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC2038	100	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	1000
HTGB	EPC8004	40	S (2.05 x 0.85)	T = 150°C, V_{GS} = 5.5 V	0	77 x 1	2000
HTGB	EPC800x	40	S (2.05 x 0.85)	T = 150°C, V_{GS} = 5.5 V	0	77 x 3	1000

Table 6. High Temperature Gate Bias Test . Note: EPC800x results are applicable to all products in the EPC8000 series.

High Temperature Storage

Parts were subjected to heat at the maximum rated temperature, in accordance with JEDEC Standard JESD22-A103 [4].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2001C	100	L (4.11 x 1.63)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2016C	100	M (2.11 x 1.63)	T = 150°C, Air	0	77 x 2	1000
HTS	EPC2021	80	XL (6.10 x 2.35)	T = 150°C, Air	0	25 x 1, 77 x 1	1000
HTS	EPC2022	100	XL (6.10 x 2.35)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC2023	30	XL (6.10 x 2.35)	T = 150°C, Air	0	25 x 1	1000
HTS	EPC2029	80	XL (4.65 x 2.65)	T = 150°C, Air	0	25 x 3	1000
HTS	EPC2032	80	XL (4.65 x 2.65)	T = 150°C, Air	0	77 x 1	1000
HTS	EPC800x	40	S (2.05 x 0.85)	T = 150°C, Air	0	77 x 3	1000

Table 7. High Temperature Storage Test
Note: EPC800x results are applicable to all products in the EPC8000 series

Temperature Cycling

Parts were subjected to temperature cycling between either (-40° C and +125° C) or (0° C and +100° C) for a total of 1000 cycles or 1500 cycles respectively, in accordance with JEDEC Standard JESD22-A104 [5].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2001C	100	L (4.11 x 1.63)	-40 to +125°C, Air	0	35 x 3	1000
TC	EPC2010C	200	M (3.55 x 1.63)	-40 to +125°C, Air	0	35 x 1	1000
TC	EPC2021	80	XL (6.10 x 2.35)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2021	80	XL (6.10 x 2.35)	-40 to +125°C, Air	0	77 x 1	500
TC	EPC2022	80	XL (6.10 x 2.35)	-40 to +125°C, Air	0	77 x 1	500
TC	EPC2023	30	XL (6.10 x 2.35)	0 to +100°C, Air	0	77 x 1	1500
TC	EPC2023	30	XL (6.10 x 2.35)	-40 to +125°C, Air	0	25 x 1	500
TC	EPC2029	80	XL (4.65 x 2.65)	-40 to +125°C, Air	0	35 x 2, 77 x 1	1000
TC	EPC2032	100	XL (4.65 x 2.65)	-40 to +125°C, Air	0	77 x 2	1000
TC	EPC800x	40	S (2.05 x 0.85)	-40 to +125°C, Air	0	77 x 3	1000
TC	EPC800x	40	S (2.05 x 0.85)	-40 to +125°C, Air	0	35 x 1	1000

Table 8. Temperature Cycling Test
Note: EPC800x results are applicable to all products in the EPC8000 series

Intermittent Operating Life

Parts were subjected to biased power cycling with junction temperature difference ≥ 100° C, in accordance with MIL-STD-750-1 [22].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
IOL	EPC800x	40	S (2.05 x 0.85)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 3	10000
IOL	EPC2001C	100	L (4.11 x 1.63)	Tj_off = +25°C, Tj_on = +125°C, delta_Tj = 100°C	0	77 x 1	6000
IOL	EPC2032	100	XL (4.65 x 2.65)	Tj_off = +40°C, Tj_on = +140°C, delta_Tj = 100°C	0	77 x 1	3000

Table 9. Intermittent Operating Life Test
Note: EPC800x results are applicable to all products in the EPC8000 series

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias at 85% RH and 85°C under 49.1 PSIA vapor pressure for a stress period of 1000 hours, in accordance with JEDEC Standard JESD22-A101 [6].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2001C	100	L (4.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 1	1000
H3TRB	EPC2010	200	L (3.55 x 1.63)	T = 85°C, RH = 85%,V_{DS} = 100 V	0	50 x 1	1000
H3TRB	EPC2012	200	M (1.71 x 0.92)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	50 x 1	1000
H3TRB	EPC2015	40	L (4.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	50 x 1	1000
H3TRB	EPC2016C	100	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 2	1000
H3TRB	EPC2022	100	XL (6.10 x 2.35)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	50 x 1, 25 x 1	1000
H3TRB	EPC2023	30	XL (6.10 x 2.35)	T = 85°C, RH = 85%, V_{DS} = 24 V	0	77 x 1	1000
H3TRB	EPC2029	80	XL (4.65 x 2.65)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	25 x 1	1000
H3TRB	EPC2032	100	XL (4.65 x 2.65)	T = 85°C, RH = 85%, V_{DS} = 80 V	0	25 x 1	1000
H3TRB	EPC2033	150	XL (4.65 x 2.65)	T = 85°C, RH = 85%, V_{DS} = 100 V	0	25 x 2	1000
H3TRB	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, V_{DS} = 40 V	0	25 x 3	1000

Table 10. High Temperature High Humidity Reverse Bias Test
Note: EPC800x results are applicable to all products in the EPC8000 series

Autoclave (Unbiased Pressure Cooker)

Parts were subjected to 100% RH at 121°C under 29.7 PSIA vapor pressure for a stress period of 96 hours, in accordance with JEDEC Standard JESD22A-102 [7]. Devices were not electrically biased during stress.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
AC	EPC2001C	100	L (4.11 x 1.63)	T = 121°C, RH = 100%	0	25 x 1	96
AC	EPC2016C	100	M (2.11 x 1.63)	T = 121°C, RH = 100%	0	25 x 2	96

Table 11. Autoclave Test

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a stress period of 168 hours. The parts were also subjected to three cycles of Lead-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020 [8].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC2001C	100	L (4.11 x 1.63)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168
MSL1	EPC2029	80	XL (4.65 x 2.65)	T = 85°C, RH = 85%, 3 reflow	0	25 x 2, 77 x 2	168
MSL1	EPC2032	80	XL (4.65 x 2.65)	T = 85°C, RH = 85%, 3 reflow	0	77 x 1	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	77 x 3	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168
MSL1	EPC800x	40	S (2.05 x 0.85)	T = 85°C, RH = 85%, 3 reflow	0	25 x 1	168

Table 12. Moisture Sensitivity Level Test   Note: EPC800x results are applicable to all products in the EPC8000 series

Electrostatic Discharge

Parts were subjected to ESD HBM, MM, and CDM in accordance with the JEDEC Standard JESD22A-114 [9] Human Body Model, JESD22A-115 [10] Machine Model, JESD22C-101 [11] Charged Device Model. EPC2001 and EPC800x were selected for the test to cover the die size range.the IPC/JEDEC joint Standard J-STD-020 [8].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 400 V	(+) 500 V	1A
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 1500 V	(-) 2000 V	1C
HBM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 200 V	(-) 400 V	B
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 400 V	(+) 600 V	C
MM	EPC2001	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 600 V	—	> Class C

Table 13. Electrostatic Discharge Test EPC2001

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin G-S	(±) 3000 V	(-) 4000 V	2
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin G-D	(±) 2000 V	(-) 3000 V	2
HBM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin D-S	(±) 2000 V	(+) 3000 V	2
CDM	EPC2001C	100	L (4.11 x 1.63)	Pin to Pin - All Pins	(±) 1000 V		C3

Table 14. Electrostatic Discharge Test EPC2001C

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	Passed Voltage	Failed Voltage	JEDEC Class
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 350 V	(-) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 350 V	(+) 500 V	1A
HBM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 500 V	(+) 1000 V	1B
CDM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin - All Pins	(±) 500 V	(-) 500 V	1C
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-S	(±) 25V	(+) 50 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin G-D	(±) 100 V	(-) 200 V	A
MM	EPC800x	40	S (2.05 x 0.85)	Pin to Pin D-S	(±) 50 V	(+) 100 V	A

Table 15. Electrostatic Discharge Test EPC800x   Note: EPC800x results are applicable to all products in the EPC8000 series

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