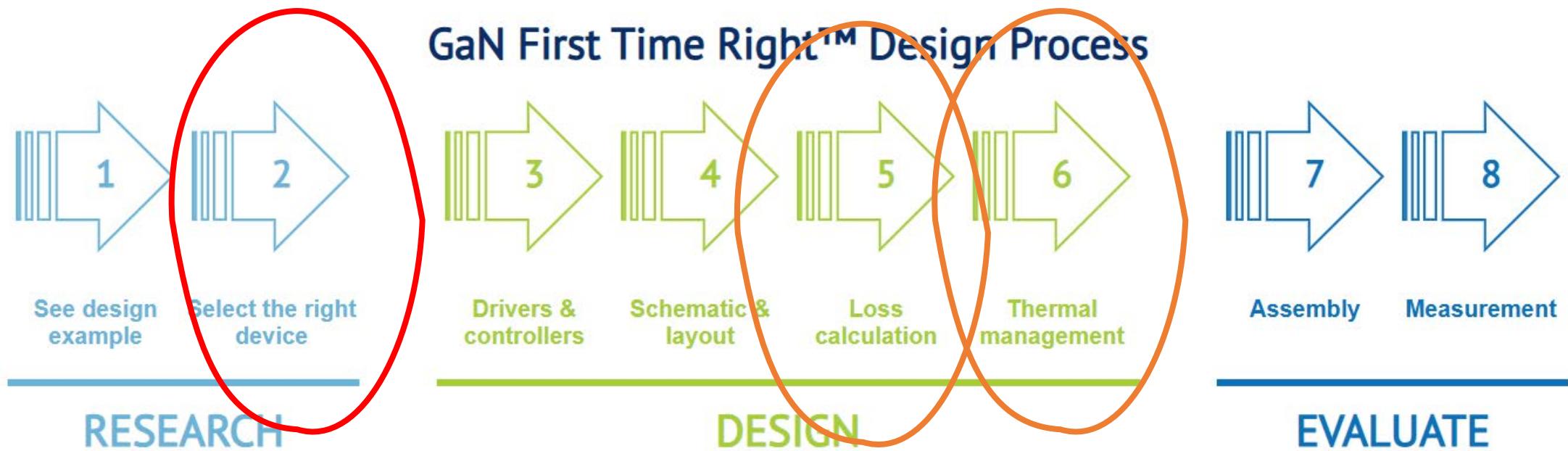
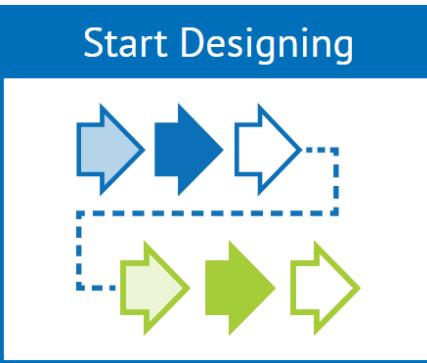


GaN First Time Right: Web-based Design Tools

Andrea Gorgerino
Director, WW FAE



GaN First Time Right



Tools

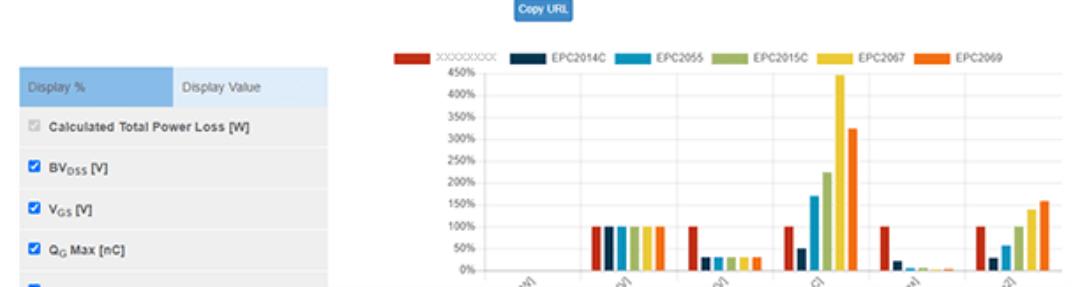
Cross reference tool



- Powered by DiscoverEE database: 20,000 MOSFETs from 28 manufacturers
- Compares the most cost-effective EPC products that **beat** Si MOSFET performance, in most cases at a **lower cost**
- Detailed datasheet comparison, including calculation of parameters in same conditions

MOSFET Operating Conditions	Vbus [V]	RgTotal [mΩ]	ID [A]	Duty Cycle	TA [C]	fsw [kHz]	300	Update
Part Number	XXXXXXX	EPC2014C	EPC2055	EPC2015C	EPC2067	EPC2069		
BV _{DSS} [V]	40	40	40	40	40	40		
V _G [V]	-20, 20	-4, 6	-4, 6	-4, 6	-4, 6	-4, 6		
Q _G Max [nC]	5	2.5	8.5	11.2	22.3	16.2		
R _{DS(on)} [mohm] (Max)	75.00	16.00	3.60	4.00	1.55	2.25		
Gate Drive [V]	10	5	5	5	5	5		
Calculated Total Power Loss [W]	0.17	0.05	0.05	0.07	0.11	0.11		

Powered By DiscoverEE. Visit us at www.discoveree.io



Display % Display Value

Calculated Total Power Loss [W]

BV_{DSS} [V]

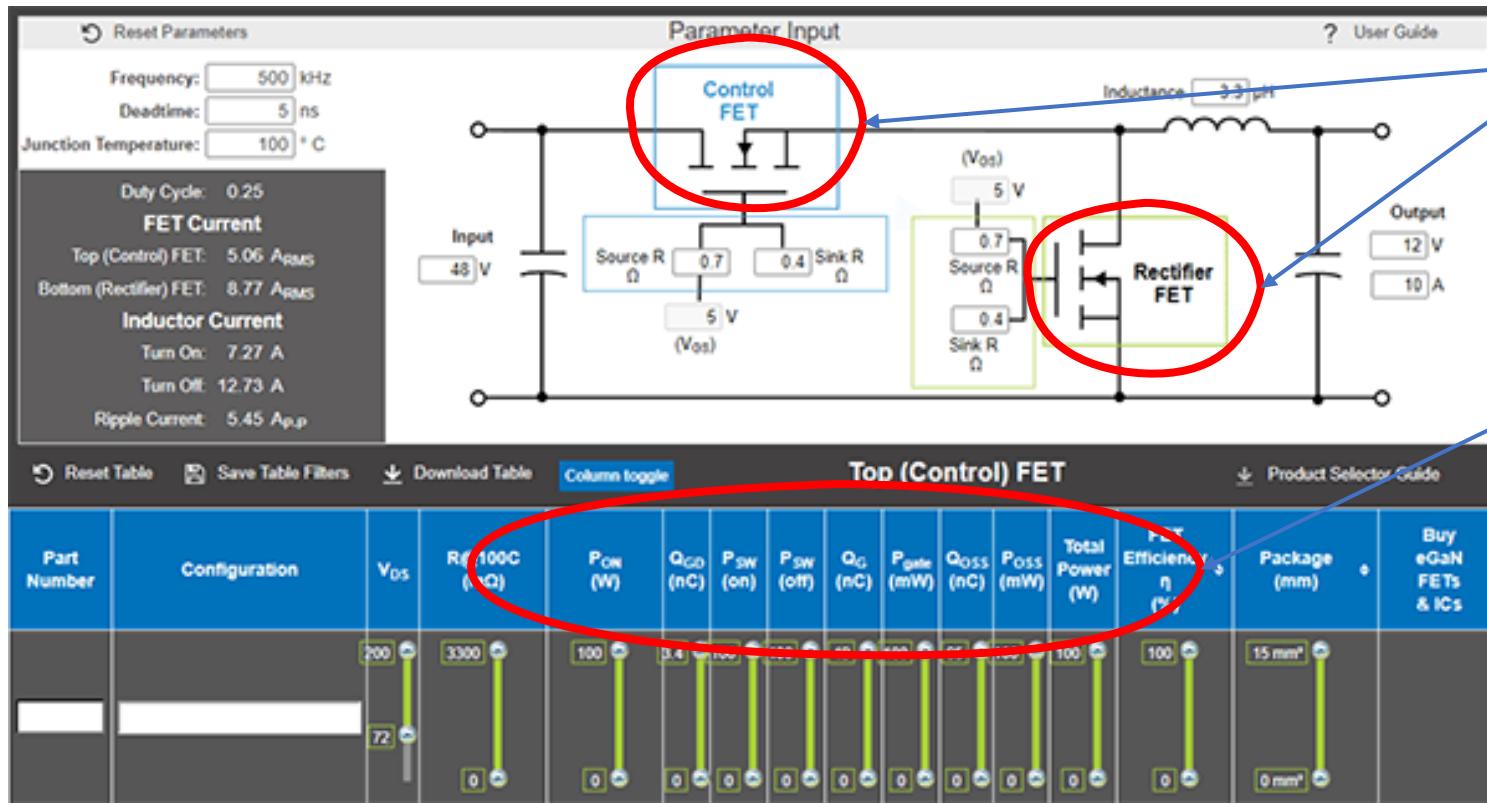
V_G [V]

Q_G Max [nC]

Table of Contents	
Part Comparison Summary	Calculated I_D & P_D Ratings
Digikey Inventory & Price	Calculated Switching Times
Detail Parts Specifications	Power Loss Calculations
Figure of Merit	Power Loss Breakdown Chart

Sync buck tool

- Formula based loss analysis for synchronous buck converter
- Calculations for all EPC products



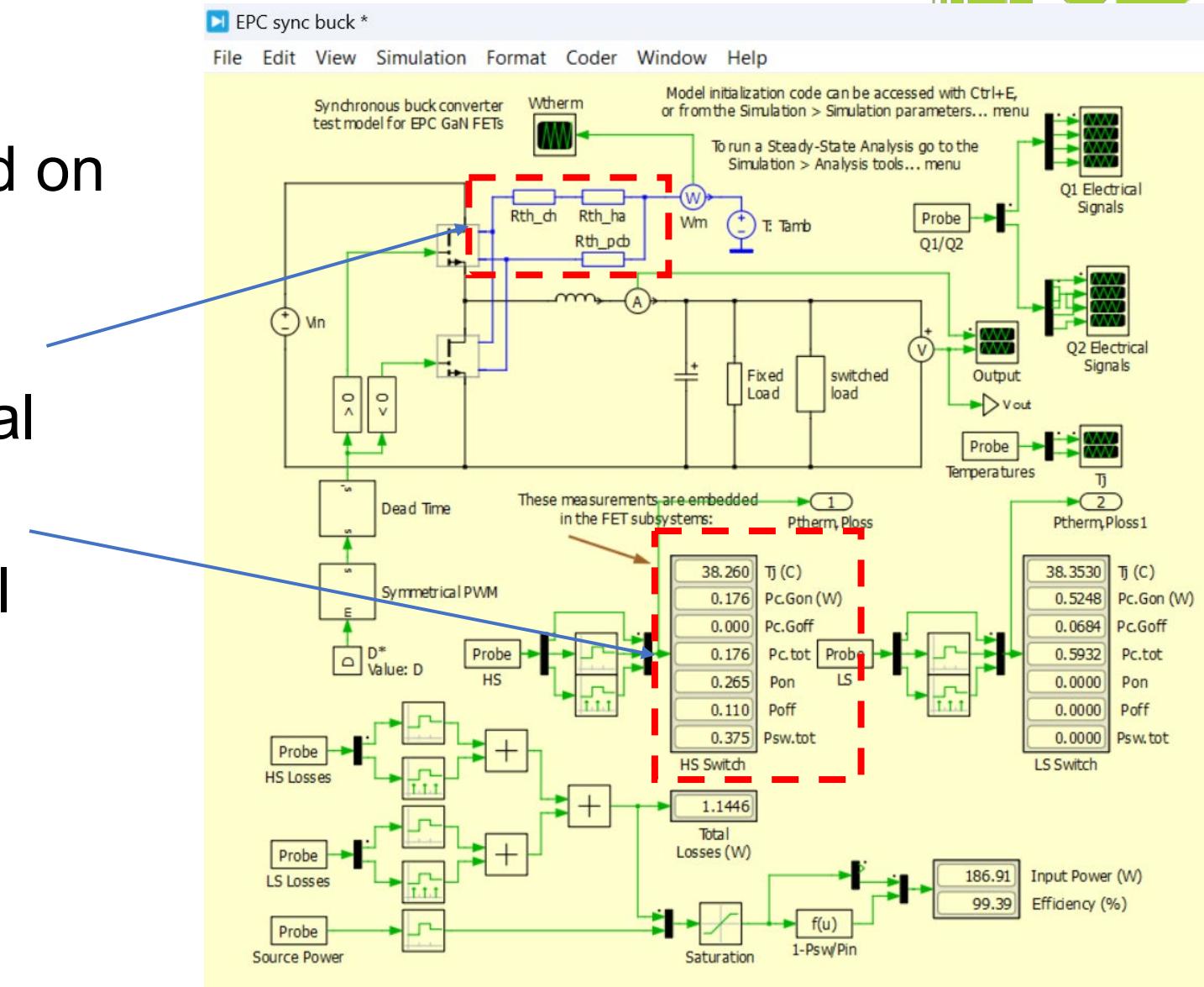
Calculations for both control and synchronous FETs

More detailed loss calculation

Electrical models: PLECS

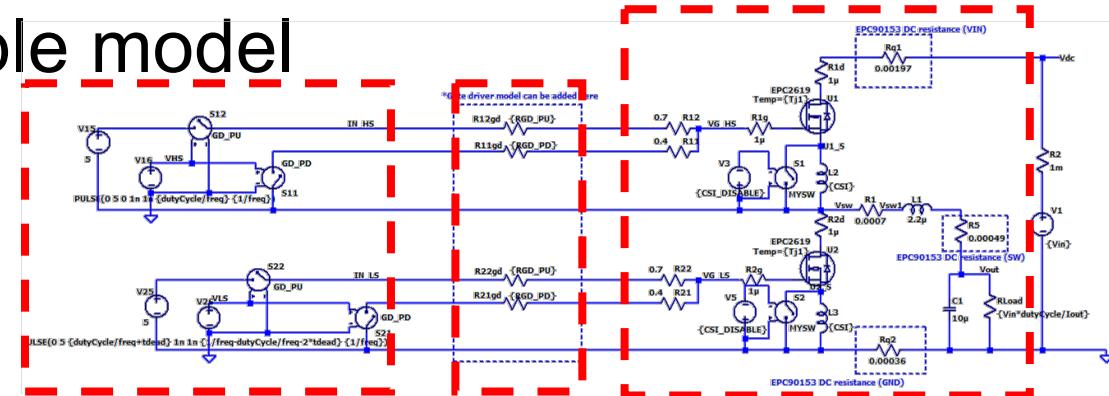


- Custom thermal model based on formula loss calculations (for symmetrical half-bridge)
- Dual port models support dual sided cooling
- Custom models have internal measurement capabilities
- Example circuit



Electrical models: Spice

- Spice models: LTS spice, Pspice, Tspice, Spectre, SIMetrix/SIMPLIS
 - Continuous model for GaN FETs and circuit
 - Gate driver model
 - PCB parasitics, especially CSI
 - Passive components parasitics
- LTS spice example model



PWM generator based on simple application inputs (f_{sw} , duty cycle, V_{IN}/V_{OUT} , I_{OUT} , L)

Simplified gate driver model

Circuit model with first level parasitic components (CSI, PCB resistance)

Loss analysis via .meas

Thermal calculator

- Parametrized tool based on FEA modeling: calculates temperature and thermal model parameters in steady state
- No detailed design required: suitable for initial device selection, iterative process with loss calculation
- PCB only cooling: vias, layers and airflow
- Heatsink cooling: TIM, heat-spreader, heatsink calculator, airflow

Navigation

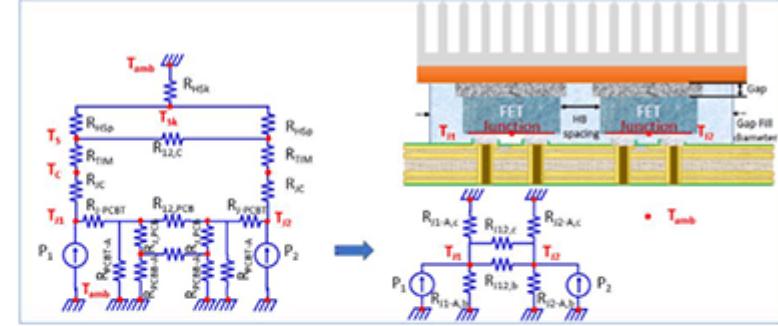
- Input Parameters
- Results
- Detailed Report

Input Parameters

	This case
EPC2218	0.00
FETI	3.50
FETw	1.95
P	5.00
PCB_I	8.00
PCB_Oz	2.00

Results

Device 1: Operating Temperature (Temperature ris...
39.7 °C (19.7 °C)



Input Parameters

Device parameters

Device Configuration Single Device Symmetric H-Bridge

EPC Device Losses P1 (W) Vias

EPC2218 Number of vias 1

Demo boards



- EPC90xx: half-bridge boards for quick prototyping, available for all EPC GaN FETs
 - EPC91xx: application specific design
 - Technology partner reference designs



EPC90153 half-bridge board for EPC2619



EPC9159 1kW LLC using EPC2619 and EPC2067



Example

Simple buck converter



- Current design
 - 48/12V 300kHz
 - P= 260W ($I_{OUT}=22A$)
 - FDMS2D5N08C 80V, 2.2mΩ
- Goal: increase switching frequency and understand the value of GaN
 - 500kHz

Cross reference

Part Comparison Summary:							
FET Operating Conditions		Vbus[V]= 40 , RgTotal= 2 , Ib[A]= 30 , DC= 0.5 , TA[C]= 25 , fsw[kHz]= 300 , RthCA[°C/W]= 5					
		Hard-switch	Update with same parts	Update with new recommendations			
Part Number	FDMS2D5N08C (ON Semi)	EPC2204 x	EPC2204A x	EPC2065 x	EPC2059 x	EPC2619 x	
Modify EPC Part		»	»	»	»	»	
BVDSS [V]	80.0	100.0	80.0	80.0	170.0	100.0	
R _{DS(ON)} [mΩ] [Typ]	2.20	4.40	4.40	2.70	6.80	3.30	
R _{THJC} [°K/W]	0.90	1.00	1.00	0.50	0.90	1.00	
Q _G Typ [nC]	60.0	5.70	5.70	9.40	5.70	8.50	
Gate Drive [V]	10.0	5.00	5.00	5.00	5.00	5.00	
Gate Drive Loss [W]	0.18	0.0086	0.0086	0.014	0.0086	0.013	
Package Area [mm ²]	W=5.00mm, L=6.00mm Area=30.0 mm ²	W=1.50mm, L=2.50mm Area=3.8 mm ²	W=1.50mm, L=2.50mm Area=3.8 mm ²	W=1.95mm, L=3.5mm Area=6.8 mm ²	W=1.40mm, L=2.80mm Area=3.9 mm ²	W=1.50mm, L=2.50mm Area=3.8 mm ²	
Calculated Total Power Loss [W]	5.98	2.73	2.66	2.30	4.08	2.28	
Auto Qualified	No	No	Yes	No	No	No	
Status	Promotion	Preferred	Preferred	Preferred	Preferred	Preferred	
Quantity Available at Digi-Key	FDM S2D5N08C: 2651	EPC2204A: 17025	EPC2204A: 17025	EPC2065: 3471	EPC2059: 20814	EPC2619ENGRT: 0	
Digi-Key Pricing	FDM S2D5N08C: 1 = \$2.88 10 = \$2.417 100 = \$1.9556 500 = \$1.73834 1000 = \$1.48845	EPC2204A: 1 = \$2.9 10 = \$2.405 100 = \$1.9144 500 = \$1.61984 1000 = \$1.37441	EPC2204A: 1 = \$2.9 10 = \$2.405 100 = \$1.9144 500 = \$1.61984 1000 = \$1.37441	EPC2065: 1 = \$3.21 10 = \$2.697 100 = \$2.1816 500 = \$1.9392	EPC2059: 1 = \$3.32 10 = \$2.787 100 = \$2.2543 500 = \$2.003 1000 = \$1.715	EPC2619ENGRT: ShareFile 1 = \$3.48	
Lead Weeks	24 week(s)	16 week(s)	16 week(s)	16 week(s)	16 week(s)	No lead time information available	

Default conditions

Expected 50% reduction of losses

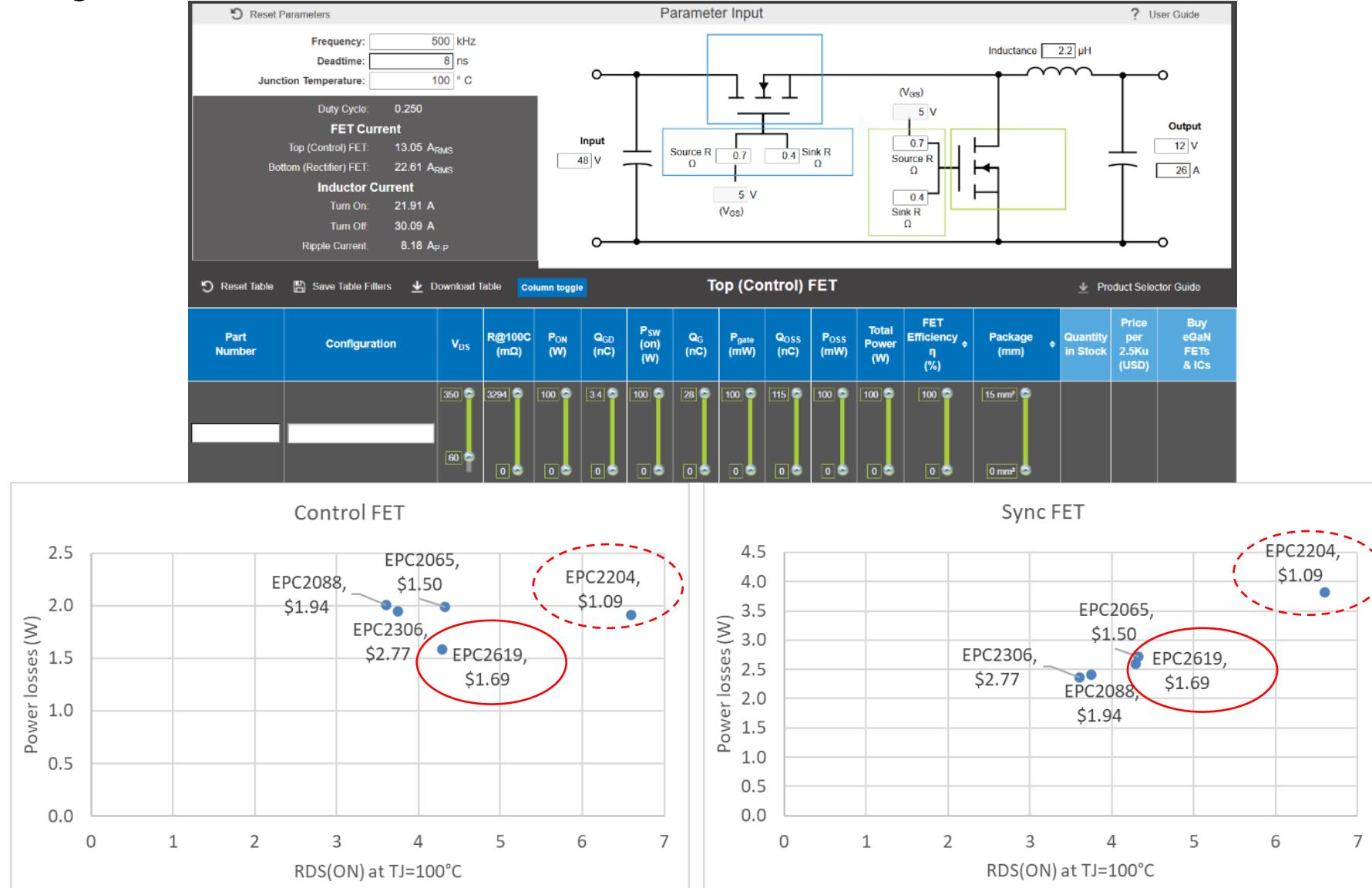
Update your conditions



Part Comparison Summary:						
FET Operating Conditions		Vbus[V]= 48 , RgTotal= 2 , Id[A]= 26 , DC= 0.25 , TA[C]= 50 , fsw[kHz]= 500 , RthCA[°C/W]= 5				
		Hard-switch	Update with same parts	Update with new recommendations		
Part Number	FDMS2D5N08C (ON Semi)	EPC2052 x	EPC2044 x	EPC2252 x	EPC2619 x	EPC2214 x
Modify EPC Part		»	»	»	»	»
BVDSS [V]	80.0	100.0	100.0	80.0	100.0	80.0
RDS(ON) [mΩ] [Typ]	2.20	10.0	7.00	8.00	3.30	15.0
RTHJC [°K/W]	0.90	2.00	1.30	1.60	1.00	2.70
QG Typ [nC]	60.0	3.50	4.30	3.50	8.50	1.80
Gate Drive [V]	10.0	5.00	5.00	5.00	5.00	5.00
Gate Drive Loss [W]	0.30	0.0088	0.011	0.0088	0.021	0.0045
Package Area [mm²]	W=5.00mm, L=6.00mm Area=30.0 mm²	W=1.50mm, L=1.50mm Area=2.3 mm²	W=1.25mm, L=2.15mm Area=2.7 mm²	W=1.50mm, L=1.50mm Area=2.3 mm²	W=1.50mm, L=2.50mm Area=3.8 mm²	W=1.35mm, L=1.35mm Area=1.8 mm²
Calculated Total Power Loss [W]	8.51	2.83	2.12	2.21	1.92	3.73
Auto Qualified	No	No	No	Yes	No	Yes
Status	Promotion	Preferred	Preferred	Preferred	Preferred	Active
Quantity Available at Digi-Key	FDMS2D5N08C: 2651	EPC2052: 133145	EPC2044: 6937	EPC2252: 24884	EPC2619ENGR: 0	EPC2214: 20060
Digi-Key Pricing	FDMS2D5N08C: 1 = \$2.88 10 = \$2.417 100 = \$1.9556 500 = \$1.73834 1000 = \$1.48845	EPC2052: 1 = \$1.52 10 = \$1.262 100 = \$1.0044 500 = \$0.84992 1000 = \$0.72114	EPC2044: 1 = \$1.67 10 = \$1.386 100 = \$1.1029 500 = \$0.93324 1000 = \$0.79184	EPC2252: 1 = \$1.79 10 = \$1.485 100 = \$1.1817 500 = \$0.9999 1000 = \$0.8484	EPC2619ENGR: 1 = \$3.48	EPC2214: 1 = \$1.19 10 = \$0.992 100 = \$0.7892 500 = \$0.7125
Lead Weeks	24 week(s)	16 week(s)	16 week(s)	12 week(s)	No lead time information available	16 week(s)

500kHz increases the advantage of GaN:
 Si MOSFET losses increase much more than GaN FETs

Sync buck losses



A few more input parameters provides a more detailed analysis

Different recommendations for both control and sync FETs

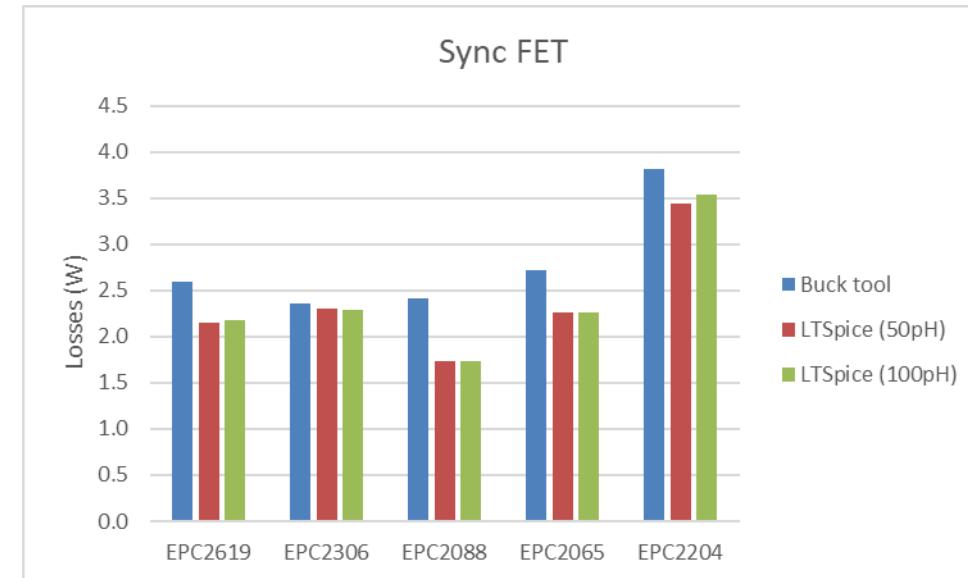
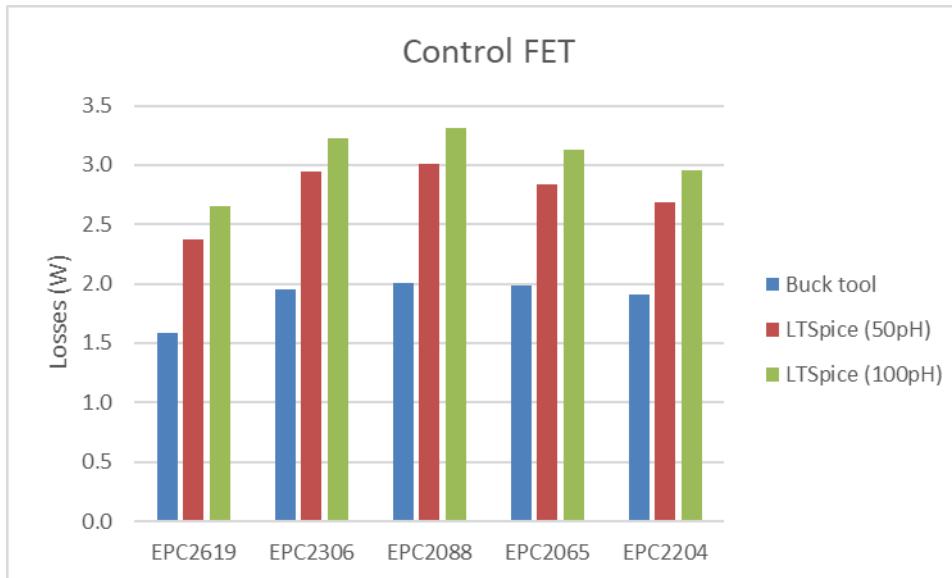
Losses and price for all EPC GaN FETs

EPC2619 latest generation eGaN FET

Detailed loss simulation

Example model from EPC LTSPice library (CSI= 100pH)

- HS: 1.6 W → 2.7 W
- LS: 2.6 W → 2.2 W



Impact of CSI: 50-100pH

Thermal verification - datasheet



Thermal Characteristics			
	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	1	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	2.6	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	66	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (EPC90153 EVB)	46	

- R_{thJC} : Used for double sided cooling, the best way to take advantage of the power density of GaN
- R_{thJB} : PCB cooling only path
- $R_{\text{thJA_JEDEC}}$: PCB cooling only path measured in a std condition (natural convection)
- $R_{\text{thJA_EVB}}$: PCB cooling only path measured on a real board EPC90153 (natural convection)
 - Control FET: $2.7 \text{ W} \rightarrow \Delta T = 124 \text{ }^{\circ}\text{C}$
 - Sync FET: $2.2 \text{ W} \rightarrow \Delta T = 101 \text{ }^{\circ}\text{C}$
 - → Need different thermal concept

Thermal verification – thermal tool

- Application conditions

Device Parameters

Device Configuration (?) EPC FETs and ICs (?) Device 2 (?)

Single Device Two Devices: Symmetric Two Devices: Asymmetric

EPC2619 EPC2619

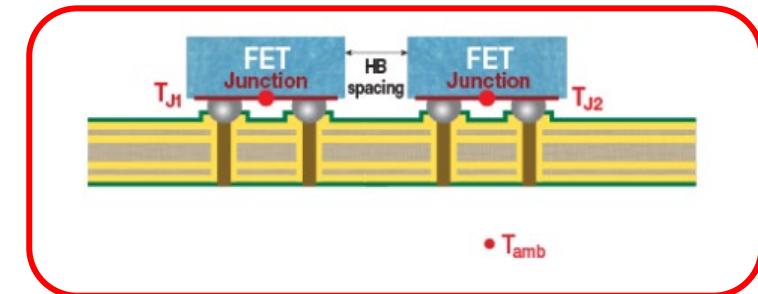
R_{th},JC = 1.0 °C/W R_{th},JC2 = 1.0 °C/W

Ambient Temperature (°C) 25 R_{th},JB = 2.5 °C/W R_{th},JB2 = 2.5 °C/W

2.5mmx1.5mm=3.8mm² 2.5mmx1.5mm=3.8mm²

Vias in Pad Losses (W): Device#1 Losses (W): Device#2

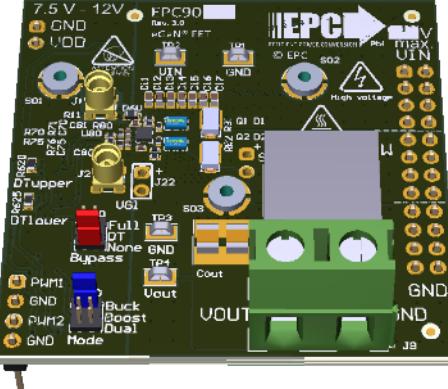
Spacing (mm) 2.70 2.20



PCB parameters: concept design



- Customer PCB concept
- Half-bridge demo board EPC90153 (EPC2619)



EPC2619 via pattern on EPC90153

Stack Up		Layer Stack		
Layer	Board Layer Stack	Name	Material	Thickness
1		Top Paste		
2		Top Overlay		
3		Top Solder	Solder Resist	0.40mil
4		Top Layer	Copper	2.76mil
5		Dielectric 1	FR370-HR	5.00mil
6		Mid-Layer 1	Copper	2.76mil
7		Dielectric 2	FR370-HR	9.70mil
8		Mid-Layer 2	Copper	2.76mil
9		Dielectric 3	FR370-HR	15.00mil
10		Mid-Layer 3	Copper	2.76mil
11		Dielectric 4	FR370-HR	9.70mil
12		Mid-layer 4	Copper	2.76mil
13		Dielectric 5	FR370-HR	5.00mil
14		Bottom Layer	Copper	2.76mil
15		Bottom Solder	Solder Resist	0.40mil
16		Bottom Overlay		
17		Bottom Paste		

Height : 61.76mil

Layer stack-up for EPC90153

The screenshot shows the EPC CoolPad software interface with several parameters highlighted by red boxes:

- spacing (mm):** 2.00 (with +/- buttons) and Die Power Density = 43 W/cm², Die Power Density = 69 W/cm².
- Number of vias, Device#1:** 10 and **Via Density:** 2.7 vias/mm².
- Number of vias, Device#2:** 18 and **Via Density:** 4.8 vias/mm².
- Insignificant PCB cooling/ No airflow to PCB:** Unchecked checkbox.
- Has Heatsink/ Case-side Cooling Solution:** Unchecked checkbox.
- PCB Parameters:**
 - PCB stackup:** 6 layers, 2 oz copper and PCB Conductor Area: 2.0inx2.0in.
 - PCB Thickness:** Standard: 1.6mm (radio button selected), User Set, Advanced PCB Stackup.
 - Conductor Area:** 2581 mm², 4.0 in².
 - Air Flow to PCB (LFM):** Sliders set at 400 and 1000.

Thermal verification results

Analyze impact of:

- PCB, heatsinking and airflow
- High side and low side differentiation
- Mutual heating

With 400LFM:

Device 1:

Junction Temperature (Temperature Rise):

77.6°C (52.6°C)

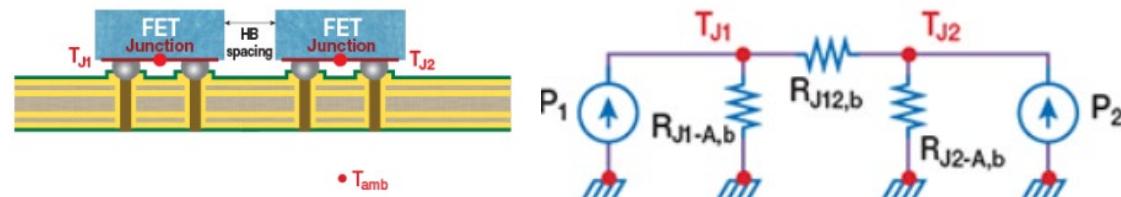
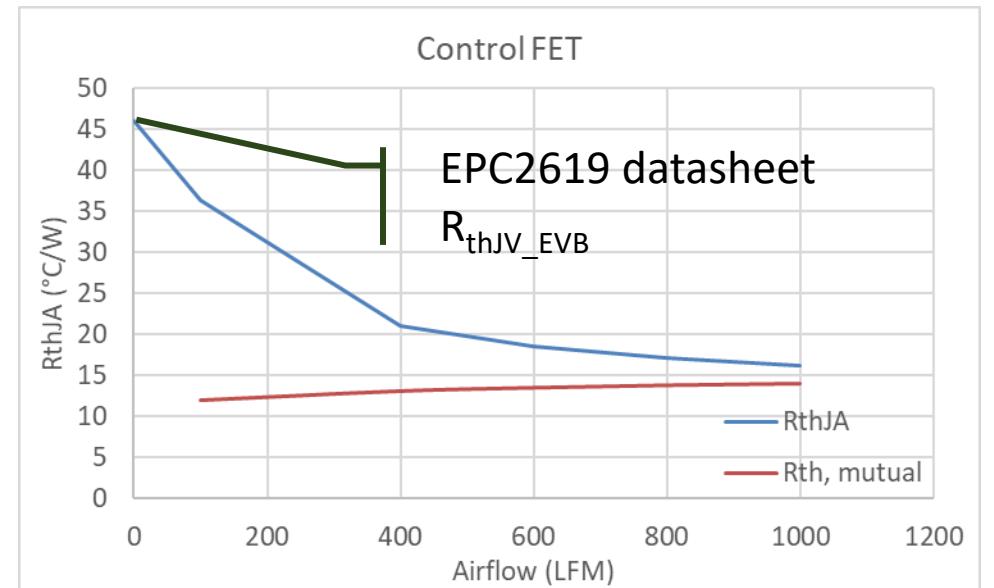
Device 2:

Junction Temperature (Temperature Rise):

75.0°C (50.0°C)

P1 = 2.7 W

P2 = 2.2 W



$$R_{J1-A,b} (\text{°C/W}) =$$

21.0

$$R_{J12,b} (\text{°C/W}) =$$

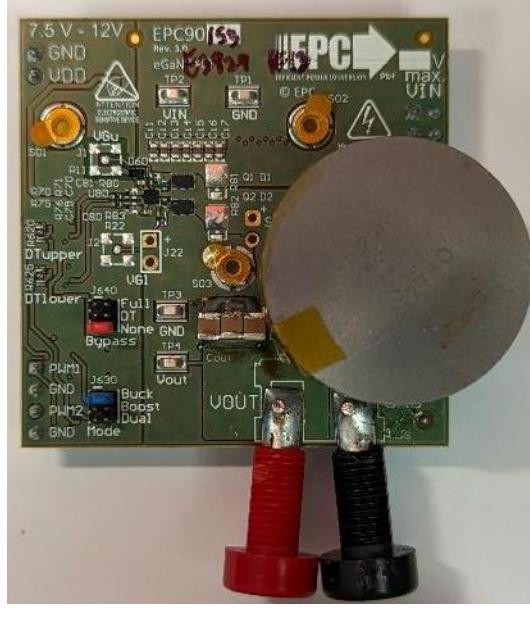
13.1

$$R_{J2-A,b} (\text{°C/W}) =$$

20.9

Real measurements

EPC2619 on EPC90153

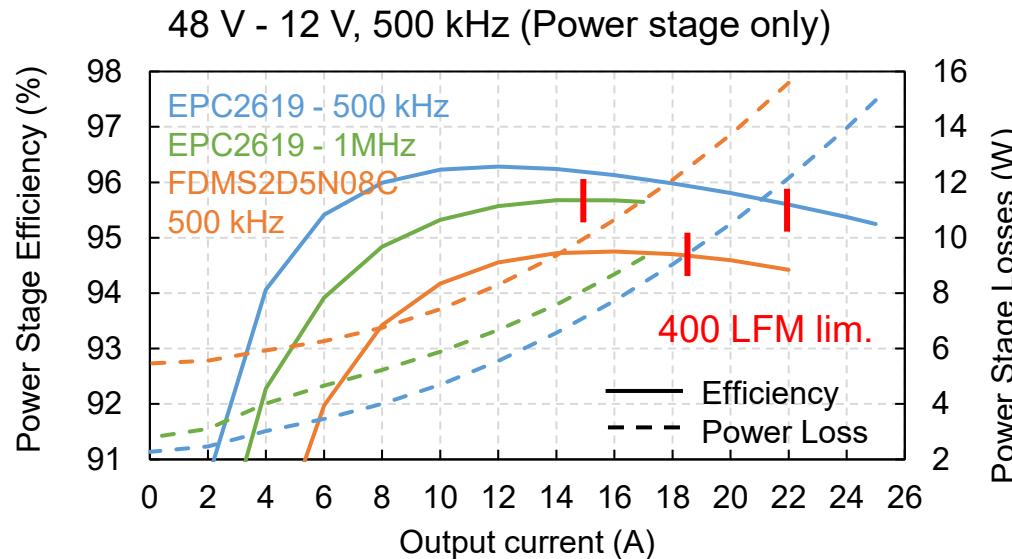


FDMS2D5N08C



Performance comparison

Measurements confirm that EPC2619 has lower losses and can carry more current



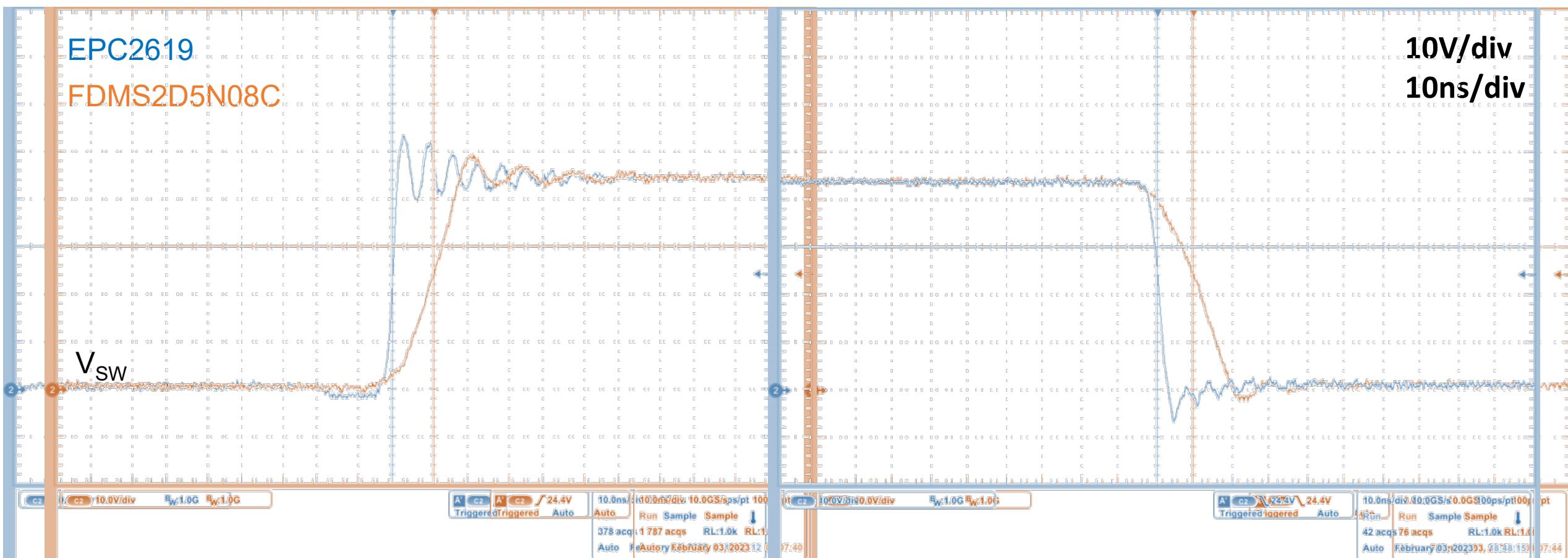
- Power Stage Efficiency and losses include FET losses and inductor
- Maximum current displayed corresponds to a maximum case temperature of ~105°C in thermal steady state with 1000 LFM

	400 LFM	1000 LFM
EPC2619 (500 kHz)	22 A	24.5 A
EPC2619 (1 MHz)	15 A	17 A
FDMS2D5N08C	18.5 A	22 A

Table with maximum output current for different airflow and $T_C \leq 105^\circ\text{C} - 107^\circ\text{C}$

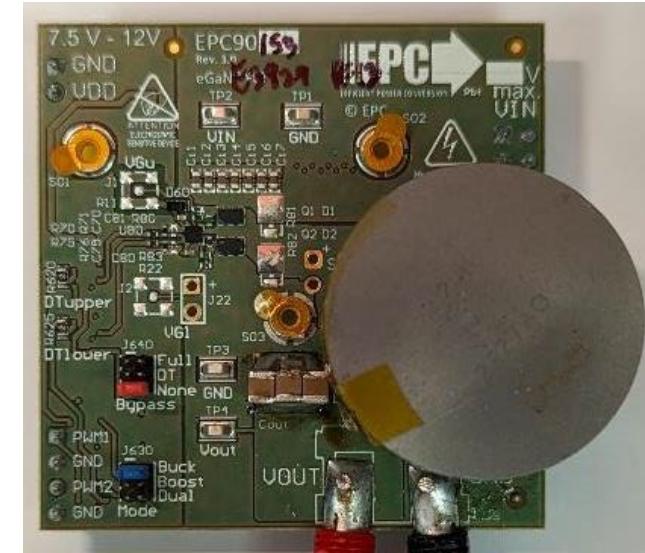
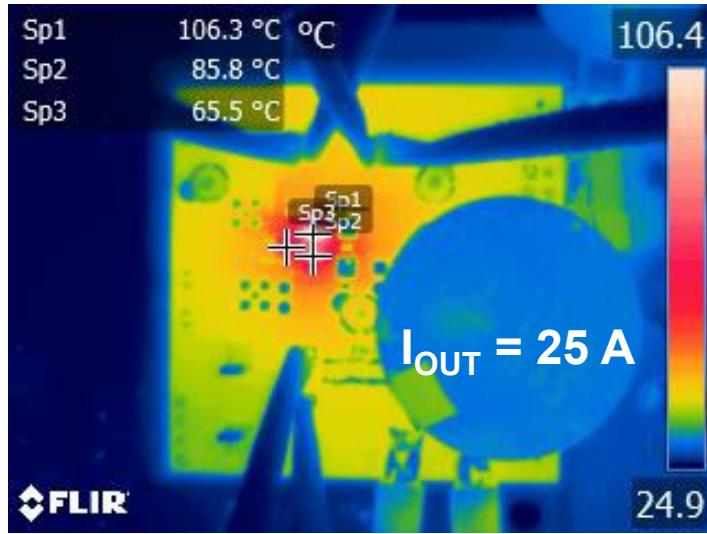
Waveform 20A (48 Vin, 12 Vout)

Switch node Waveform Comparison: R_g tuning

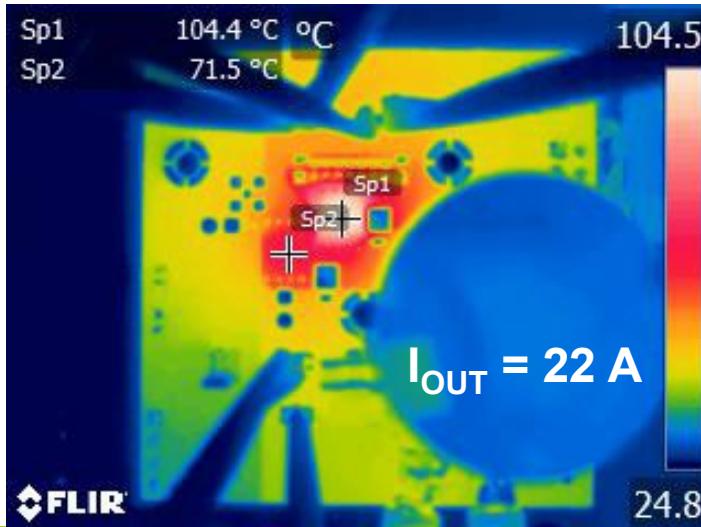


Thermal Equilibrium 48/12 V, 500 kHz

EPC2619



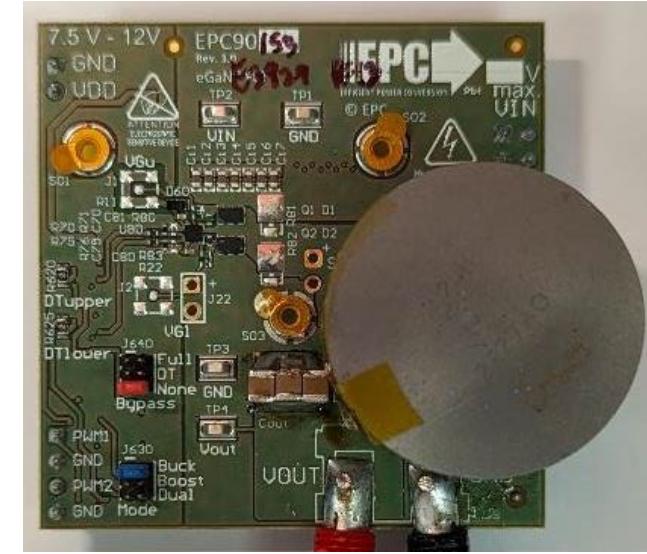
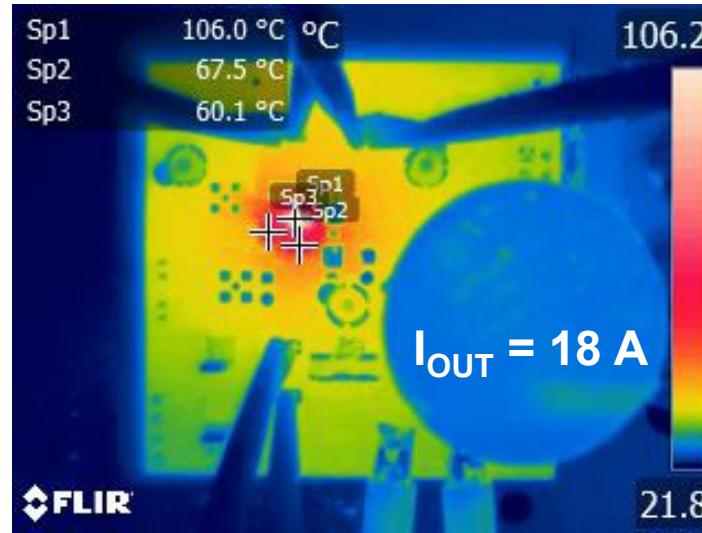
FDMS2D5N08C



No heatsink, 1000 LFM

Thermal Equilibrium 48/12 V, 1 MHz

EPC2619



No heatsink, 1000 LFM

Summary



In the example we used the web tools to compare a Si MOSFET to EPC eGaN FETs, and confirmed via measurements that EPC2619 has lower losses, can carry more current and is cheaper than the original Si MOSFET

1. The cross reference provides the easiest way to compare Si MOSFET to GaN, including pricing
2. The loss calculators and simulations provide mode detailed device optimization and trade-off analysis
3. The thermal tool provides a fast and flexible way to assess thermal concepts and trade-off analysis
4. Finally, the hardware boards help to validate the device selection