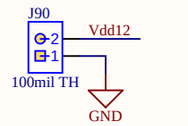
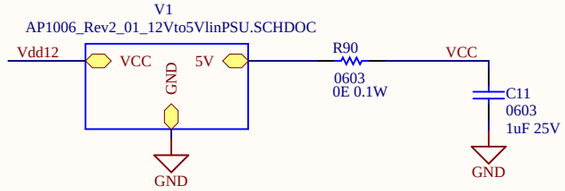
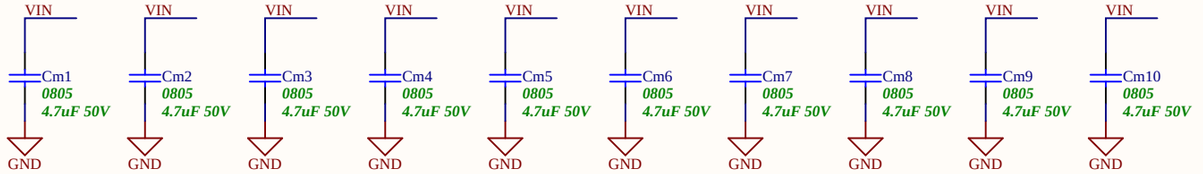


Logic Supply

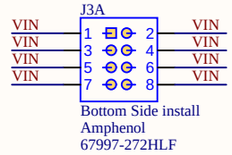
12VDC



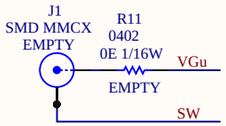
5 V Logic Regulator



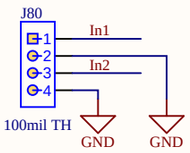
Intermediate Capacitors



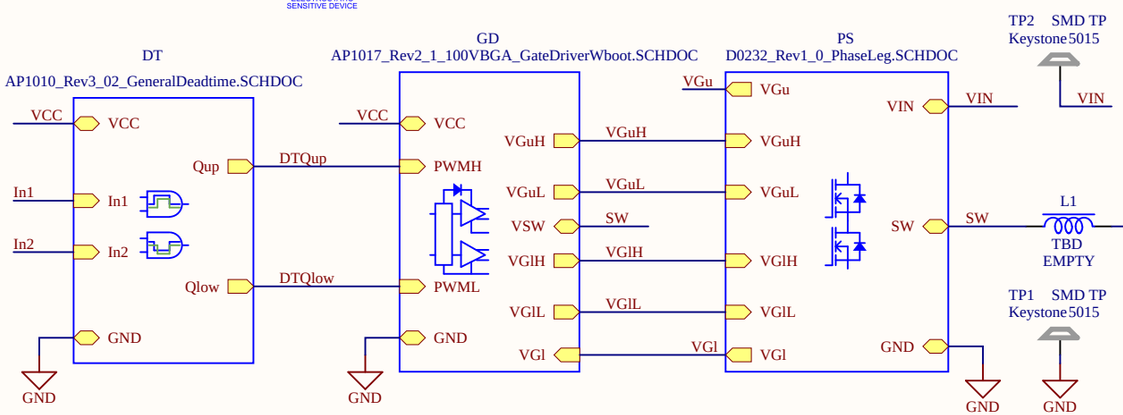
Main Supply Input



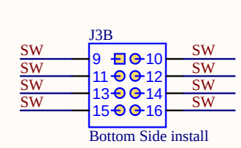
Upper Gate



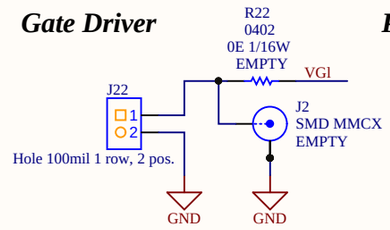
Signal Inputs



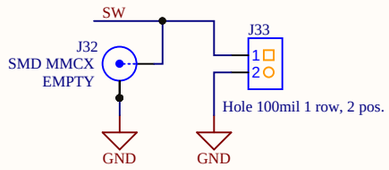
dead-time and buffers ***Gate Driver*** ***Power Stage*** ***Sync Buck Output***



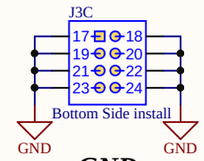
SW Output



Lower Gate

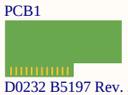


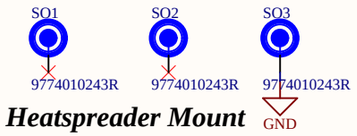
Switch-node



GND

For evaluation only;
not FCC approved for resale





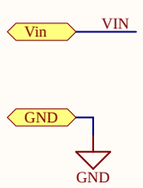
Heatspreader Mount

 eGaN® FET

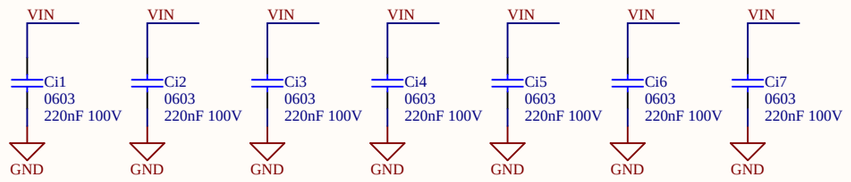
Evaluation Board Main Schematic

Title	EPC90146_B5197_Rev3_0		
Size: A	1	Revision: 1	
Date: 9/8/2022		Sheet 1 of 5	
File: D0232_B5197_Rev3_0.SCHDOC			

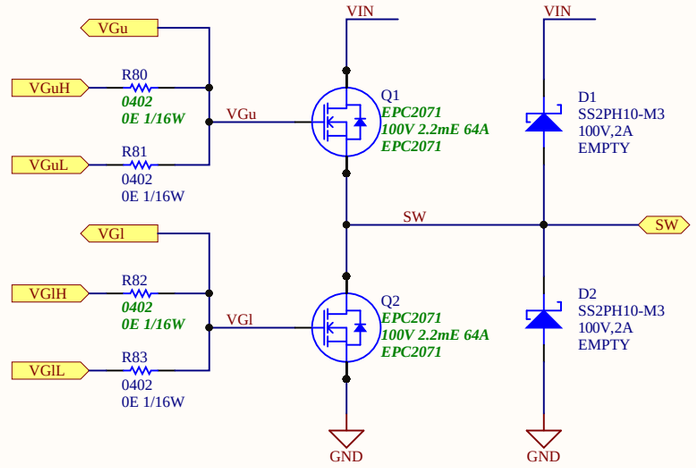
Efficient Power Conversion
909 N. Pacific Coast Hwy, Ste. 23
El Segundo, CA 90245
United States
www.epc-co.com



DC Input
80 Vmax.



HF loop Capacitors



Power Stage ***Optional Diodes***

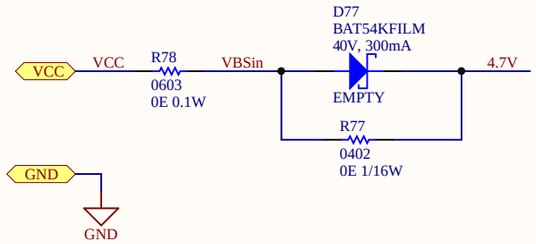
EPC2071

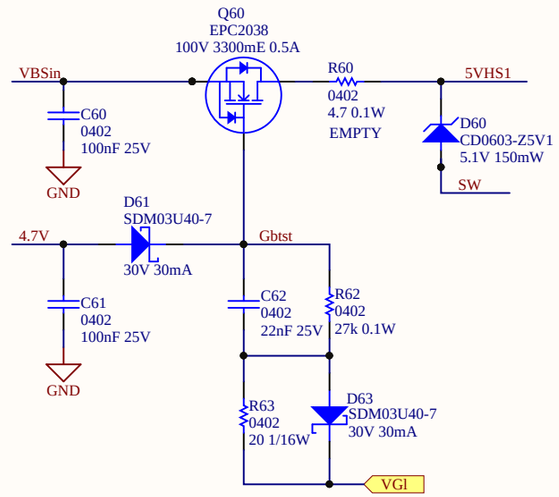
Title D0232 Phase Leg Rev 1.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	2	Revision: 1	
Date: 11/17/2022		Sheet 2 of 5	
File: D0232_Rev1_0_PhaseLeg.SCHDOC			

Sync Boot = Install R60 and D77, remove R77

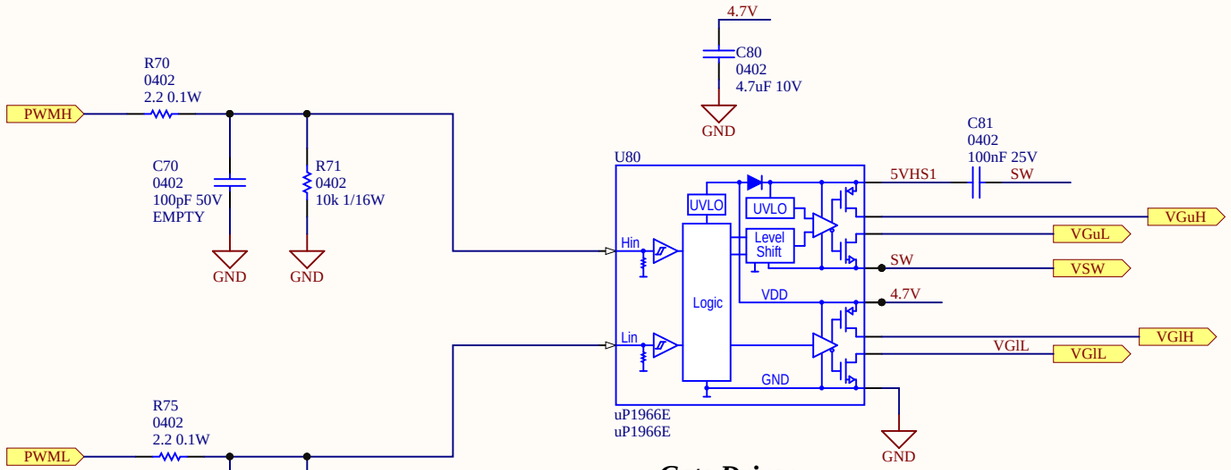
No Sync Boot = Install R77, remove R60 and D77

Default = No Sync Boot





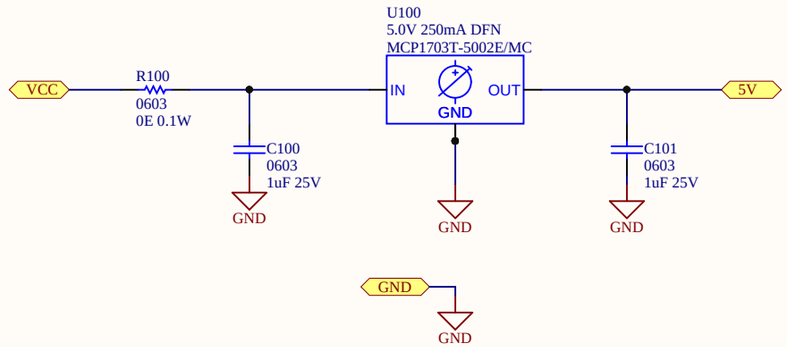
Synchronous Boostrap Power Supply



Gate Driver

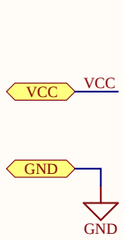
100 V Gate Driver with Bootstrap

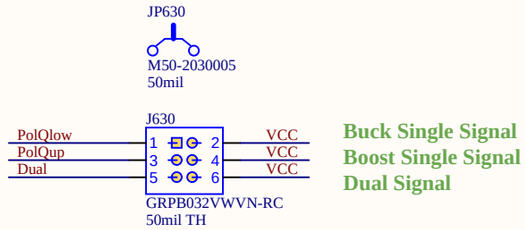
Title AP1017 Rev. 2.1		Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A 3	Revision: 1	
Date: 9/8/2022	Sheet 3 of 5	
File: AP1017_Rev2_1_100VBGA_GateDriverWboot.SCHDOC		



12 V to 5 V LDO power supply

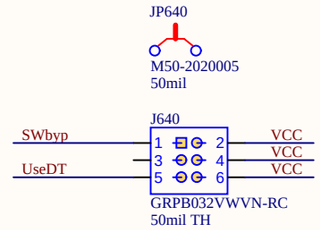
Title AP1006 Rev. 2.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	4	Revision: 1	
Date: 9/2/2022		Sheet 4 of 5	
File: AP1006_Rev2_01_12Vto5VlinPSU.SCHDOC			





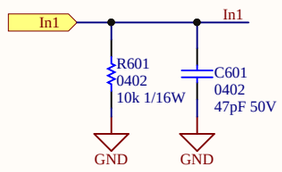
Buck Single Signal
Boost Single Signal
Dual Signal

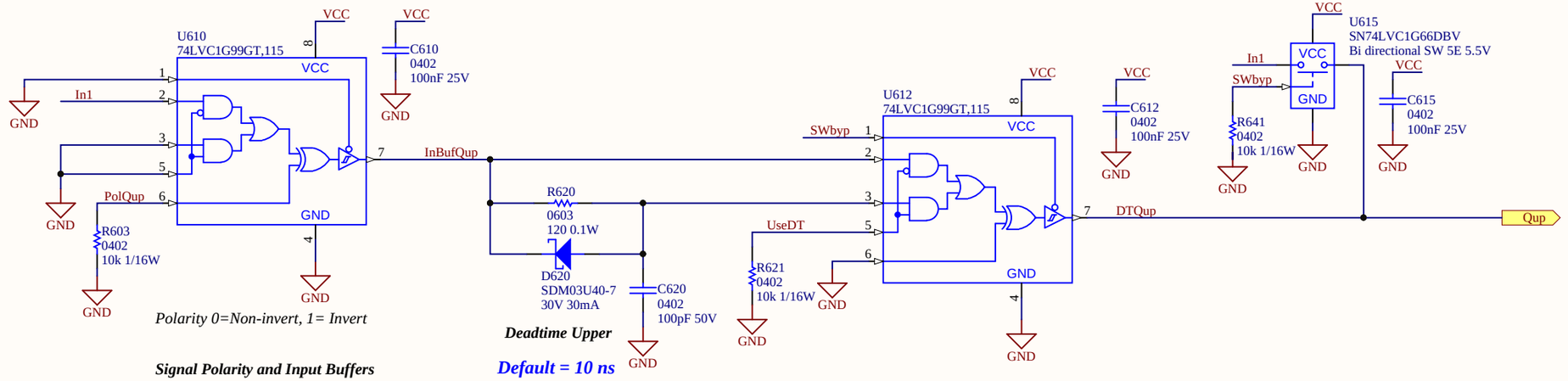
Dual/Single PWM, Buck, and Boost Mode Selector



Full Bypass
DT Bypass
No Bypass

Bypass Mode Select





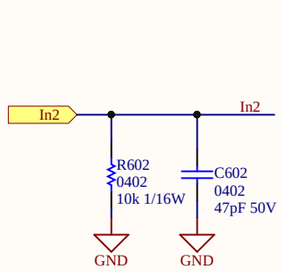
Polarity 0=Non-invert, 1= Invert

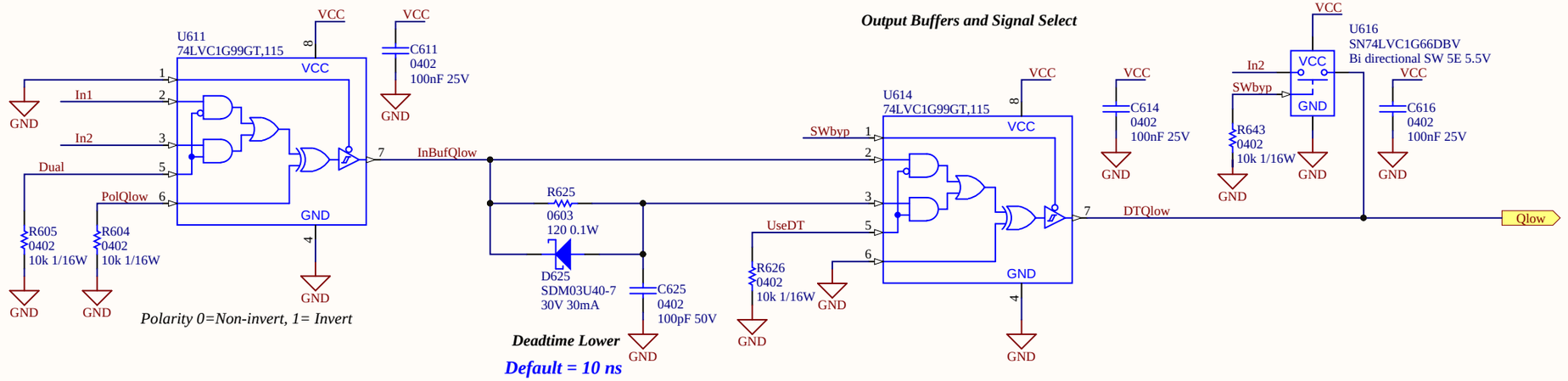
Signal Polarity and Input Buffers

Deadtime Upper

Default = 10 ns

Output Buffers and Signal Select





Polarity 0=Non-invert, 1= Invert

Deadtime Lower

Default = 10 ns

Output Buffers and Signal Select

General Dead-time with Polarity Changer and Bypass

Title AP1010 Rev. 3.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	5	Revision: 1	
Date: 9/2/2022		Sheet 5 of 5	
File: AP1010_Rev3_02_GeneralDeadtime.SCHDOC			