Figure 15: EPC9167 main schematic
9 V min. to 80 V max.

UVLO Settings:
- 8 V on, 1.73 V hysteresis

PSU disconnect

Figure 16: 80 V to 5 V housekeeping power supply
Figure 17: Bi-Directional Leg Current Sense Amplifier
Figure 18: Bi-Directional Over Current Detection

R12 and C9 are not mounted because they are mounted in front of the gate driver.
Figure 19: EPC2065 Phase-Leg. In EPC9167 only Q1 and Q2 are mounted. In EPC967HC all four transistors (Q1, Q2, Q3, and Q4) are mounted.
**3V3 500 mA max.**

Figure 20: 5 V to 3.3 V LDO Housekeeping Power Supply

Figure 21: 5 V to 3.3 V LDO power supply

Phase Voltage Sense

81.5 V scale to 3.3 V

Figure 22: Phase shunt and phase voltage sense
Shaft Encoder connection
Quadrature with Index
Supports Optical and Hall

5 V
GND
GND

100 mil SMD

EncdrA
EncdrB
EncdrI

VDD
3V3
GND

Figure 23: Shaft-encoder interface schematic

VCC
GND

AGND

R40 0 Ω 0.125 W

U40 AD590JCPZ-R5

GND

AGND

C41 0805 100 nF 50 V

D41 DNP

150°C scale to 3.3 V
25°C scale to 2.3 V
-55°C scale to 1.7 V

Figure 24: Temperature sensor schematic
**Figure 25: Current sense amplifier**

- **INA240A1PWR Gain 20 V/V**
- **Offset Voltage = 1.65 V**

**Figure 26: Heatsink kit schematic**
Figure 27: High Power Motor Drive DC Bus Capacitors
Figure 28: Bi-Directional Over Current Detection

R12 and C9 are not mounted in front of the gate driver.

R12 and C9 are not mounted in front of the gate driver.
The 0 Ω resistor can be modified to filter spikes from the comparators lines.

VddPullup is connected to 3.3 V or to 5 V depending on microcontroller voltage.

Figure 29: Half Bridge Gate Driver