Driving eGaN™ Transistors for Maximum Performance

Johan Strydom: Director of Applications, Efficient Power Conversion Corporation

Alex Lidow: CEO, Efficient Power Conversion Corporation

The recent introduction of enhancement mode GaN transistors (eGaN™) as power MOSFET/ IGBT replacements in power management applications enables many new products that promise to add great system value. In general, an eGaN transistor behaves much like a power MOSFET with a quantum leap in performance, but to extract all of the newly-available eGaN transistor performance requires designers to understand the differences in drive requirements.

eGaN Power Transistor Characteristics

As with silicon power MOSFETs, applying a positive bias to the gate relative to the source of an eGaN power transistor causes a field effect, which attracts electrons that complete a bidirectional channel between the drain and the source. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region and, once again, giving it the capability to block voltage.

To obtain a higher-voltage device, the distance between the drain and gate is increased. Doing so increases the on-resistance of the transistor. However, as the mobility of electrons in a GaN HEMT (high electron mobility transistor) is very high, increasing its blocking voltage capability has much less of an impact on the device's on-resistance than would be the case with a silicon power MOSFET.

Figure 1 compares the theoretical resistance-times-die area limits of GaN, silicon carbide (SiC) and silicon (Si) as a function of voltage [1]. EPC's first generation eGaN transistor is shown as well. Please note that after 30 years of power MOSFET development, silicon has approached its theoretical limits. In contrast, GaN is young in its life cycle, and will see significant improvement in the years to come.

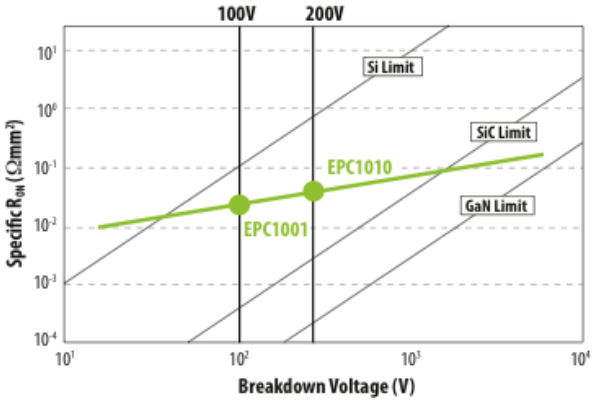

Figure 1. Theoretical resistance times die area limits of GaN, silicon, and silicon carbide versus voltage.

Figure of Merit (FOM)

The FOM is a useful method for comparing power devices and has been used by MOSFET manufactures to show both generational improvements and to compare their parts to others. What makes this so useful is that no matter the size of the die, the FOM is almost constant for a given technology. There are two distinct FOMs:

1) Switching FOM (lower is better): For measuring switching performance ($R_{DS(ON)}$x Q_{GD}) is used as Q_{GD} plays a dominant role in switching loss, and it is impossible to reduce this number without increasing $R_{DS(ON)}$ for a given technology. This is considered a good measure of switching performance.

2) Rectifier FOM (lower is better): This is the traditional MOSFET FOM, and determines rectifier performance in terms of conduction and gate drive power loss ($R_{DS(ON)}$x Q_G). For a 'soft' switching device, where Q_{GD} is not important, you would like to lower $R_{DS(ON)}$ to improve efficiency, but this increases Q_G and thereby increases gate drive losses and overdrive time.

Of these two FOMs, the switching performance is more important in 'hard switching' converter circuits. Figure 2 plots $R_{DS(ON)}$ vs. Q_{GD} for the EPC eGaN power transistors as well as for different equivalent silicon MOSFETs. We can see that, based on switching FOM, the eGaN transistors offer a distinct advantage over any equivalent voltage rated silicon device.

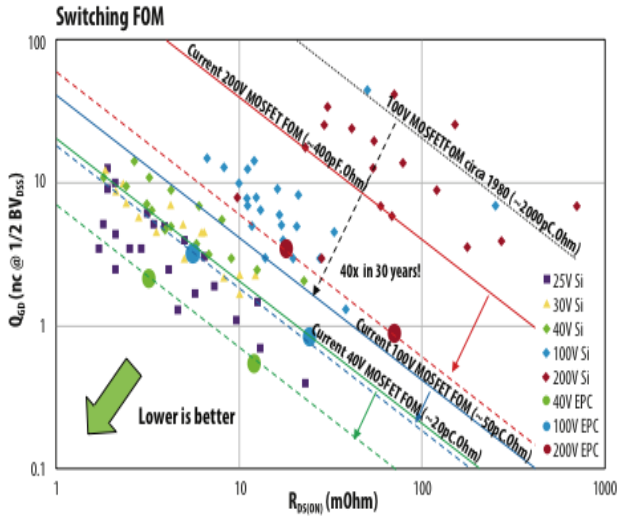

Figure 2: $R_{DS(ON)}$ vs. Q_{GD} for different power transistors

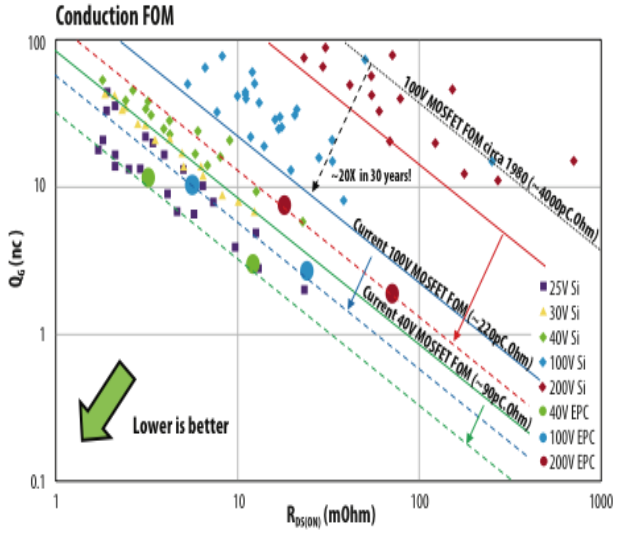

Figure 3: $R_{DS(ON)}$ vs. Q_G for different power transistors

The rectifier FOM is shown in Figure 3 and plots $R_{DS(ON)}$vs. Q_G for the eGaN power transistors as well as for a variety of silicon MOSFETs. From this we can see that the eGaN transistor shows an even stronger improvement over equivalent silicon devices.

Gate Threshold and Maximum Gate Voltage

The threshold of the eGaN transistor is generally lower than that of silicon MOSFETs. This poses less of a limitation to the designer because, (a) there is an almost flat relationship between threshold and temperature, and (b) the very low gate-to-drain capacitance (C_{GD}) makes the devices less sensitive to false turn-on. Figure 4 shows the transfer characteristics curve for the EPC1001, 100V, 7 mΩ transistor. Please note the negative relationship between current and temperature. This allows excellent current sharing in the linear region and in diode conduction. Since the device starts to conduct significant current at 1.6 V, care must be taken to ensure a low-impedance path from gate to source when the device needs to be held off during dV/dt in a rectifier function.

EPC's eGaN devices have a maximum gate voltage of +6V/-5V, which is more than adequate to fully enhance the channel. However, lower gate-to-source voltage limits compared with silicon MOSFETs mean a more accurate gate-drive voltage is required, but this also means total gate-drive losses will be lower.

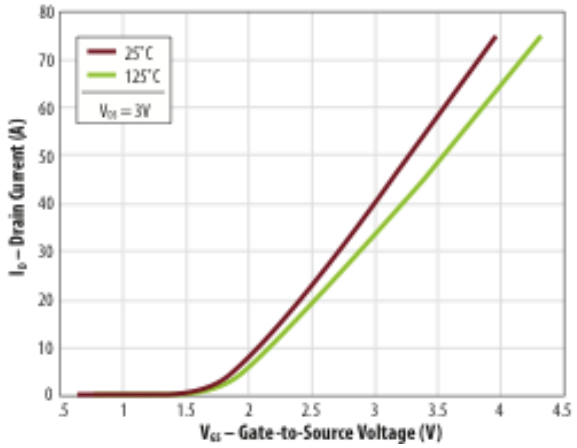

Figure 4: Transfer characteristics curve for the EPC1001, 100-V, 7-mΩ transistor.

Resistance

$R_{DS(ON)}$ versus V_{GS} is also similar to a MOSFET. EPC first-generation eGaN transistors are designed to operate with 5V drive. As there is negligible gate-drive loss penalty, the eGaN transistor should be driven with the full 5V. The temperature coefficient of $R_{DS(ON)}$ for the eGaN transistor is also similar to that of the silicon MOSFET in that it is positive, but the magnitude is significantly less. At 125°C, the $R_{DS(ON)}$ of the 100V eGaN is 1.45 times the 25°C value, compared to 1.7 for silicon.

Capacitance

In addition to the low $R_{DS(ON)}$, the lateral structure of the eGaN transistor makes it a very low-capacitance device. It has the capability of switching hundreds of volts in just a few nanoseconds, enabling multi-megahertz switching. This capability leads to smaller power converters, and higher-fidelity class D audio amplifiers. Most important for switching performance is C_{GD}. An extremely low C_{GD} leads to the eGaN transistor's ability to switch voltage very rapidly.

Capacitance curves for the EPC1001 are shown in Figure 5 [2]. Again, the eGaN transistor looks similar to silicon except that, for a similar on-resistance, the capacitances are significantly lower and "flatten out" much sooner. C_{GS} is large when compared with C_{GD}, but since C_{GD} flattens out to a non-negligible value quickly, this cumulative Q_{GD} change does impact dV/dt immunity with increasing drain-to-source voltage.

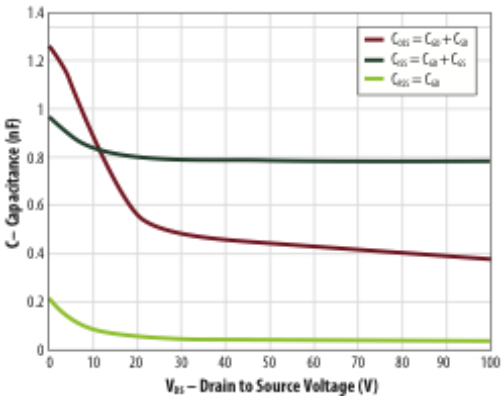

Figure 5: EPC1001 capacitance curves.

In summary, the 40V devices (EPC1014 and EPC1015) have excellent Miller ratios (Q_{GD}/Q_{GS} < 0.6), while the 150V and 200V devices (EPC1010, EPC1011, EPC1012, and EPC1013) have Miller ratios >1.9, and therefore require some careful gate-driver design. Overall, the value of C_{GS} is still small when compared with silicon MOSFETs, enabling very short delay times and excellent controllability in low duty-cycle applications. C_{DS} is also small, being limited to the capacitance across the dielectric from the field plate to the drain.

Series Gate Resistance and Leakage

Series gate resistance (R_G) limits how quickly the capacitance of any transistor can be charged or discharged. Consistent with the high switching-speed capability of the eGaN transistor, EPC transistors have been designed to have gate resistances of a couple tenths of an ohm. This low gate resistance also helps with dV/dt immunity.

The eGaN devices do not use an insulator in the gate. For this reason, the gate leakage current is higher than that of silicon MOSFETs. Designers should expect gate leakage on the order of 1 mA. As these devices have low required gate-drive voltage, losses associated with gate leakage are low and therefore not an issue in most applications.

Body Diode

The last part of the performance picture is that of the so-called "body diode". The eGaN transistor reverse bias or "diode" operation has a different mechanism but similar function. With zero bias from gate to source, there is an absence of electrons in the region under the gate. As the drain voltage is decreased, a positive bias on the gate is created relative to the drift region, injecting electrons under the gate. Once the gate threshold is reached, there will be sufficient electrons under the gate to form a conductive channel. The benefit of this mechanism is that there are no minority carriers involved in conduction, and therefore no reverse-recovery losses.

Although Q_{RR} is zero, the output capacitance (C_{OSS}) still has to be charged and discharged with every switching cycle. For devices of similar $R_{DS(ON)}$, eGaN transistors have significantly lower C_{OSS} than MOSFETs. As it takes a threshold voltage to turn on the eGaN transistor in the reverse direction, the forward voltage of the "diode" is higher than for silicon transistors and therefore care should be taken to minimize diode conduction.

Table 1 summarizes the similarities and differences between a silicon power MOSFET rated at 100V V_{DS} and a similarly rated eGaN transistor.

Table 1: A comparison between silicon and GaN characteristics

	Typical 100V Silicon	**100V eGaN™**
Maximum gate-source voltage	±20 V	+6 V and -5 V
Avalanche capable	Yes	Not rated
Reverse-direction 'diode' voltage	~1 V	~1.5 V to 2.5 V
Body-diode reverse-recovery charge	High	None
Gate-to-source leakage	A few nanoamps	A few milliamps
Gate threshold	2 V to 4 V	0.7 V to 2.5 V
Internal gate resistance	>1 Ω	<0.6 Ω
dV/dt capacitance (Miller) ratio Q_{GD}/Q_{GS}	0.6 to 1.1	1.1
Change in $R_{DS(ON)}$ from 25°C to 125°C	>+70%	<+50%
Change in V_{TH} from 25°C to 125°C	-33%	-3%

The "Ideal" eGaN Transistor Gate Drive

To understand the differences between an eGaN-specific gate drive and a generic MOSFET driver, it is necessary to consider what characteristics an "ideal" eGaN gate drive would have.

Such an ideal gate-drive solution (IC or discrete) is best considered as two separate functions: (1) the gate driver itself, which converts a high-impedance logic input into a low-impedance source to drive each of the power-device gates directly and (2) the level-shifting, delay-matching and other logic circuitry that assures that the input logic is reproduced correctly and with proper timing at the two eGaN transistor gates.

The important gate-driver characteristics are:

- Pull-down resistance as low as 0.5 Ω. With dV/dt slew rates of 20 V/ns to 30 V/ns or more. The risk of Miller turn-on and shoot-through becomes a concern for the higher-voltage devices.
- An accurate gate-drive supply voltage. There is only 1V headroom between the recommended gate-overdrive voltage (5V) and the absolute maximum rating (6V). This accuracy requirement is more difficult to achieve for a bootstrapped supply.
- Adjustable pull-up resistance for EMI and voltage-overshoot control. In half-bridge MOSFET applications, a resistor with an anti-parallel diode is typically used for this purpose. With eGaN transistors, the need for minimizing pull-down resistance means that this resistor and anti-parallel diode connection is not recommended. The simplest general solution is to split the gate pull-up and pull-down connections and allow the insertion of a discrete resistor as needed.
- Low gate-drive loop impedance. At these high switching speeds, the impact of the gate-drive interconnection impedance becomes important, requiring the gate drive to be placed as close as possible to the eGaN power device.

The important level-shifting and delay-matching characteristics are:

- A 5 ns ±2 ns deadtime interval to minimize 'body-diode' conduction losses. As with silicon, the effective deadtime increases with load as turn-on time increases. For higher-voltage devices, this interval is less critical as power levels and the switching period increase.
- A ±2 ns propagation-delay matching. Propagation delays from input to output for both high-side and low-side need to be matched to a much greater accuracy as determined by the deadtime requirement above. This delay matching avoids cross-conduction or shoot-through. The actual delay itself and its variation with temperature are less important.

- A >50-V/ns dV/dt immunity. Switching dV/dt is typically 30 V/ns or higher. Therefore, high dV/dt immunity is required to avoid turning on (or off) both power devices due to the dV/dt glitch.

For non-synchronous or self-driven gate drives, level shifting and delay matching are not relevant.

Discrete Gate-Drive Solutions

Although there are no eGaN-specific gate-drive ICs on the commercial market as of this date, there are a variety of circuits available with adequate drive capability. It is also straightforward to employ a discrete solution.

Considering just the gate-driver element, a simple discrete solution is shown in Figure 6 and works for both ground-referenced (low-side) and floating (high-side) drivers. This solution requires an accurate external ~5.6V supply (depending on the effective forward drop of the bootstrap diode) to supply both high-side and low-side drivers through identical "matching" diodes to achieve the 5.0V gate drive. M2 should be chosen to have 500 mΩ or lower $R_{DS(ON)}$, while R2 can adjust the effective pull-up resistance (to control voltage overshoot and EMI ringing) without impacting the pull-down impedance. During layout, the loop between the eGaN transistors and the discrete (or IC) gate drive should be minimized.

Discrete MOSFETs M1 and M3 should be scaled so they can be driven with a higher impedance (logic-level input) source while still being able to drive M2 and M4. Resistor R1 is added to limit cross conduction between M1 and M3 and eliminate cross conduction in M2 and M4. For applications with only ground-referenced eGaN devices, the diode can be removed and an accurate 5.0V supply can be used to directly power the discrete driver.

In addition to this discrete circuit being compatible with all 5V logic control ICs, it can also be combined with higher logic voltage ICs where no 5V logic versions exist (e.g. level shifters above 100V). Figure 7 shows an example of adding a 5.0V regulator between the level-shifting/gate-drive IC and the discrete-driver solution. By placing the regulator before the discrete MOSFETs, the pre-drive MOSFETs (M1 and M3 in Figure 7) provide logic translation from the higher voltage to 5 V. This also lengthens the gate pulse by only speeding up the gate turn-on, which can be advantageous when the deadtime is already too large.

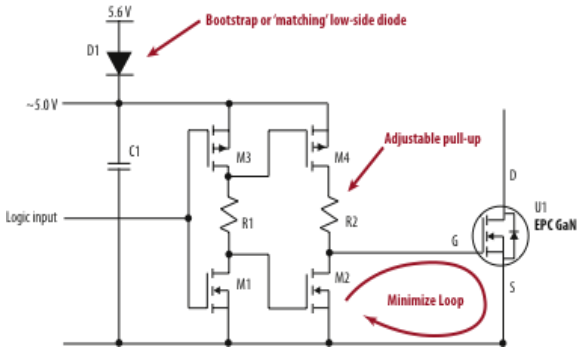

Figure 6: Discrete eGaN gate-driver solution.

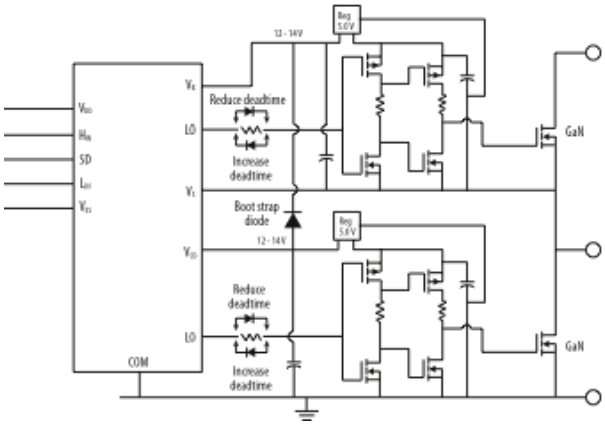

Figure 7: Discrete gate-drive solution paired with higher logic voltage level-shift IC.

Gate-Driver ICs

There are also a number of commercially available gate-driver ICs that are adequate for driving eGaN transistors. As low pull-down impedance is required, these ICs tend to be single gate-drive buffer ICs with very high-current drive capability. Please note that for the 40V EPC devices (EPC1014 and EPC1015), this pull-down resistance requirement can be relaxed due to the favorable Miller ratio.

A partial list of these gate-drivers is given in Table 2. It should be noted that some may not meet the 0.5Ω pull-down requirement, which may not be necessary, depending on the actual dV/dt and the eGaN device used.

Table 2: Gate-drive ICs suitable for eGaN Transistors

Manufacturer	Part number	Typical pull-down resistance
Fairchild	FAN3121/22	>9A[a]
	FAN3123/24	>4A[a]
Intersil	EL7158	0.5 Ω[b]
IXYS	IXDE509	0.7 Ω
Maxim	MAX5048	<0.5 Ω
	MAX15024	0.5 Ω
National	LM5110/12	1.4 Ω[c]
Micrel	MIC4421/2	0.8 Ω
	MIC4451/2	0.8 Ω
Microchip	TC4421/2A	0.8 Ω
	TC4451/2	0.9 Ω
Texas Instruments	UCC27321/2	1.1 Ω
	TPS28225/6	>1 Ω

Notes:
a Resistance not given
b Used on EPC9001/2 development boards
c Negative pull-down supply possible on LM5112

Level Shifters and Logic Circuitry

Whether a discrete or IC solution is used to drive eGaN transistors, the requirement for minimizing deadtime and controlling propagation delay is still a concern. In general, MOSFET-friendly level-shifter ICs have at least 20ns deadtime, and this value tends to increase with the level-shifter voltage rating. As these ICs have some drive capability, a simple RCD circuit (see Figure 8) can be placed on the output to slow down turn-off and decrease deadtime. Care should be taken not to reduce the deadtime so much as to cause cross conduction considering the variation in deadtime of the driver from part-to-part or over temperature can be significant. Such modifications will also affect maximum and minimum pulse widths.

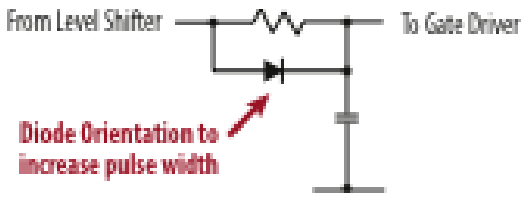

Figure 8: Simple RCD circuit to adjust gate-drive pulse width.

Apart from level-shifter ICs, the transfer of gate-pulse information across a high dV/dt barrier can also be achieved through a pulse transformer, optocoupler or by other means (e.g. iCoupler [3]) and these may be realistic options for higher-voltage and higher-power applications.

Switching Results

An experiment was conducted in which the generalized discrete gate-drive circuit from Figure 5 was used to drive a half-bridge consisting of two 200V, 25 mΩ EPC1010 devices. The detailed schematic for this circuit is shown in Figure 9 and the resulting waveforms are shown in Fig. 10. These are the waveforms for a 100V-to-10V, 7A buck circuit operating at 400 kHz. Diode conduction can clearly be seen, while the turn-on time is less than 3 ns and dV/dt slew rates are as high as 40 V/ns.

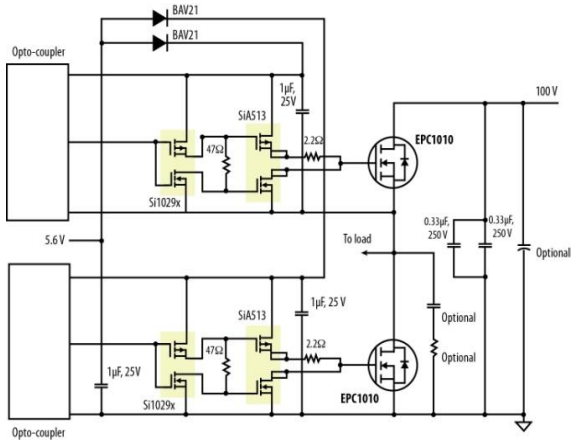

Figure 9. Schematic of discrete gate-drive circuit.

Figure 10: EPC1010 switching 100 V and 7 A using a discrete gate-drive solution. Ch1: low-side G-S voltage (2 V/div), CH2: inductor current (2 A/div), Ch4: low-side D-S (switch-node) voltage (20 V/div). Time scale: 50 ns/div.

Suggested eGaN-Friendly Gate Driver ICs

Given the information on eGaN transistor drive requirements above, it should be possible to define an eGaN driver IC that will meet these requirements. At first, to leverage the existing MOSFET controller and level-shifter infrastructure, a simple eGaN driver interface IC is suggested. This part is defined to interface between controller and eGaN switch as shown in Figure 11. The same part could also be used for synchronous rectification and single switch isolated topologies (such as flyback and forward). These would also be suited for digital controllers where the gate drive function would normally be external to the controller. The suggested device pin-out and pin descriptions are given in Figure 12 and Table 3 respectively.

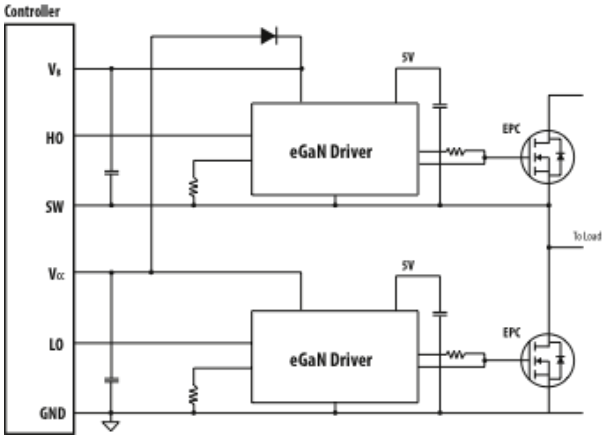

Figure 11: Partial schematic of a half bridge converter showing controller, eGaN driver and eGaN devices

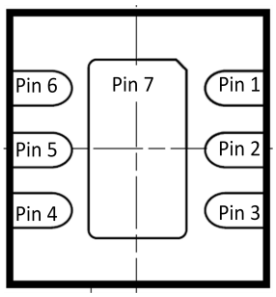

Figure 12: eGaN friendly interface gate driver in 6-pin DFN package (bottom view)

Conclusions

EPC's eGaN transistors give the design engineer a whole new spectrum of performance compared with silicon power MOSFETs. In order to extract full advantage from this new, game-changing technology, designers must understand how to apply the type of simple and cost-effective drive circuitry that has been demonstrated here. Eventually, semiconductor suppliers will develop driver ICs specifically optimized for eGaN technology using specifications like those presented above for the "ideal" drive IC. When such gate-driver chips become commercially available, the task of transitioning from silicon to eGaN technology will become even more simple and cost effective.

Table 3: eGaN driver pin descriptions

Pin #	Name	Description	Requirements
1	VCC	Input supply voltage	6-15V operational
2	Input	Logic input	Hysteretic input threshold, possibly function of VCC voltage
3	Delay	Lengthens or shortens input pulse. Pull up resistor to 5V sets sink current to shorten pulse (leading edge). Alternatively a pull down resistor sets source current to lengthen trailing edge	Adjustable to +/- 100ns should be adequate.
4	OL	Gate drive pull-down. Connects directly to eGaN gate	MOSFET pull-down with ~0.5 Ohm $R_{DS(ON)}$ @ 5V)
5	OH	Gate drive pull-up Resistor between OH and OL sets pull-up speed. Can be combined with pin 4 for some applications.	MOSFET pull-up with ~2 Ohm $R_{DS(ON)}$@ 5V)
6	5V	Regulated output for gate drive. LDO from VCC pin. Can tie VCC to 5V if external 5V supply is available.	Generate 5V output for pull up
7	GND	Ground reference and gate drive return	Exposed pad for improved thermal performance

References:

1. B. J. Baliga, Power Semiconductor Devices, 1996, PWS Publishing Company, p. 373

2. http://epc-co.com/epc/documents/datasheets/EPC1001_datasheet_final.pdf

3. http://www.analog.com/en/interface/digital-isolators/products/CU_over_iCoupler_Digital_Isolation/fca.html