EPC2121 – Bidirectional eGaN® Power Switch

V_{DD}, 100 V

$R_{DD(on)}$, 50 mΩ typ

I_D, 2.5 A

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DD}	Drain-to-Drain Voltage (Continuous)	100	V
	Drain-to-Drain Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous (T_A = 25 °C)	2.5	A
	Pulsed (25 °C, T_{PULSE} = 300 µs)	18	
V_{GD}	Gate-to-Drain Voltage	6	V
	Gate-to-Drain Voltage	-100	
V_{GS}	Gate-to-Source Voltage	6	
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	4.8	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	18	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DDS}	Drain-to-Drain Voltage	$V_{GD1(D2)S}$ = 0 V, $I_{D1(D2)S}$ = 10 µA, source tied to one drain terminal	100			V
I_{DDS}	Drain-Drain Leakage	$V_{D1(D2)S}$ = 80 V, $V_{GD1(D2)}$ = 0 V, source tied to one drain terminal		0.1	10	µA
I_{GD}	Gate-to-Drain Forward Leakage	$V_{GD1(D2)}$ = 5 V, source tied to one drain terminal		0.8	200	
	Gate-to-Drain Reverse Leakage	$V_{GD1(D2)}$ = -80 V, source tied to one drain terminal		0.1	7	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{D1(D2)S}$ = V_{GS}, $I_{D1(D2)}$ = 0.7 mA, source tied to one drain terminal	0.8	1.2	2.5	V
$R_{DD(on)}$	Drain-Drain On Resistance	V_{GS} = 5 V, I_D = 1 A		50	78	mΩ

Die size: 0.9 x 0.9 mm

EPC2121 eGaN® FETs are supplied in passivated die form with solder bumps.

Applications

- Solid-state relay in a thermostat
- USB PD 3.1 port protection
- Battery and reverse battery protection
- Bidirectional blocking load switch
- RF switch

Benefits

- Bidirectional blocking
- Ultra Small Footprint, 90% smaller than MOSFET alternative
- Lower On-Resistance, 50% lower than two MOSFETs in common source configuration

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2121

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DD} = 50 V, V_{GS} = 0 V, Source tied to one drain terminal		137	218	pF
C_{RSS}	Reverse Transfer Capacitance			1		
C_{OSS}	Output Capacitance			54	63	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DD} = 0 to 50 V, V_{GS} = 0 V, Source tied to one drain terminal		63		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			83		
R_G	Gate Resistance			5.9		
Q_G	Total Gate Charge	V_{DD}= 50 V, V_{GS} = 5 V, I_D = 1 A, Source tied to one drain terminal		1.1	1.6	nC
Q_{GS}	Gate-to-Source Charge	V_{DD} = 50 V, I_D = 1 A, Source tied to one drain terminal		0.28		
Q_{GD}	Gate-to-Drain Charge			0.16		
$Q_{G(TH)}$	Gate Charge at Threshold			0.21		
Q_{OSS}	Output Charge	V_{DD} = 50 V, V_{GS} = 0 V, Source tied to one drain terminal		4.2	5	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V_{DSS}.

Figure 1: Typical Output Characteristics at 25°C*

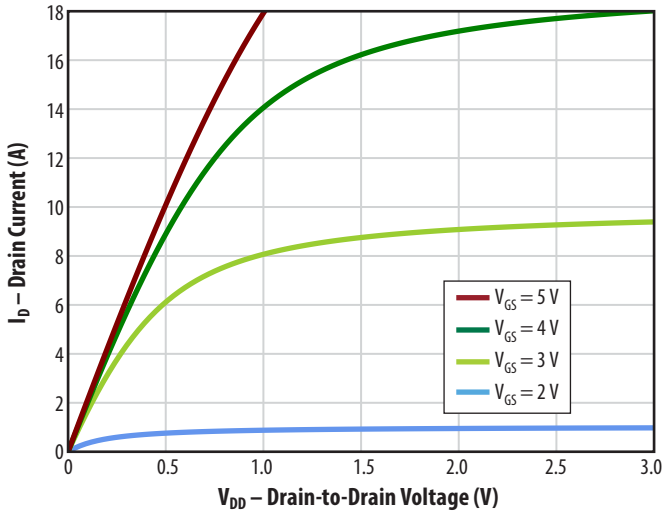


Figure 2: Typical Transfer Characteristics*

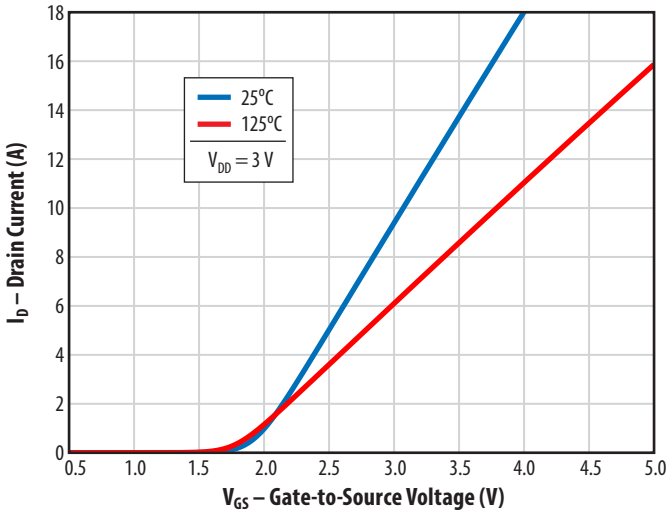


Figure 3: Typical $R_{DD(on)}$ vs. V_{GS} for Various Currents*

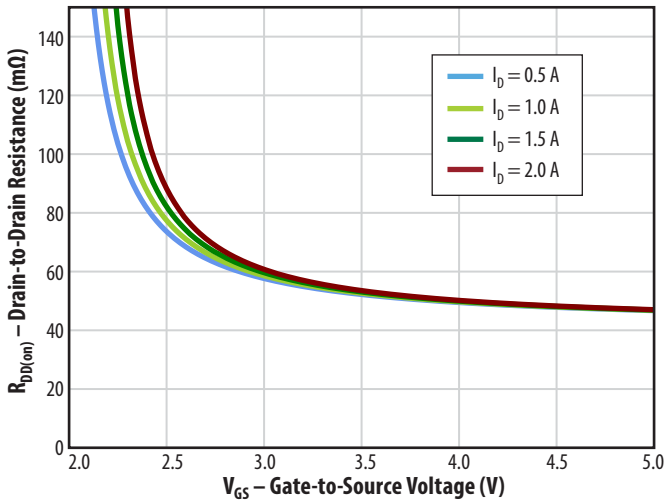
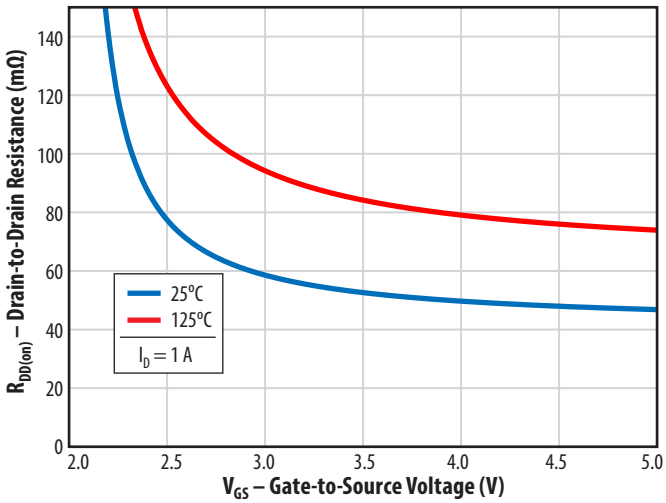


Figure 4: Typical $R_{DD(on)}$ vs. V_{GS} for Various Temperatures*



* Source tied to one drain terminal; drains are symmetrical. See Figure 13.

Figure 5a: Typical Capacitance (Linear Scale)*

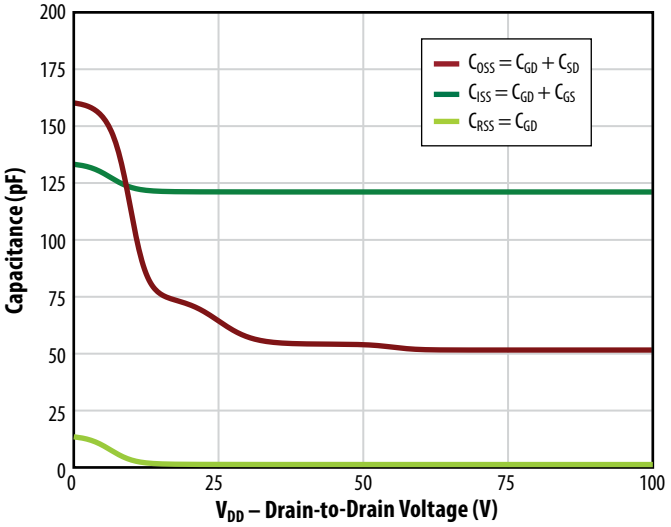


Figure 5b: Typical Capacitance (Log Scale)*

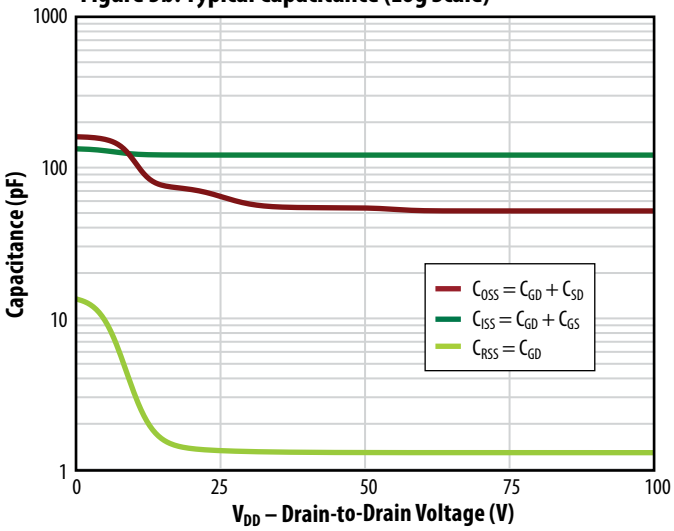


Figure 6: Typical Output Charge and C_{OSS} Stored Energy*

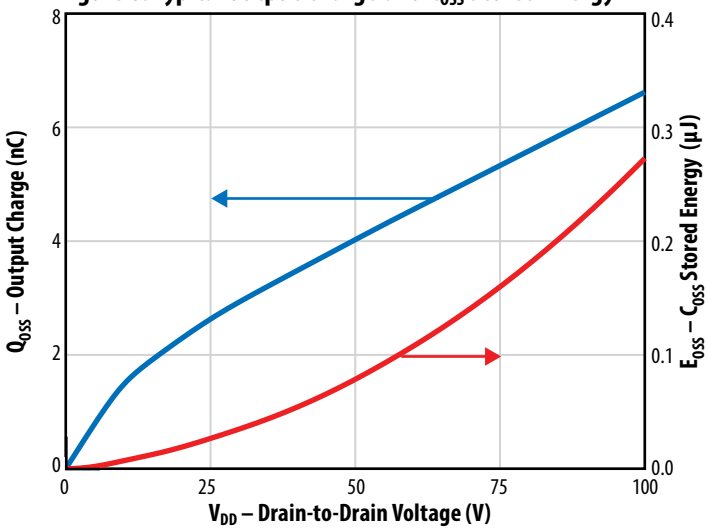


Figure 7: Typical Gate Charge*

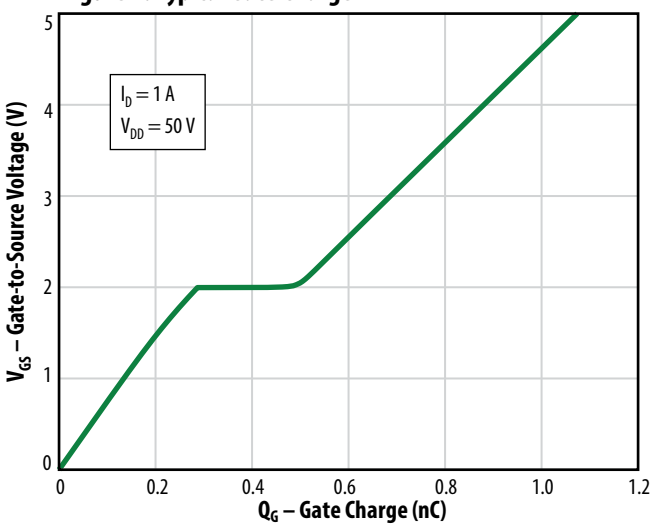
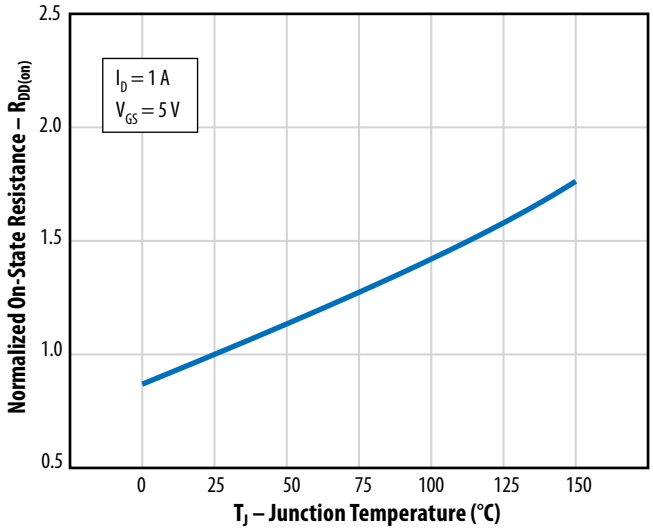


Figure 8: Normalized On-State Resistance vs. Temperature*



* Source tied to one drain terminal; drains are symmetrical. See Figure 13.

Figure 9: Normalized Threshold Voltage vs. Temperature*

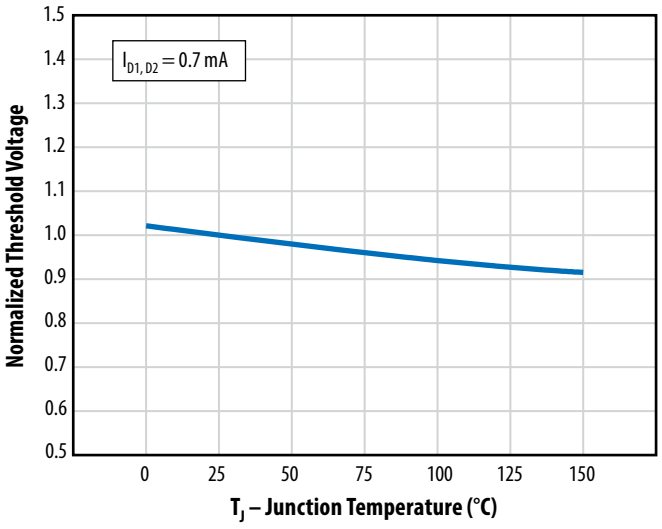
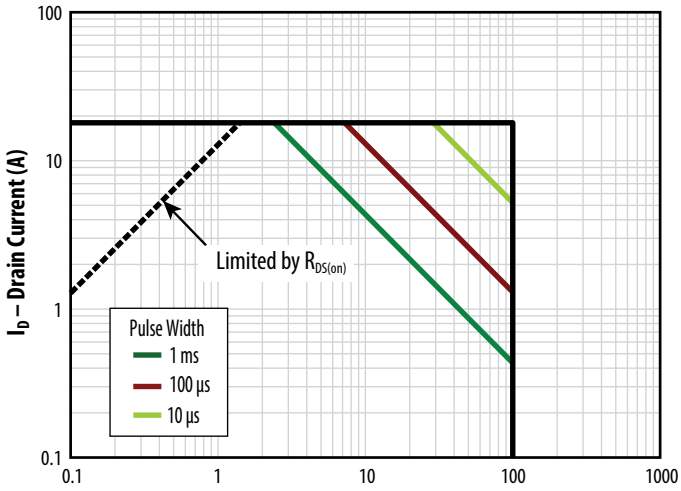


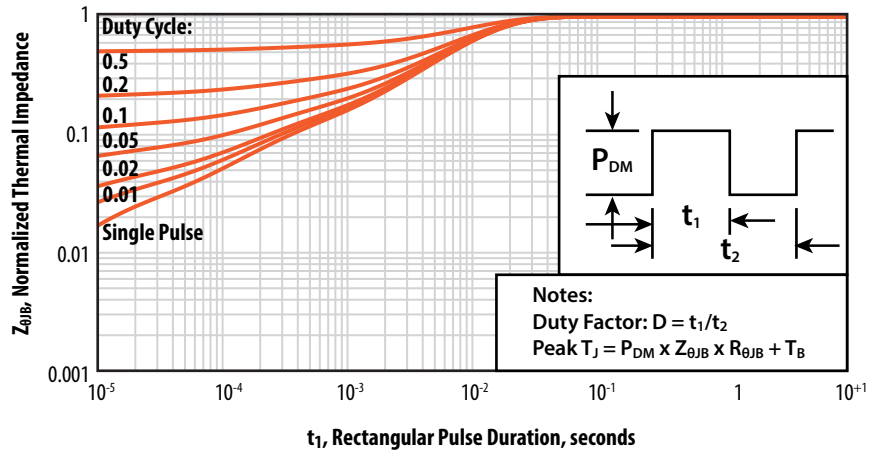
Figure 10: Safe Operating Area*



T_J = Max Rated, T_C = 25°C, Single Pulse

Figure 11: Typical Transient Thermal Response Curves

Junction-to-Board



Junction-to-Case

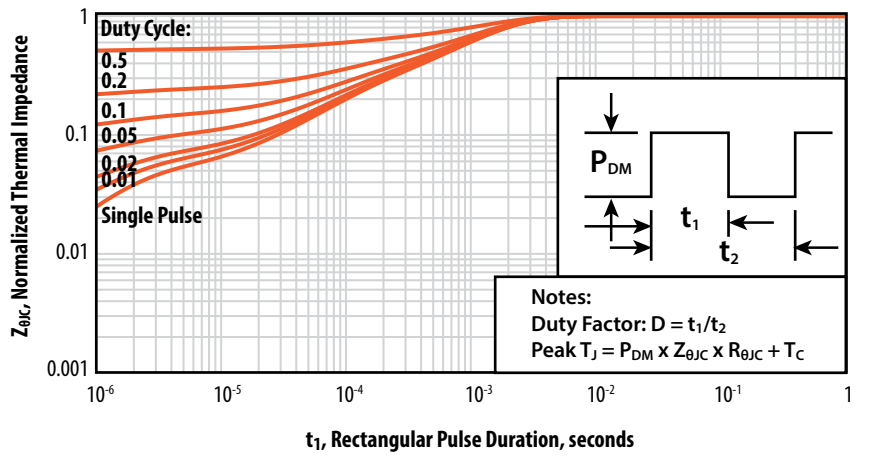


Figure 12: Application configuration

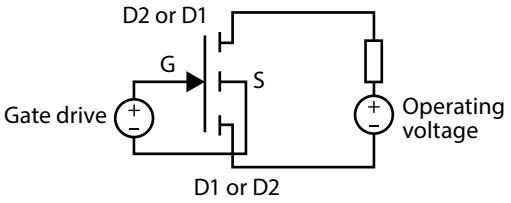
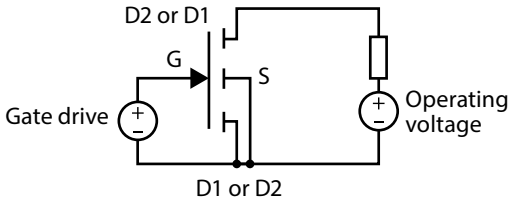


Figure 13: Test circuit



TYPICAL THERMAL CONCEPT

The EPC2121 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

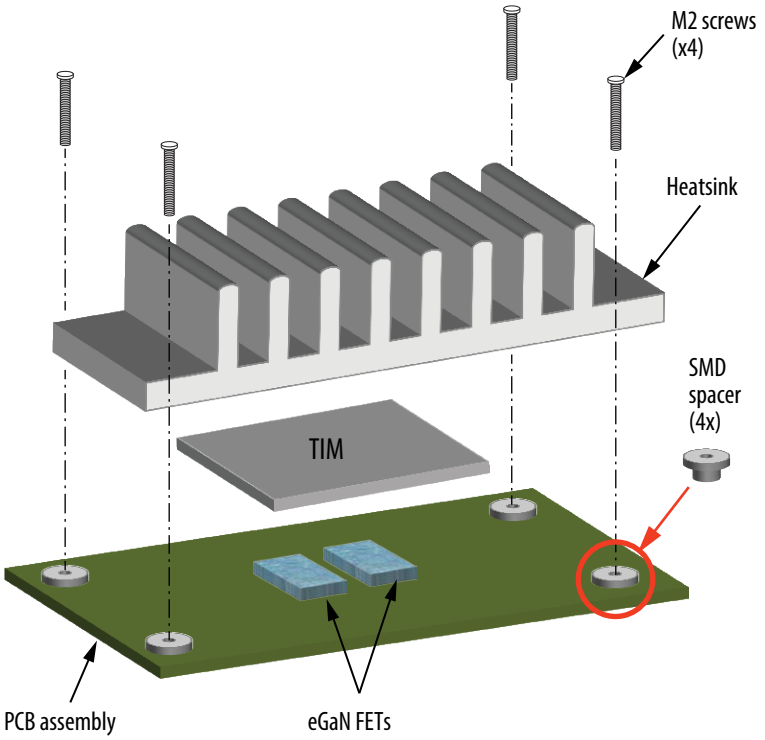


Figure 14: Exploded view of heatsink assembly using screws

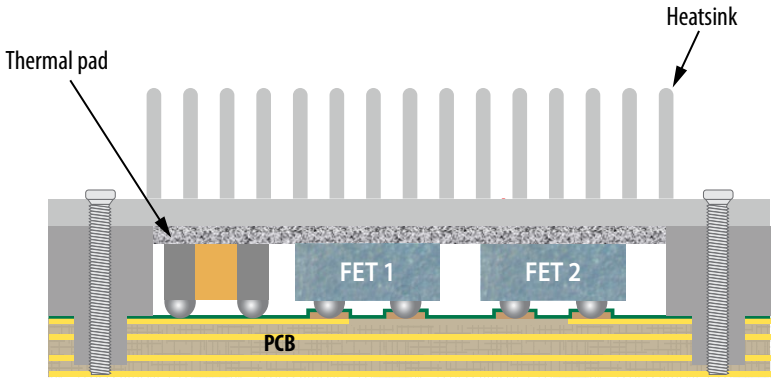


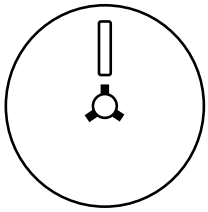
Figure 15: A cross-section image of dual sided thermal solution

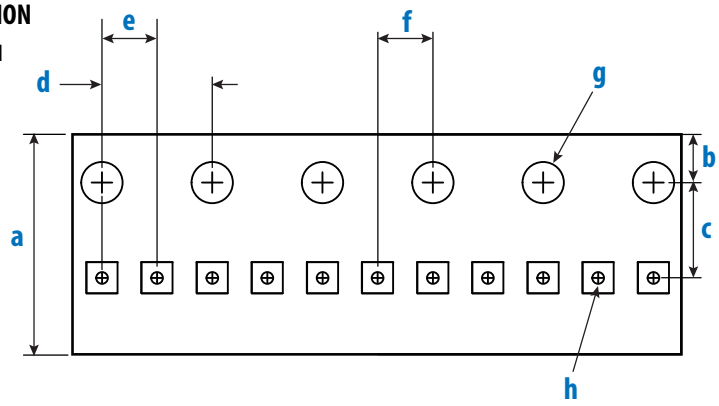
Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

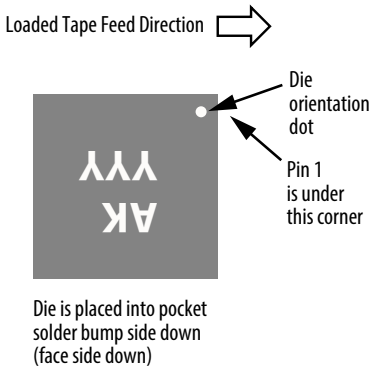
The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

TAPE AND REEL CONFIGURATION

2 mm pitch, 8 mm wide tape on 7" reel





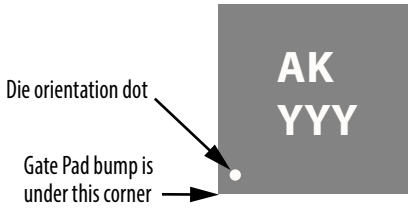


	Dimension (mm)		
EPC2121 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	2.00	1.95	2.05
f (Note 2)	2.00	1.95	2.05
g	1.50		1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

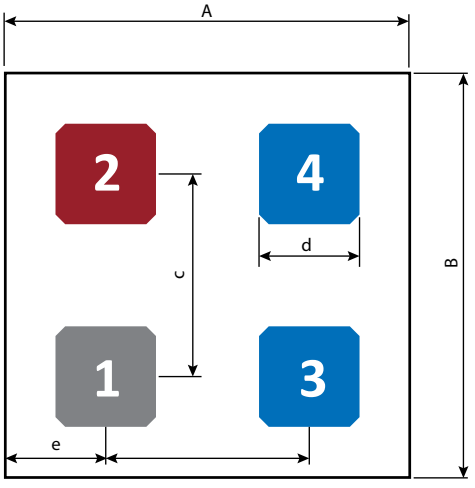
DIE MARKINGS



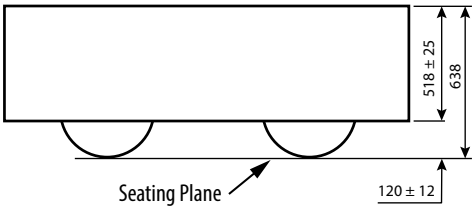
Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2121	AK	YYY

DIE OUTLINE

Solder Bump View



Side View



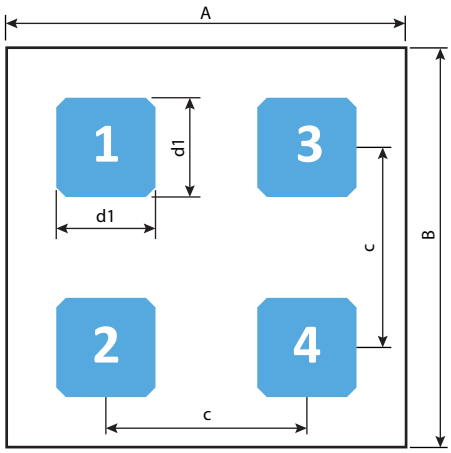
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	870	900	930
B	870	900	930
c		450	
d	205	225	245
e		225	

Pad 1 is Gate;
Pad 2 is Source;
Pad 3 is Drain 1;
Pad 4 is Drain 2

Note: Drain 1 and Drain 2 are interchangeable

RECOMMENDED LAND PATTERN

(units in µm)



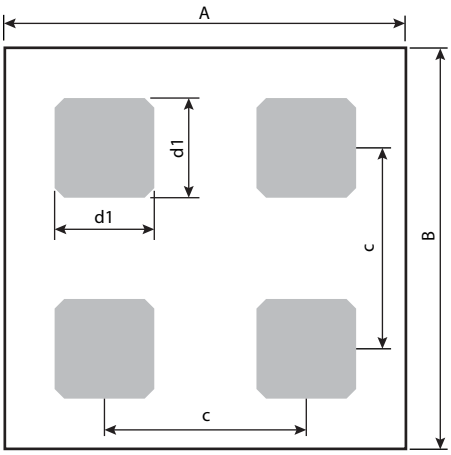
Land pattern is solder mask defined

DIM	MICROMETERS
A	900
B	900
c	450
d1	205

Pad 1 is Gate;
Pad 2 is Source;
Pad 3 is Drain 1;
Pad 4 is Drain 2

RECOMMENDED STENCIL DRAWING

(measurements in µm)



DIM	MICROMETERS
A	900
B	900
c	450
d1	205

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, opening per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional resources available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)