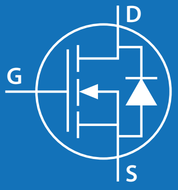
EPC2307 – Enhancement Mode Power Transistor

V_{DS} , 200 V
$R_{DS(on)}$, 10 mΩ max



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised March 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
	Drain-to-Source Voltage (Repetitive Transient) (1)	220	
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	240	
I_D	Continuous ($T_A \leq$ 125°C)	62	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	130	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 175	

(1) Pulsed repetitively, duty cycle factor (DCFactor) ≤ 1%; See Figure 13 and Reliability Report Phase 16, Section 3.2.6"

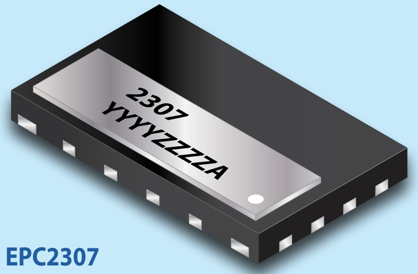
Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.5	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	3.0	
$R_{θJA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	54	
$R_{θJA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90150 EVB)	23	

Static Characteristics (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.25 mA	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 160 V		0.003	0.25	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.0015	0.6	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.15	1.3	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.02	0.8	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4 mA	0.8	1.5	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 15 A		7.2	10	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.



EPC2307
Package size: 3 x 5 mm

Applications

- Synchronous Rectification
- AC/DC chargers, SMPS, adaptors
- High Frequency DC-DC Conversion
- Class D audio
- Wireless Power
- High power lidar & dToF

Benefits

- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint – Higher power density
- Moisture rating MSL1

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2307

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		1298	1682	pF
C_{RSS}	Reverse Transfer Capacitance			2.8		
C_{OSS}	Output Capacitance			343	505	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 100 V, V_{GS} = 0 V		435		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			579		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 5 V, I_D = 15 A		10.1	12.6	nC
Q_{GS}	Gate to Source Charge	V_{DS} = 100 V, I_D = 15 A		3.5		
Q_{GD}	Gate-to-Drain Charge			1.2		
$Q_{G(TH)}$	Gate Charge at Threshold			2.5		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		58	72	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

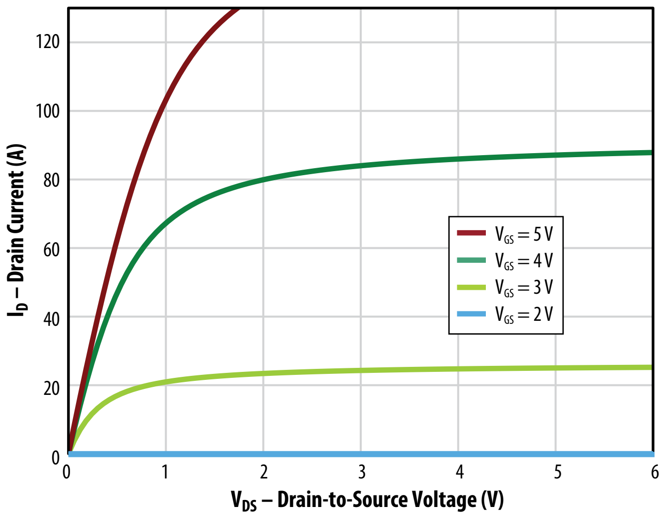


Figure 2: Typical Transfer Characteristics

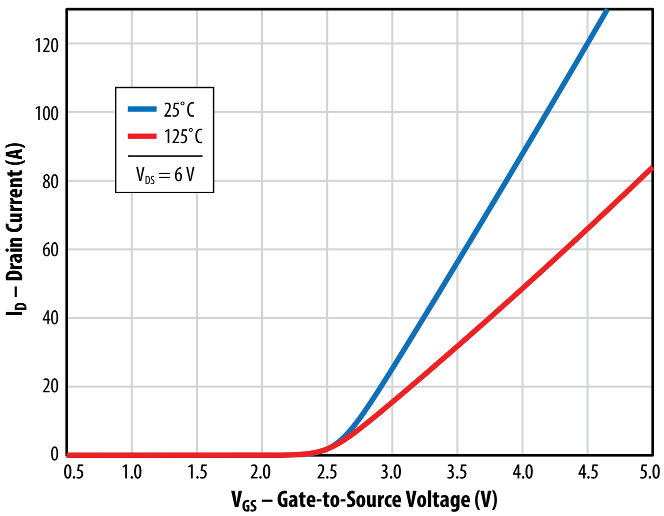


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

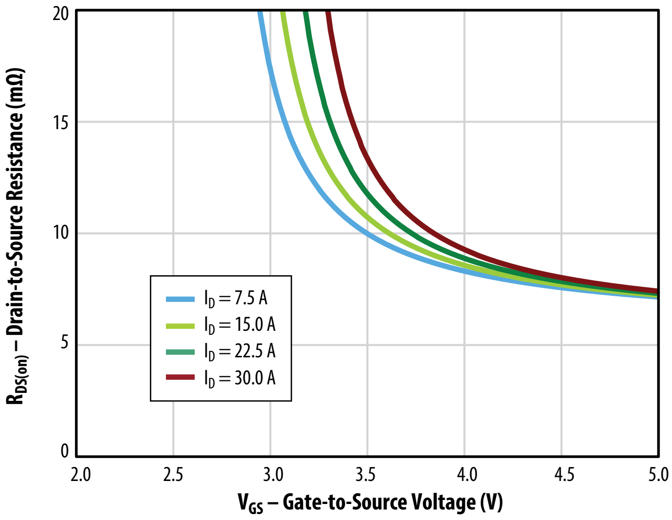


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

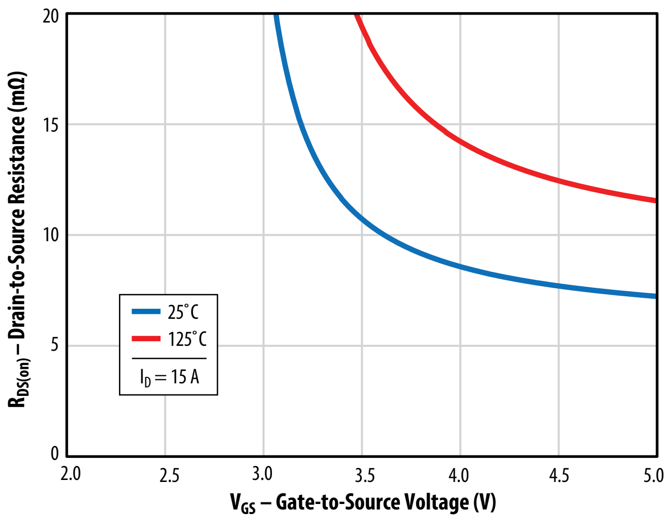


Figure 5a: Typical Capacitance (Linear Scale)

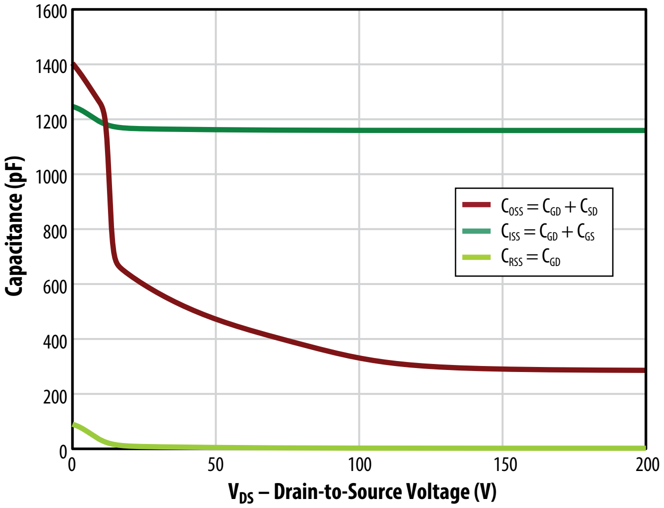


Figure 5b: Typical Capacitance (Log Scale)

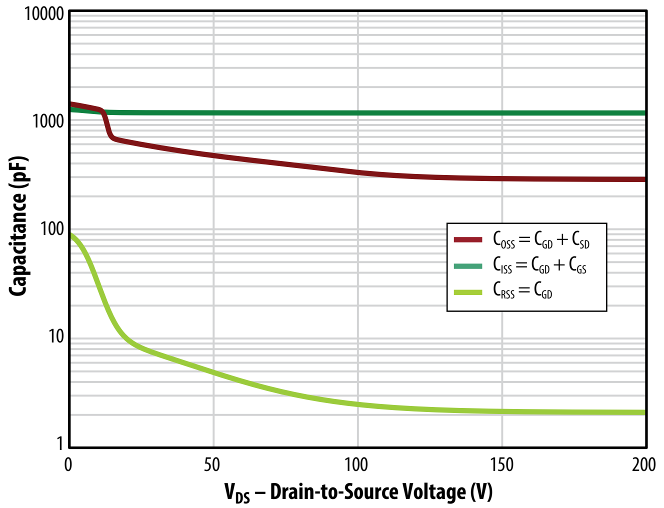


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

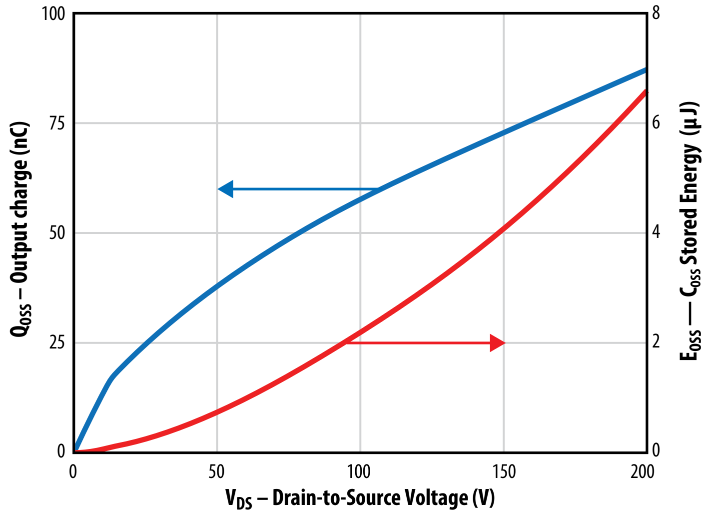


Figure 7: Typical Gate Charge

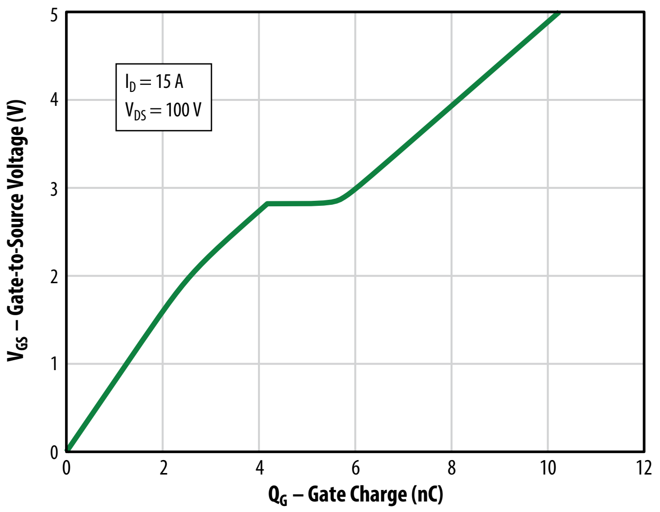
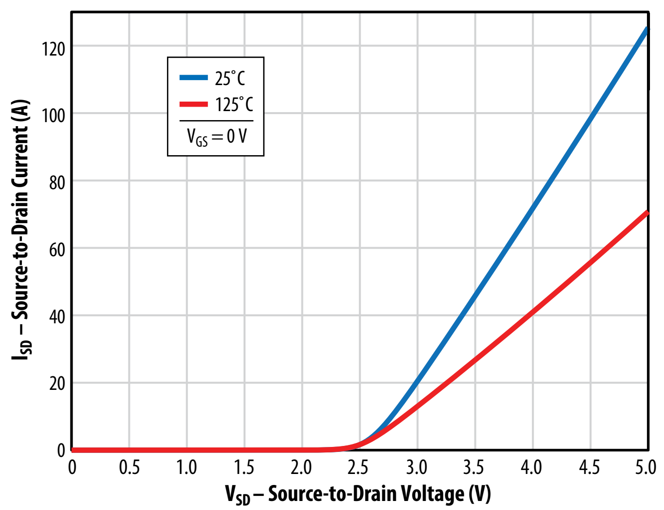


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

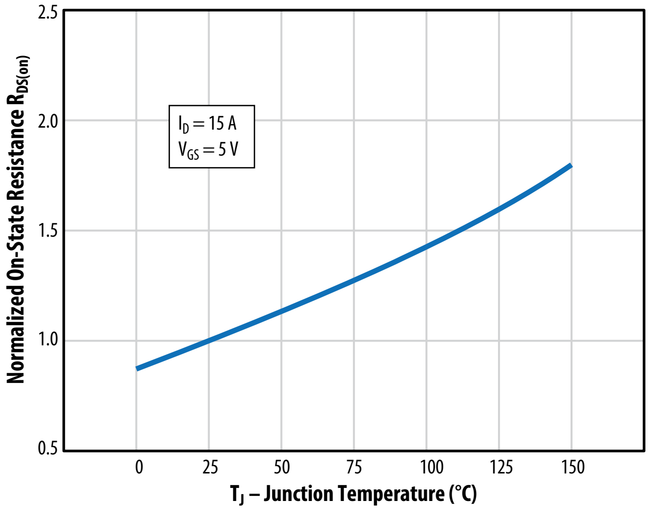


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

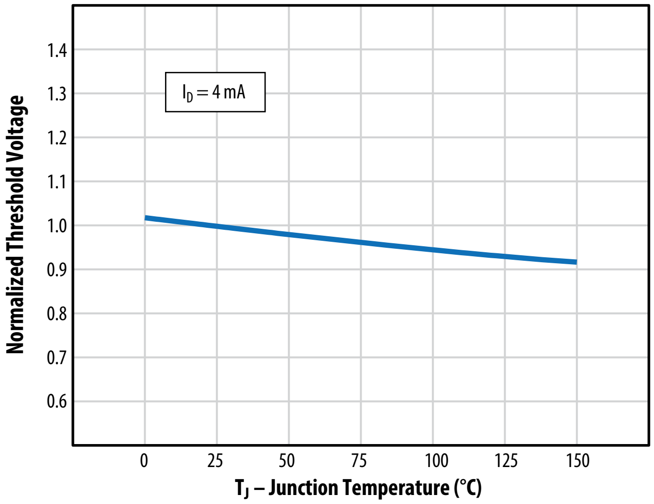


Figure 11: Safe Operating Area

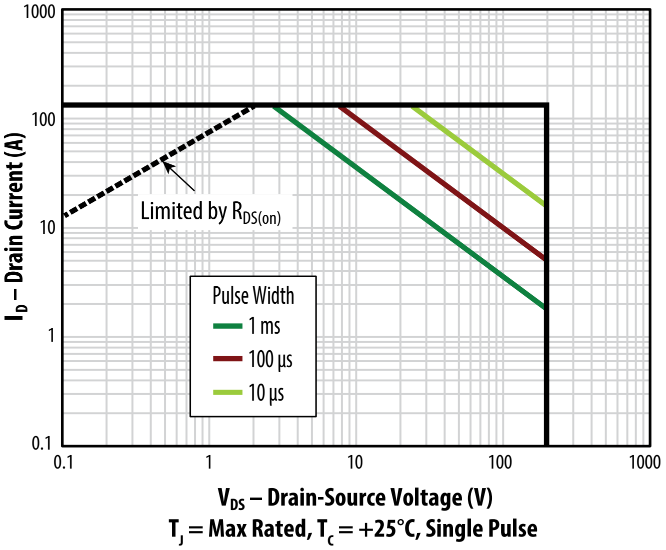
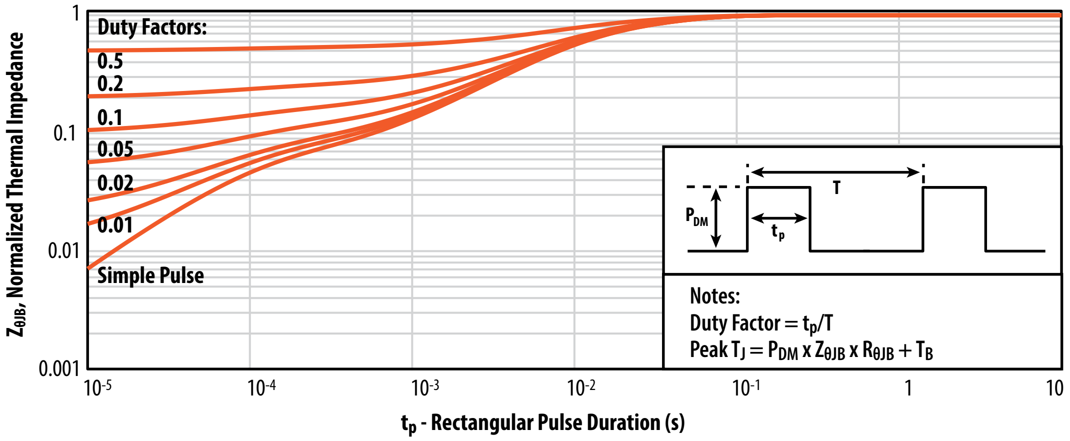


Figure 12: Transient Thermal Response Curves

Junction-to-Board



Junction-to-Case

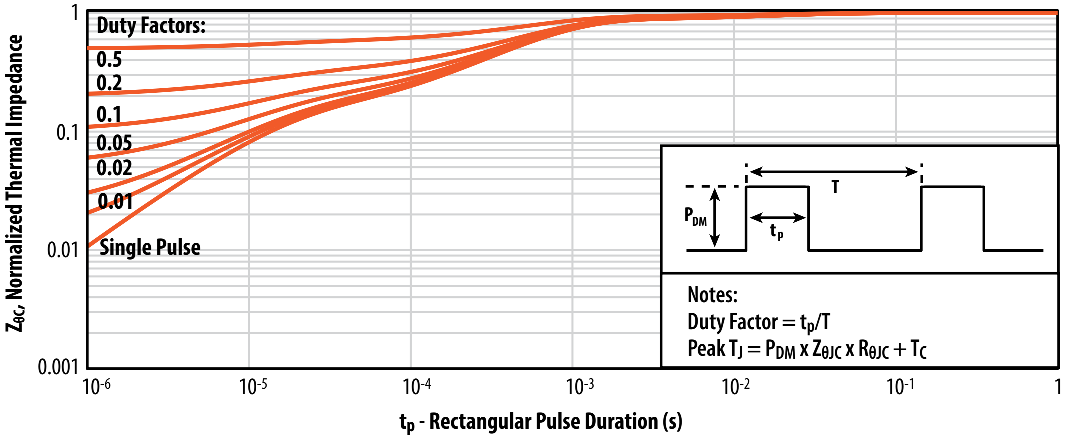
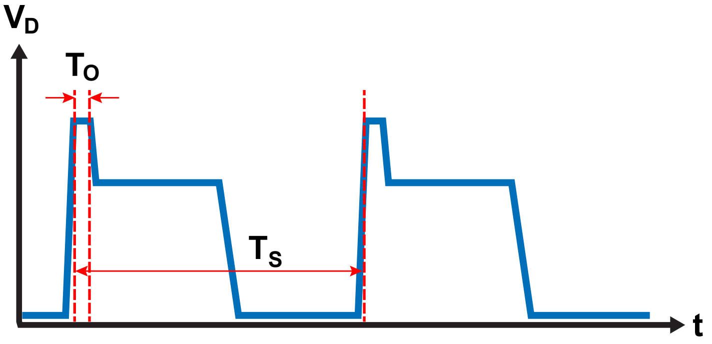


Figure 13: Duty Cycle Factor (DC_{Factor}) Illustration for Repetitive Overvoltage Specification



1% is the ratio between T_O (overvoltage duration) and T_S (one switching period)

LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the first inner layer used as a reference for the gate loop under the gate resistors and the relative pins of the gate driver: ground for the bottom FET and switch node for the top FET.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The **EPC90150 Half-Bridge Development Board Using EPC2307** implements our recommended vertical inner layout.

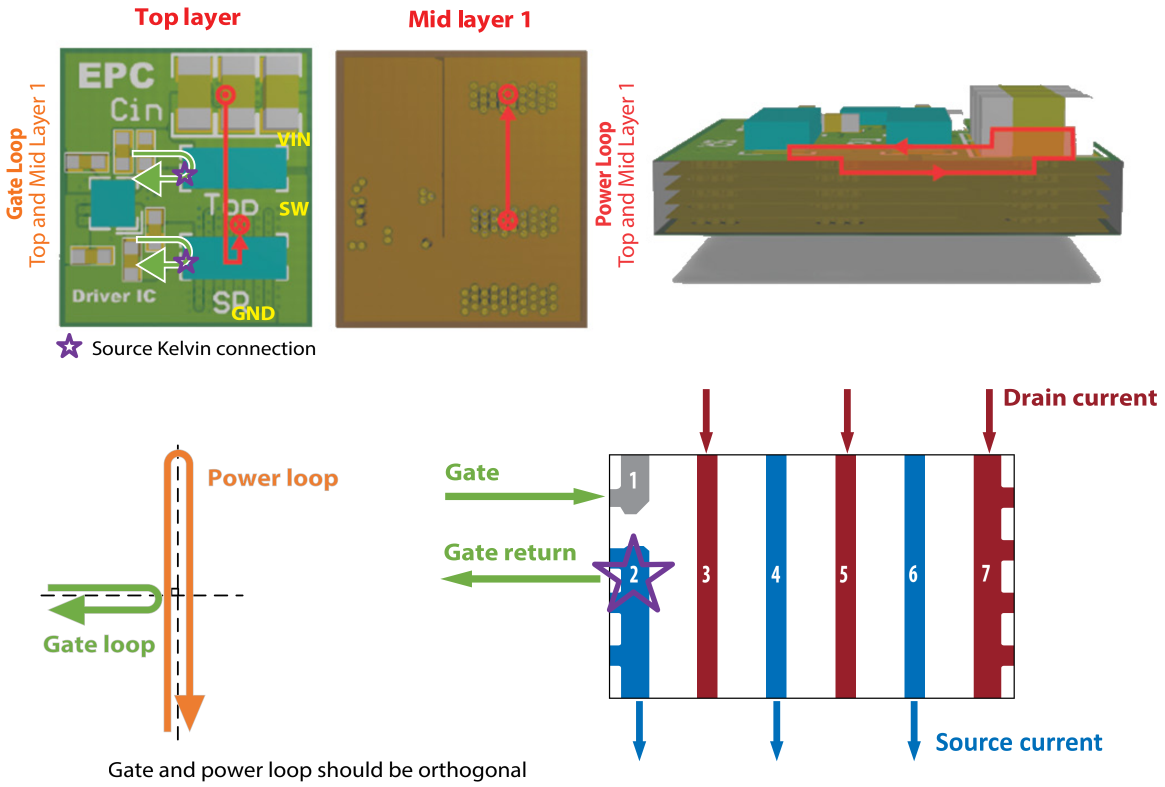


Figure 14: Inner Vertical Layout for Power and Gate Loops

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**

TYPICAL SWITCHING BEHAVIOR

The following typical switching waveforms are captured in these conditions:

- **EPC90150 Half-Bridge Development Board Featuring EPC2307**
- Gate driver: NCP51820 with 1A source and 2 A sink capability
- External $R_G(ON) = 1\ \Omega$, $R_G(OFF) = 0\ \Omega$
- $V_{IN} = 150\ V$, $I_L = 30\ A$

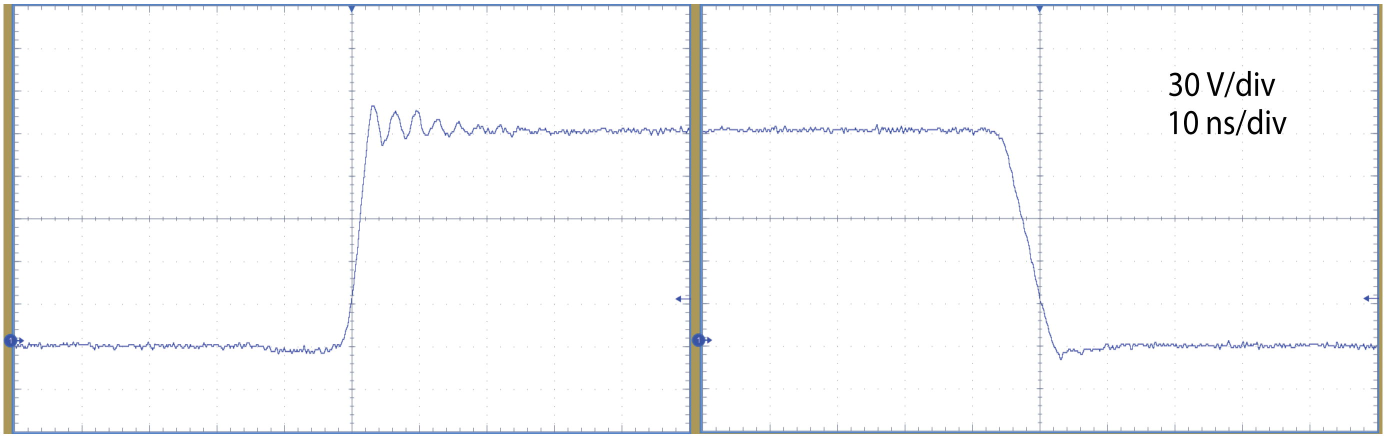


Figure 15: Typical half-bridge voltage switching waveforms

TYPICAL THERMAL CONCEPT

The EPC2307 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in
How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf.

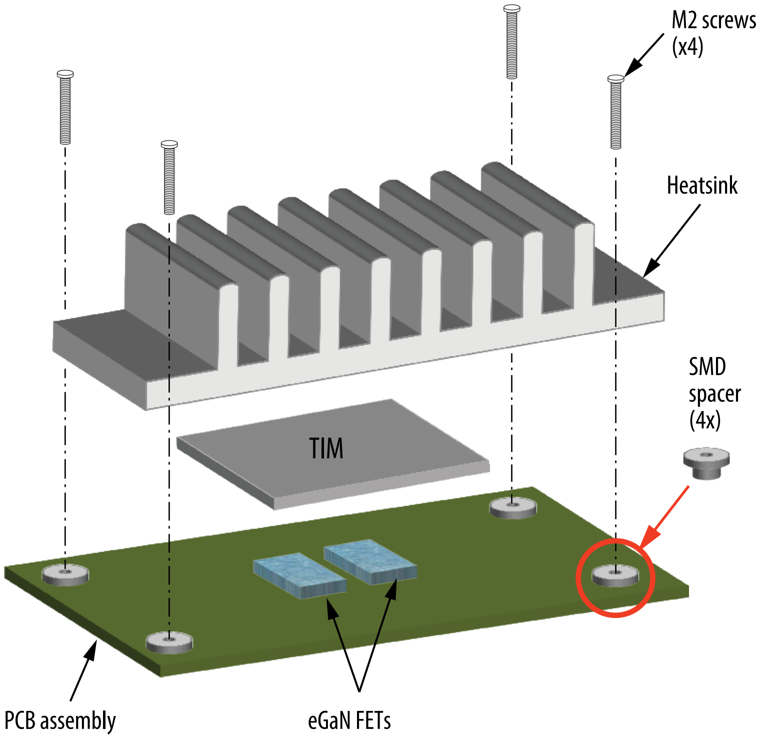


Figure 16: Exploded view of heatsink assembly using screws

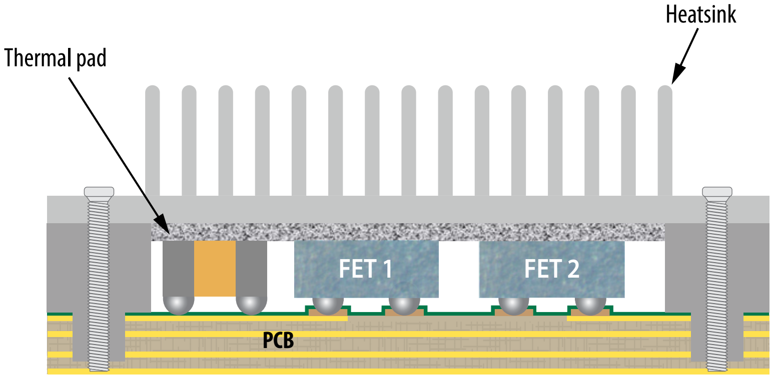


Figure 17: A cross-section image of dual sided thermal solution

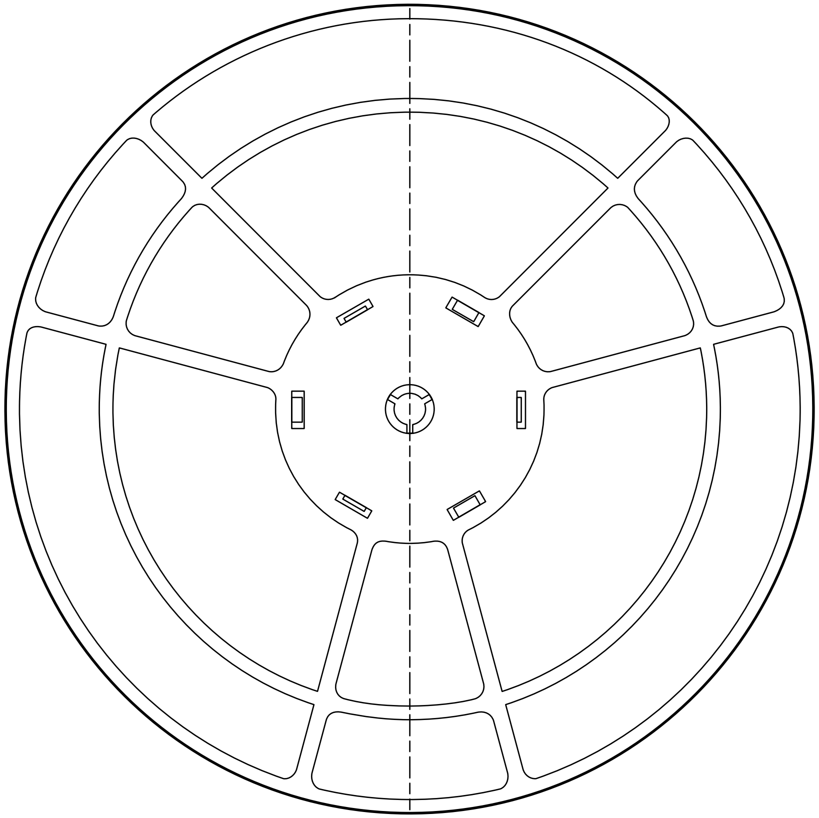
Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

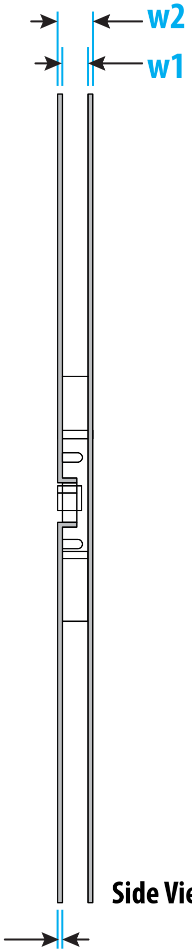
The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

TAPE AND REEL

(units in mm)

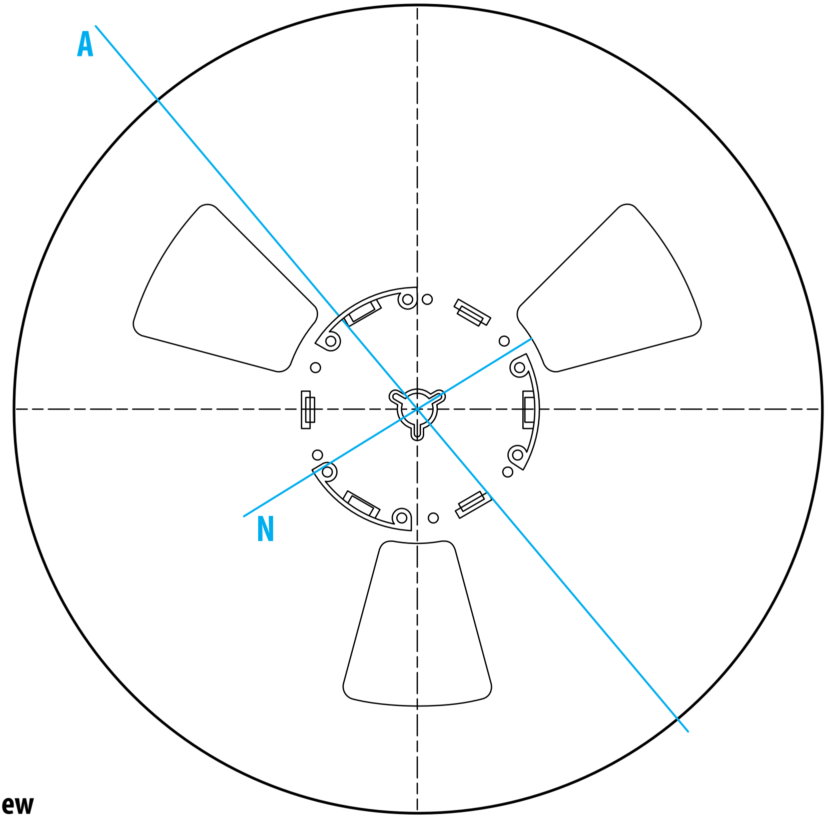
Top View

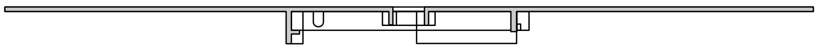




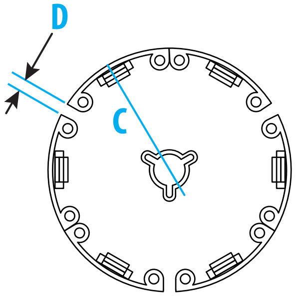
Side View

Bottom View

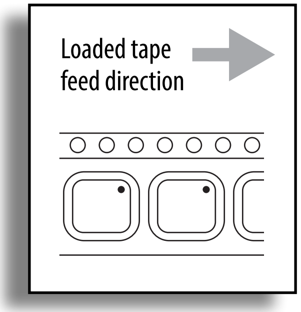




Top View Detail

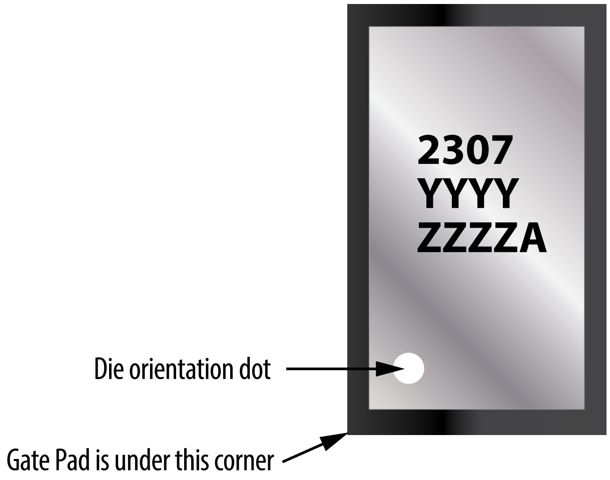


Bottom View Detail

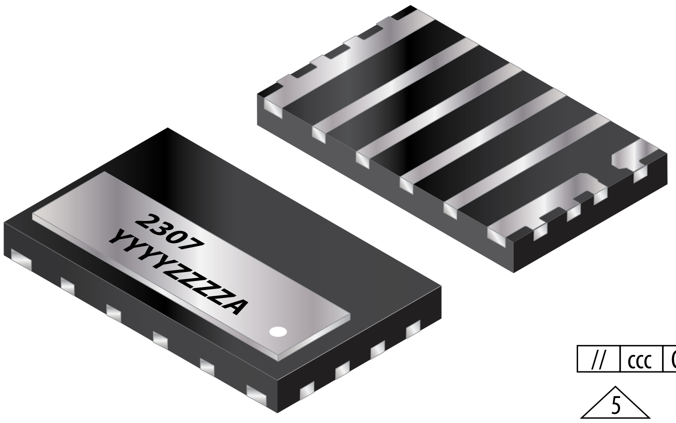


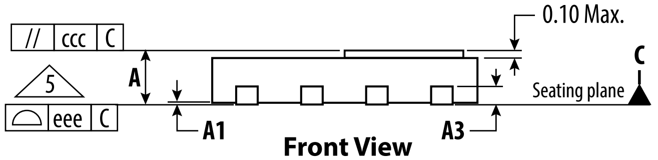
Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5

Part Marking

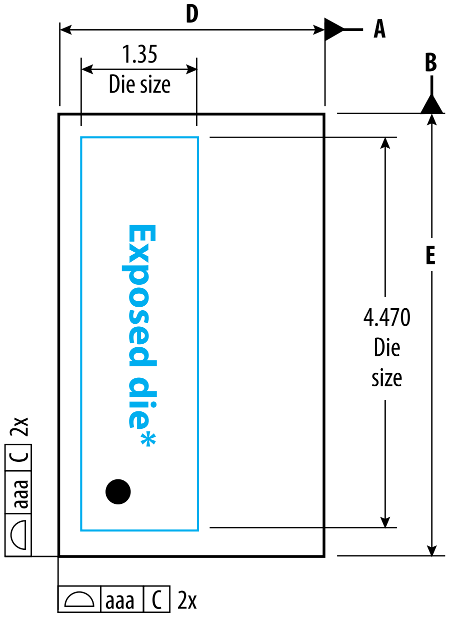


Part Number	Laser Markings	
	Part # Marking Line 1	Lot_Date Code Marking Line 2
EPC2307	2307	YYYYZZZZA

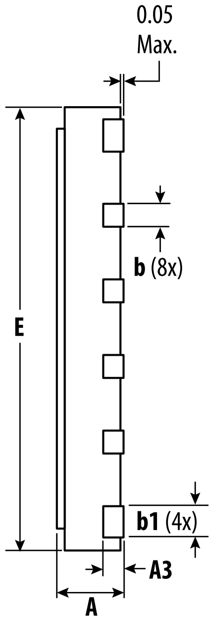




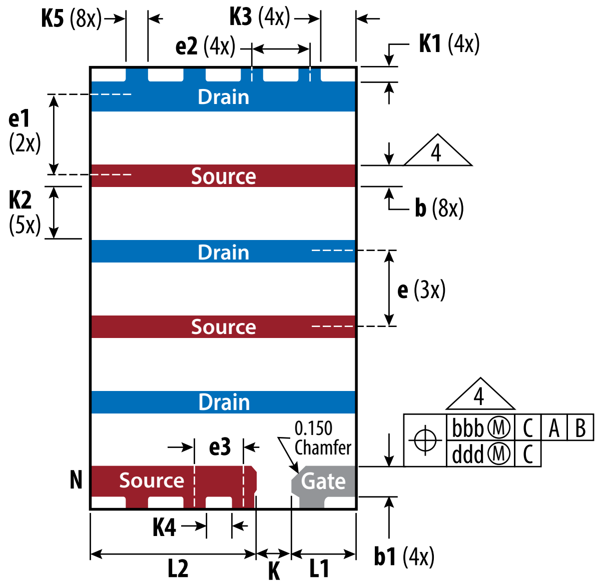
Front View



Top View



Side View



Bottom View

*The exposed die is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A			0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
D	2.90	3.00	3.10	
E	4.90	5.00	5.10	
e		0.85 BSC		
e1		0.90 BSC		
e2		0.65 BSC		
e3		0.55 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K		0.40 Ref		
K1		0.15 Ref		
K2		0.60 Ref		
K3		0.40 Ref		
K4		0.30 Ref		
K5		0.25 Ref		
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		7		3

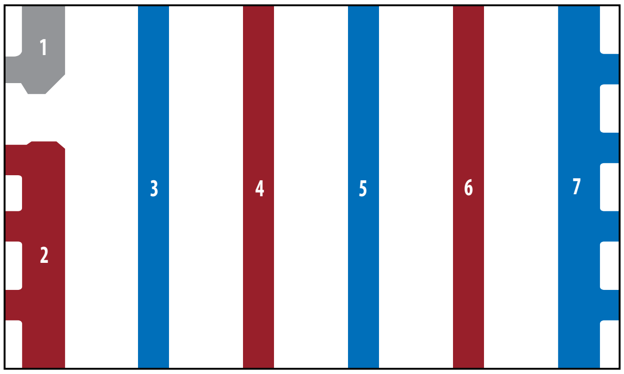
Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals

4. Dimension **b** applies to the metalized terminal and a radius on the other end of it, dimension **b** should not be measured in that radius area.

5. Coplanarity applies to the terminals and all the other bottom surface metallization.

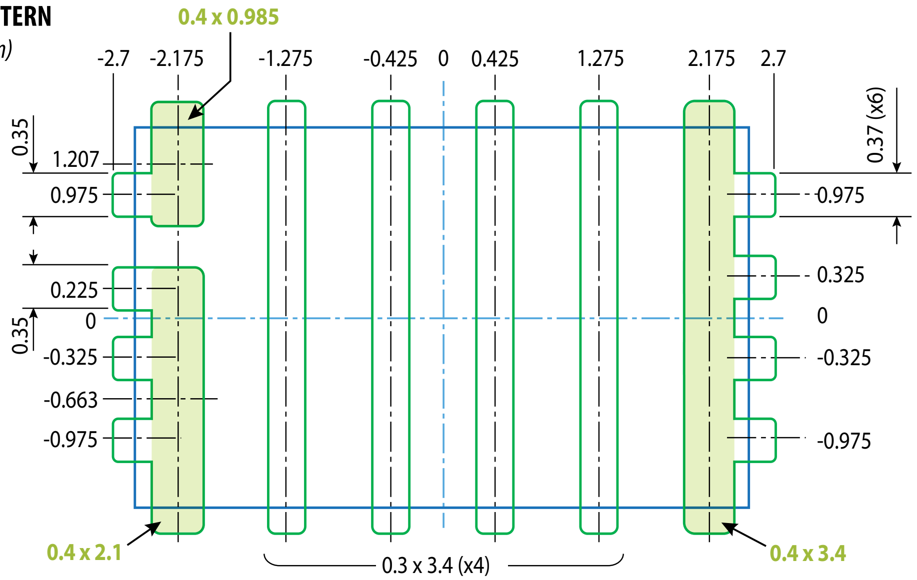
TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Legend:

Part outline

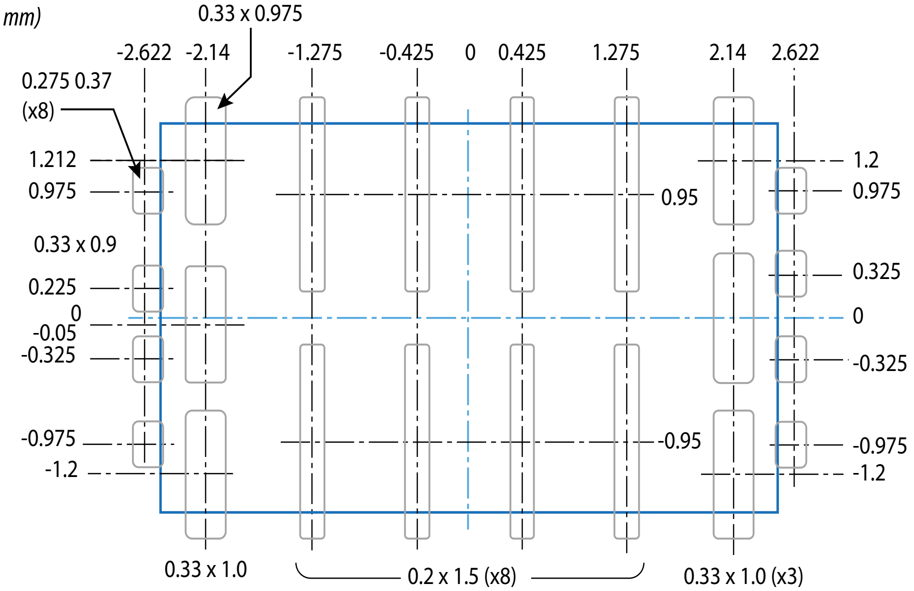
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



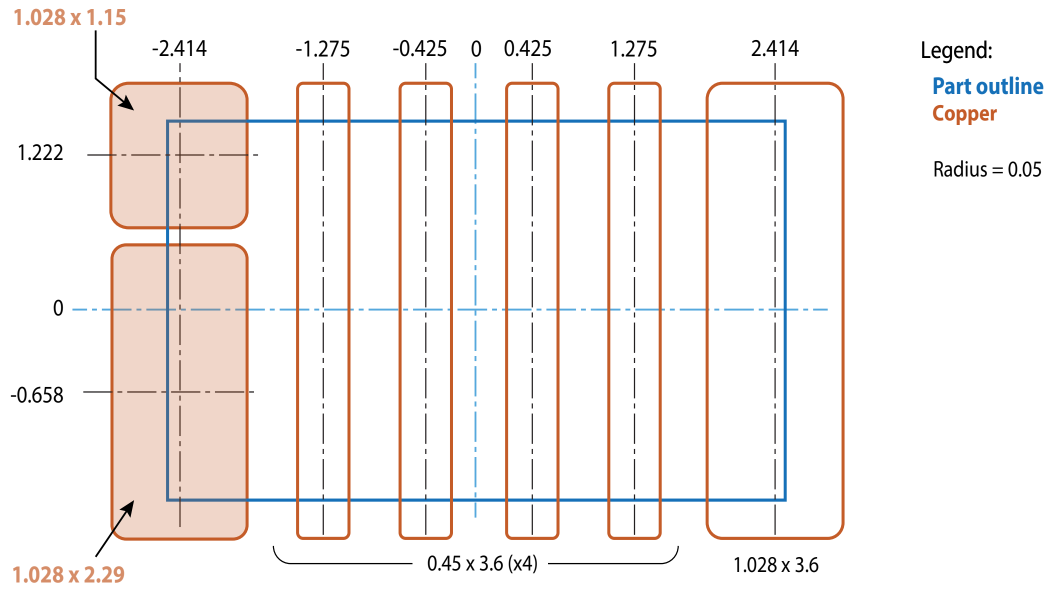
Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of 0.1.

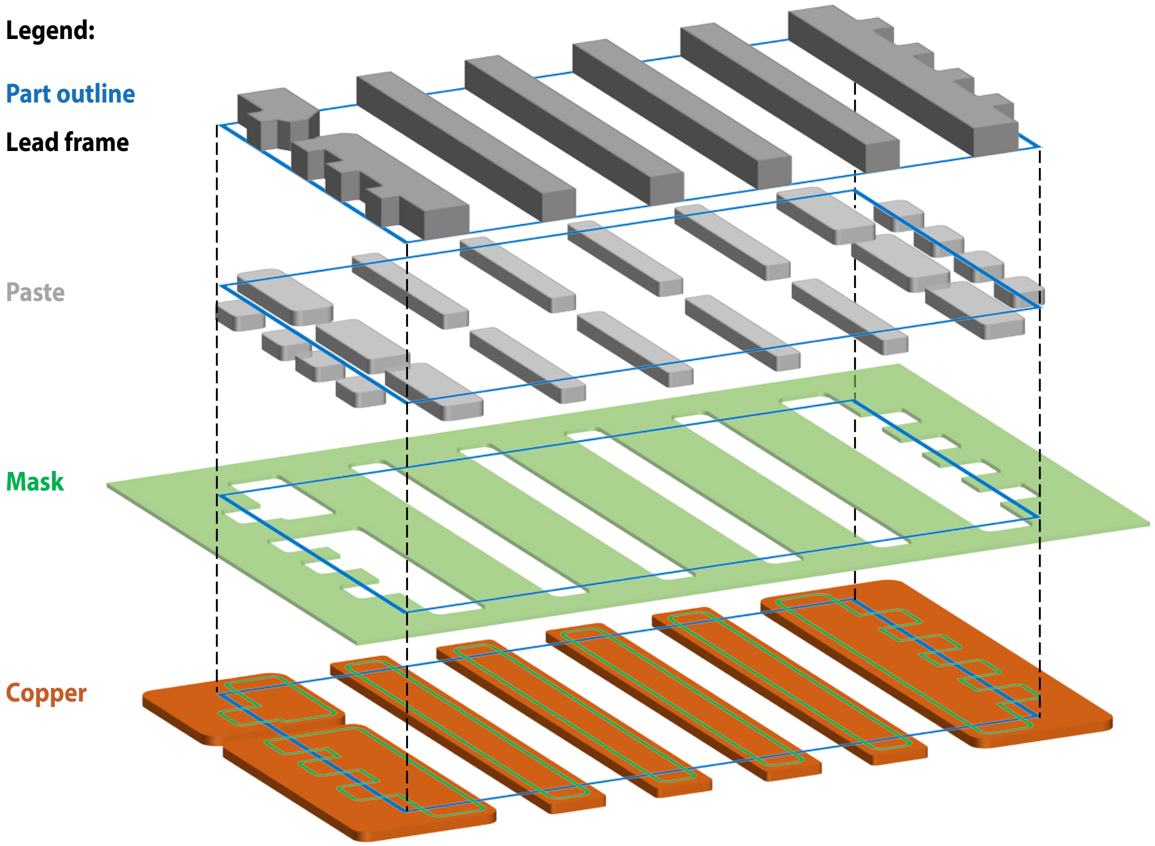
Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

RECOMMENDED COPPER DRAWING

(units in mm)



3D COMPOSITE



ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

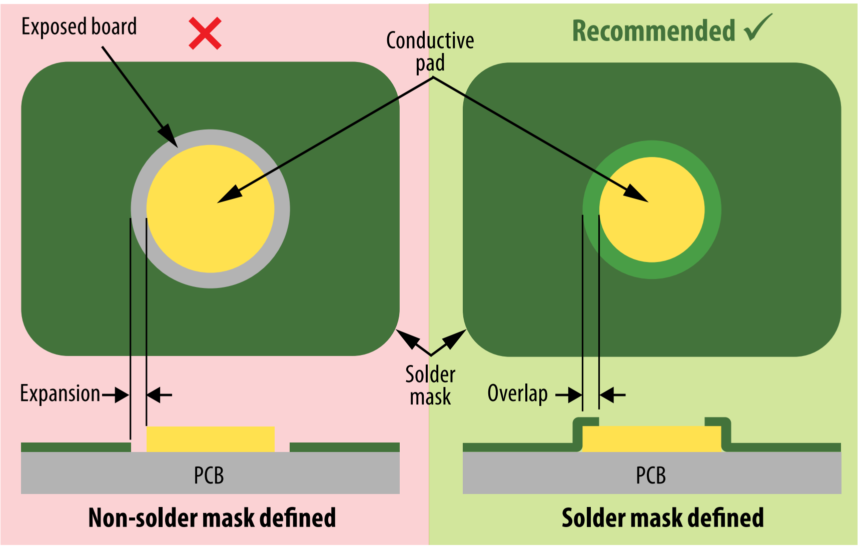


Figure 18: Solder mask defined versus non-solder mask defined pad

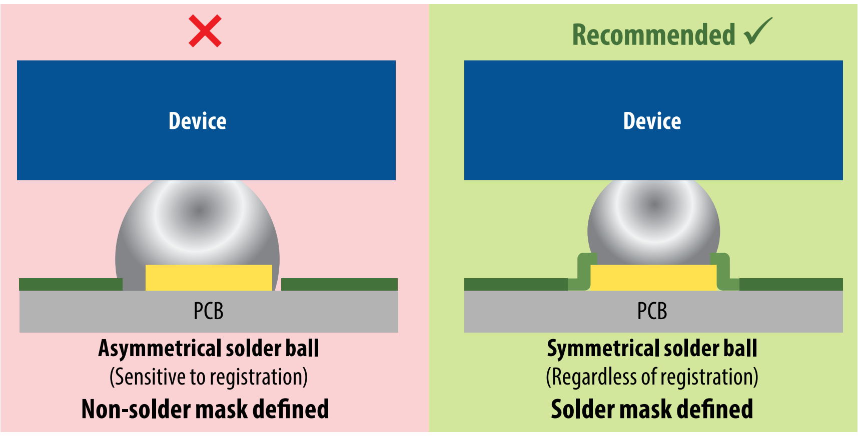


Figure 19: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip**
  (for preliminary device Altium footprints, contact EPC)