EPC23104 – ePower™ Stage IC

V_{IN}, 100 V

I_{Load}, 15 A

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised December 1, 2025

The ePower™ Stage IC Product Family integrates input logic interface, high-side level shifting, synchronous bootstrap charging, and gate drivers along with eGaN output FETs into one monolithic integrated circuit in an MSL1 QFN package, using EPC's proprietary GaN IC technology. The result is a Power Stage IC that translates logic level control signals into a high voltage and high current power stage, which is simpler to design, smaller in size and easier to manufacture while being more efficient to operate.

Questions:
Ask a GaN Expert

ASK AN EXPERT GaN

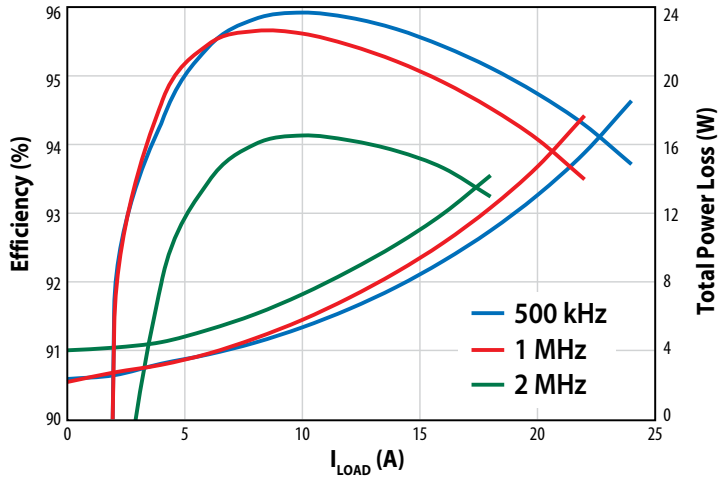
Key Parameters		
PARAMETER	**VALUE**	**UNIT**
Power Stage Load Current (1 MHz)	15	A
Operating PWM Frequency (Minimum)	5	kHz
Operating PWM Frequency (Maximum)	3	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	
Nominal Bias Supply Voltage	5	

Output Current and PWM Frequency Ratings are specified at ambient temperature of 25°C. See the Application Information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

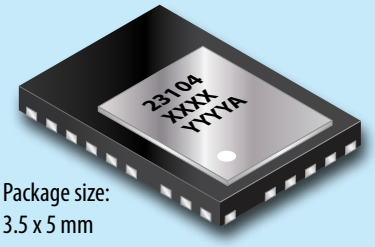
Device Information		
PART NUMBER	**Rated $R_{DS(on)}$ for HS and LS FETs at 25 °C**	**QFN Package Size (mm)**
EPC23104	8.7 mΩ + 8.7 mΩ typ	3.5 x 5

All exposed pads feature wettable flanks that allow-side wall solder inspection. High voltage and low voltage pads are separated by 0.6 mm spacing to meet IPC rules.

Figure 1: Performance Curves



Buck Converter, V_{IN} = 48 V, V_{OUT} = 12 V, Deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, Top Side Heatsink attached, Airflow = 400 LFM, T_A = 25°C, using **EPC90152 Evaluation Board**.



Package size:
3.5 x 5 mm

EPC23104 ePower™ Stage IC

Applications

- Buck, boost, buck-boost converters
- Half-bridge, full bridge LLC converters
- Motor drive inverters
- Class D audio amplifiers

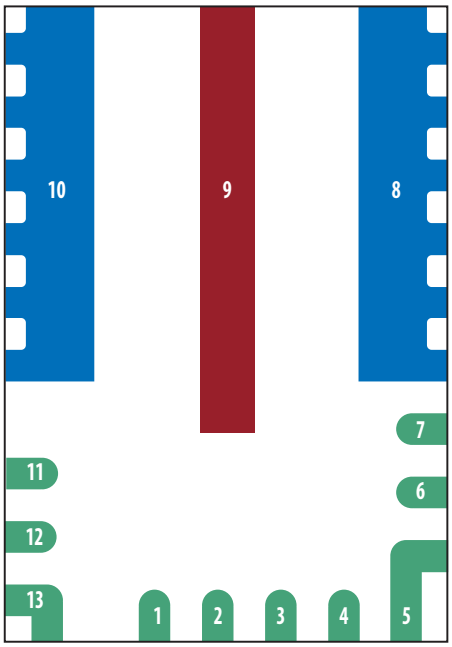
Features

- Integrated high-side and low-side eGaN® FET with internal gate driver and level shifter
- 5 V external bias supply
- 3.3 V or 5 V CMOS input logic levels
- Independent high-side and low-side control inputs
- Logic lockout commands both FETs off when inputs are both high at same time
- External resistors to tune SW switching times
- Robust level shifter operation for hard and soft switching conditions
- Synchronous charging for high-side bootstrap supplies
- Standby function for low quiescent current mode
- Power-on-reset for low-side and high-side power supplies
- Power stage high impedance guaranteed in absence of V_{DRV}/V_{BOOT} supplies
- Thermally enhanced QFN package with exposed top for low thermal resistance from junction to top-side heatsink

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC23104

Figure 2: EPC23104 Quad Flat No-Lead (QFN) Package (Transparent Top View)



Transparent Top View

EPC23104 Pinout Description

Pin	Pin Name	Pin Type	Description
1	HS_{IN}	L	High-side PWM logic input referenced to AGND. Internal pull-down resistor is connected between HS_{IN} and AGND.
2	LS_{IN}	L	Low-side PWM logic input referenced to AGND. Internal pull-down resistor is connected between LS_{IN} and AGND.
3	STB	L	V_{DD} standby input referenced to AGND. Internal V_{DD} is disabled when STB is pulled up or driven high. Internal pull-down resistor disables the standby function by default. Do NOT tie directly STB to V_{DD} (unless V_{DD} is tied to V_{DRV}).
4	V_{DD}	S	Internal power supply referenced to AGND, connect a bypass capacitor from V_{DD} to AGND.
5	V_{DRV}	S	External 5 V power supply referenced to AGND, connect a bypass capacitor from V_{DRV} to AGND.
6	R_{DRV}	G	Insert a resistor between R_{DRV} and V_{DRV} to control the turn-on slew rate of the low-side FET.
7	AGND	S	Logic ground. AGND is internally connected to PGND.
8	PGND	P	Power ground. Connected to the source terminal of the low-side FET.
9	SW	P	Switching node. Connected to half-bridge power stage output.
10	V_{IN}	P	Power DC input. Connected to drain terminal of the high-side FET. Connect power loop capacitors from V_{IN} to PGND.
11	V_{PHASE}	S	V_{PHASE} is Kelvin connected to SW. Used as ground return for the bootstrap capacitor C_{BOOT}.
12	R_{BOOT}	G	Insert a resistor between R_{BOOT} and V_{BOOT} to control the turn-on slew rate of the high-side FET.
13	V_{BOOT}	S	Floating bootstrap power supply referenced to V_{PHASE} (=SW). Connect an external bootstrap capacitor, C_{BOOT}, between V_{BOOT} and V_{PHASE}.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs, G = Gate Drive Adjust

Note: do not tie directly STB to V_{DD}, otherwise the IC will be damaged (unless V_{DD} is tied to V_{DRV}).

Note: AGND and PGND are internally connected.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to PGND unless indicated otherwise. AGND and PGND are internally connected.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
V_{IN}	DC Power input voltage		100	V
$SW_{(continuous)}$	Output switching node voltage, continuous		100	
V_{DRV}	External bias supply voltage (V_{DRV} to AGND)		6	
V_{DD}	Internal low-side supply voltage (V_{DD} to AGND)		6	
$V_{BOOT} - V_{PHASE}$	Internal high-side supply voltage (V_{BOOT} to V_{PHASE}), V_{PHASE} = SW		6	
HS_{IN}, LS_{IN}	PWM logic input voltage	-1	5.5	
STB	V_{DD} disable input voltage - standby function	-1	5.5	
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	

ESD Ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)(1)	+/-500		V
CDM	Charged-device model (JEDEC JESD22-C101)(2)	+/-500		

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

Thermal Characteristics

$R_{\theta JA\_JEDEC}$ is measured using JESD51-2 standard setup with 1 cubic foot enclosure with no forced air cooling, heat dissipated only through natural convection. The test used JEDEC Standard 4-layers PCB with 2 oz top and bottom surface layers and 1oz buried layers. $R_{\theta JA\_EVB}$ is measured using EPC90152 EVB with no forced air cooling, this rating is more indicative of actual application environment.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{\theta JC\_Top}$	Thermal resistance, junction-to-case (Top surface of exposed die substrate)	0.61	°C/W
$R_{\theta JB\_Bottom}$	Thermal resistance, junction-to-board (At solder joints of V_{IN}, SW and PGND pads)	3.7	
$R_{\theta JA\_JEDEC}$	Thermal resistance, junction-to-ambient (using JEDEC 51-2 PCB)	50	
$R_{\theta JA\_EVB}$	Thermal resistance, junction-to-ambient (using EPC90152 EVB)	27	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. If used outside the recommended operating conditions but within the absolute maximum ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device's lifetime. All voltage parameters are absolute voltages referenced to PGND unless indicated otherwise. AGND and PGND are internally connected.

Recommended Operating Conditions					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	DC power input voltage - V_{DRV} not tied to V_{DD}	10		80	V
$V_{IN(Boost\ Mode)}$	DC power input voltage - V_{DRV} tied to V_{DD} (3)	0			
$SW_{(Q3\ Mode)}$	Output switch node, 3rd quadrant mode	-2.5		V_{IN} + 2.5	
$SW_{(pulse2ns)}$	Output switch node, transient pulse < 2 ns	-10		V_{IN} + 10	
V_{DRV}	External supply voltage (V_{DRV} to AGND)	4.75	5	5.5	
V_{DD}	Internal low-side supply voltage (V_{DD} to AGND)	4.75	5	5.5	
$V_{BOOT} - V_{PHASE}$	Internal high-side supply voltage (V_{BOOT} to V_{PHASE}), V_{PHASE} = SW	4.75	5	5.5	
HS_{IN}, LS_{IN}	PWM logic input voltage	0		5	
STB	V_{DD} disable input voltage – standby function	0		5	
$T_{J,op}$	Operating junction temperature	-40		125	°C

(3) Tie V_{DD} and V_{DRV} together to disable the standby function, see figure 13.

Electrical Characteristics

Nominal V_{IN} = 48 V, V_{DRV} = V_{DD} = 5 V and (V_{BOOT} – V_{PHASE}) = 5 V. All typical ratings are specifed at T_A = 25°C unless otherwise indicated. All voltage parameters are absolute voltages referenced to PGND unless indicated otherwise. AGND and PGND are internally connected. Parameters that show only the typical value are guaranteed by design and not tested in production.

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Low-side Power Supply						
I_{DRV_Q}	OFF state total quiescent current	HS_{IN}/LS_{IN}/STB = 0 V, SW floating	7	10	13	mA
I_{DRV_100kHz}	Total operating current @100 kHz	PWM = 100 kHz, 50% ON-time, includes bootstrap current		16		
I_{DRV_1MHz}	Total operating current @1 MHz	PWM = 1 MHz, 50% ON-time, includes bootstrap current		23		
Standby Current						
$I_{VIN\_standby}$	V_{IN} current in standby mode	STB = 5 V		110	180	µA
$I_{DRV\_standby}$	V_{DRV} current in standby mode	STB = 5 V		1	50	
Bootstrap Power Supply						
I_{BOOT_Q}	OFF state bootstrap supply current	HS_{IN}/LS_{IN}/STB = 0 V	4	6	8	mA
I_{BOOT_100kHz}	Bootstrap supply current @100 kHz	HS PWM = 100 kHz, 50% ON-time		7		
I_{BOOT_1MHz}	Bootstrap supply current @1 MHz	HS PWM = 1 MHz, 50% ON-time		12		
$R_{ON\_SYNC\_BOOT}$	ON resistance of sync-boot FET	I_{SYNC_BOOT} = 25 mA	1	1.7	2.6	Ω
Power On Reset						
V_{DD_POR+}	POR trip level V_{DD} rising	LS_{IN} = 5 V, V_{DD} ramps up			4.25	V
$V_{DD\_POR\_HYST}$	POR V_{DD} falling hysteresis	LS_{IN} = 5 V, V_{DD} ramps down		0.15		
V_{BOOT_POR+}	POR trip level (V_{BOOT} - V_{PHASE}) rising	HS_{IN} = 5 V, V_{BOOT} ramps up			4.25	
$V_{BOOT\_POR\_HYST}$	POR (V_{BOOT} - V_{PHASE}) falling hysteresis	HS_{IN} = 5 V, V_{BOOT} ramps down		0.15		
Logic Input Pins						
V_{IH}	High-level logic threshold	HS_{IN}, LS_{IN} rising	2.4			V
V_{IL}	Low-level logic threshold	HS_{IN}, LS_{IN} falling			0.8	
V_{IHYST}	Logic threshold hysteresis	V_{IH} rising – V_{IL} falling	0.3			
R_{IN}	HS_{IN} and LS_{IN} pull-down resistance	HS_{IN}, LS_{IN} = 5 V		5		kΩ
V_{DD} Disable - Standby Function						
V_{STB_H}	High-level STB logic threshold	STB rising	2.4			V
V_{STB_L}	Low-level STB logic threshold	STB falling			0.8	
R_{STB}	STB pull-down resistance	STB = 5 V		200		kΩ
High-Side Internal Power FET (HS_FET)						
$R_{DS(on)\_HS}$	High-side FET $R_{DS(on)}$	I_{SW} = +/-1 A, HS_{IN} = 5 V, LS_{IN} = 0 V (2)		8.7	11	mΩ
$V_{HS\_DS\_Clamp}$	High-side 3rd quadrant clamp	I_{SW} = - 1 A, HS_{IN} = LS_{IN} = 0 V (2)	-2.1	-1.7		V
$V_{HS\_DS\_Clamp\_0V}$	High-side 3rd quadrant clamp	I_{SW} = - 1 A, HS_{IN} = LS_{IN} = 0 V, V_{BOOT} – V_{PHASE} = 0 V (2)		-3.5		
C_{OSS_HSFET}	Output capacitance (V_{IN} to SW)	HS_{IN} = 0 V, SW = 0 V		189		pF
Q_{OSS_HSFET}	Output charge (V_{IN} to SW)	HS_{IN} = 0 V, SW = 0 V		15		nC
E_{QOSS_HSFET}	Output capacitance stored energy	HS_{IN} = 0 V, SW = 0 V		0.27		µJ
$E_{ON\_HS\_0}$	Turn-ON switching energy (HS_FET)	HS turn-ON, SW = 0 V to 48 V, R_{BOOT} = 0 Ω, I_{SW} = 1 A (2,4)		1.5		
$E_{ON\_HS\_1}$		HS turn-ON, SW = 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{SW} = 1 A (2,4)		2.7		
E_{OFF_HS}	Turn-OFF switching energy (HS_FET)	HS turn-OFF, SW = 48 V to 0 V, I_{SW} = 1 A (2,4)		0.09		
Low-Side Internal Power FET (LS_FET)						
$R_{DS(on)\_LS}$	Low-side FET $R_{DS(on)}$	I_{SW} = +/-1 A, LS_{IN} = 5 V, HS_{IN} = 0 V (2)		8.7	11	mΩ
$V_{LS\_DS\_Clamp}$	Low-side 3rd quadrant clamp	I_{SW} = 1 A, HS_{IN} = LS_{IN} = 0 V (2)	-2.1	-1.7		V
$V_{LS\_DS\_Clamp\_0V}$	Low-side 3rd quadrant clamp	I_{SW} = 1 A, HS_{IN} = LS_{IN} = 0 V, V_{DD} = 0 V (2)		-3.5		
C_{OSS_LSFET}	Output capacitance (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		189		pF
C_{WELL}	HV-well capacitance (SW to PGND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		32		
Q_{OSS_LSFET}	Output charge (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		15		nC
E_{QOSS_LSFET}	Output capacitance stored energy	LS_{IN} = 0 V, SW = 48 V		0.27		µJ
$E_{ON\_LS\_0}$	Turn-ON switching energy (LS_FET)	LS turn-ON, SW = 48 V to 0 V, R_{DRV} = 0 Ω, I_{SW} = -1 A (2,4)		1.5		
$E_{ON\_LS\_1}$		LS turn-ON, SW = 48 V to 0 V, R_{DRV} = 2.2 Ω, I_{SW} = -1 A (2,4)		2.7		
E_{OFF_LS}	Turn-OFF switching energy (LS_FET)	LS turn-OFF, SW = 0 V to 48 V, I_{SW} = -1 A (2,4)		0.09		

Electrical Characteristics *(continued)*

Electrical Characteristics# (continued)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power FETs Quiescent Currents – include internal biasing circuits(3)						
I_{Q_VIN-SW}	Quiescent current (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 100 V, SW = 0 V			250	µA
$I_{Q\_SW-PGND}$	Quiescent current (SW to PGND)	LS_{IN} = 0 V, V_{IN} = 100 V, SW = 100 V			1.3	mA
$I_{Q\_VIN-PGND}$	Quiescent current (V_{IN} to PGND)	HS_{IN} = 0 V, V_{IN} = 100 V		119	250	µA
		HS_{IN} = 0 V, V_{IN} = 48 V			160	
Dynamic Characteristics (Logic Input to Output Switching Node SW) (See Figure 3a and 3b for Test Circuit and Timing Diagram)						
PW_{Range}	Pulse width range ($PW_{\_min}$ to $PW_{\_max}$)	50% to 50% width, LS_{IN} and HS_{IN}	0.03(1)		200(7)	µs
t_{Filter}	Input filter cutoff time	50% to 50% width, LS_{IN} and HS_{IN}		15		ns
$t\_delay_{HS\_on}$	High-side ON propagation delay	SW = 0 V and HS FET turn-ON		36		
$t\_delay_{LS\_on}$	Low-side ON propagation delay	SW = 48 V and LS FET turn-ON		36		
$t\_delay_{HS\_off}$	High-side OFF propagation delay	SW = 48 V and HS FET turn-OFF		36		
$t\_delay_{LS\_off}$	Low-side OFF propagation delay	SW = 0 V and LS FET turn-OFF		36		
t_match_{on}	Delay matching LS_{off} to HS_{on}	LS turn-OFF to HS turn-ON		0		
t_match_{off}	Delay matching HS_{off} to LS_{on}	HS turn-OFF to LS turn-ON		0		
t_lockout	Cross-conduction lockout time	LS turn-OFF to HS turn-ON or HS turn-OFF to LS turn-ON – no dead time on LS_{IN} HS_{IN} inputs		5		
$t\_rise_{SW\_HS0}$	SW rise time at high-side FET turn-ON (buck mode, hard switching)	HS turn-ON buck mode, 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 5 A (4)		1		
$t\_rise_{SW\_HS4.7}$		HS turn-ON buck mode, 0 V to 48 V, R_{BOOT} = 4.7 Ω, I_{LOAD} = 5 A (4)		3		
$t\_fall_{SW\_LS0}$	SW fall time at low-side FET turn-ON (boost mode, hard switching)	LS turn-ON boost mode, 48 V to 0 V, R_{DRV} = 0 Ω, I_{LOAD} = 5 A (4)		1		
$t\_fall_{SW\_LS4.7}$		LS turn-ON boost mode, 48 V to 0 V, R_{DRV}= 4.7 Ω , I_{LOAD} = 5 A (4)		3		
$t\_rise_{SW\_HS10}$	SW rise time at high-side FET turn-ON (motor drive, hard switching)	HS turn-ON current exiting from SW node, 0 V to 48 V, R_{BOOT} = 10 Ω, I_{LOAD} = 5 A (5)		5		
$t\_fall_{SW\_LS10}$	SW fall time at low-side FET turn-ON (motor drive, hard switching)	LS turn-ON current entering the SW node, 48 V to 0 V, R_{DRV} = 10 Ω, I_{LOAD} = 5 A (5)		5		

(1) Not tested, guaranteed by design

(2) I_{SW} is positive when exiting from SW node

(3) The quiescent currents include the power FET I_{DSS} as well as the internal circuits biasing currents

(4) Measured on application board EPC90152

(5) Measured on application board EPC91104

(6) $C_{OSS\_LS\_Total} = C_{OSS\_LSFET} + C_{WELL}$ for the low-side GaN FET includes the capacitance C_{WELL} of the high-side driver and high-side power FET circuit

(7) $PW_{\_max}$ for the high-side FET depends also on the external bootstrap capacitor. If the C_{BOOT} capacitance value is low, the under voltage threshold may be hit before the IC internal capacitors are discharged.

Dynamic Characteristics Parameter Definition

Figure 3a: Test Circuit for Dynamic Characteristics

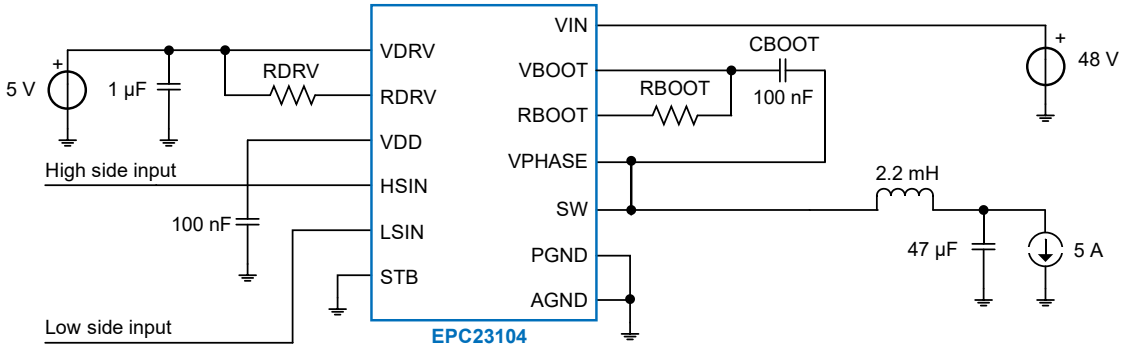
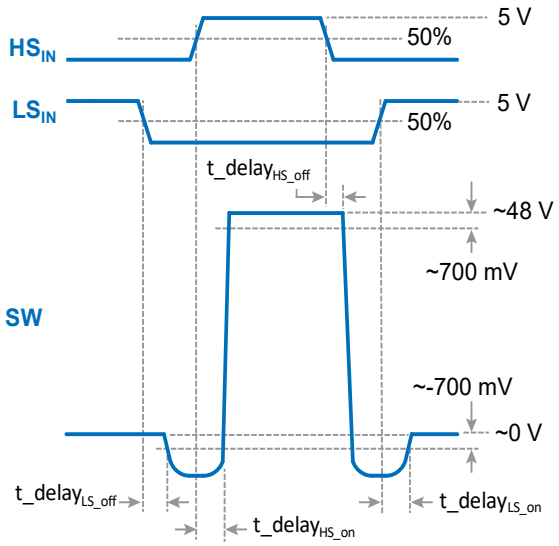


Figure 3b: Logic Input to Output Switching Node Timing Diagram (current exiting from SW node)



Output Capacitance vs. Drain-to-Source Voltage

Figure 4a: C_{OSS_HSFET} of high-side Power GaN FET

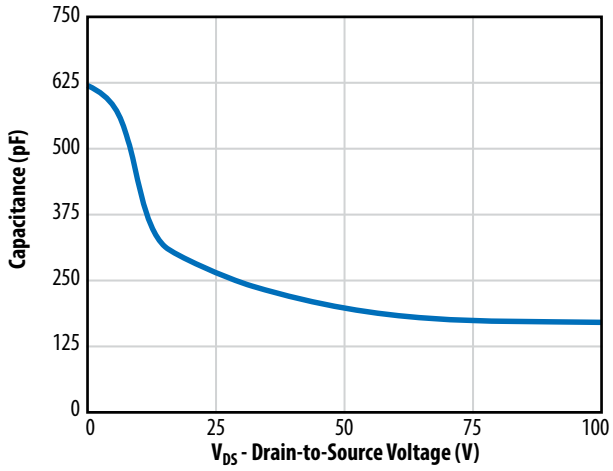
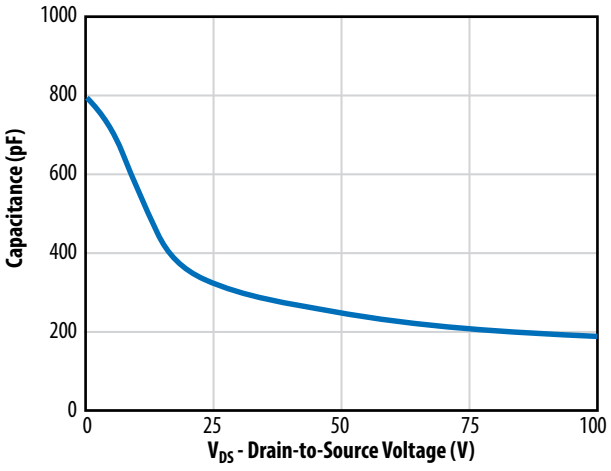


Figure 4b: $C_{OSS\_LS\_Total} = C_{OSS\_LSFET} + C_{WELL}$ for low-side Power GaN FET



Typical Output Charge and C_{OSS} Stored Energy

Figure 5a: Q_{OSS} and E_{OSS} of High-Side Power GaN FET

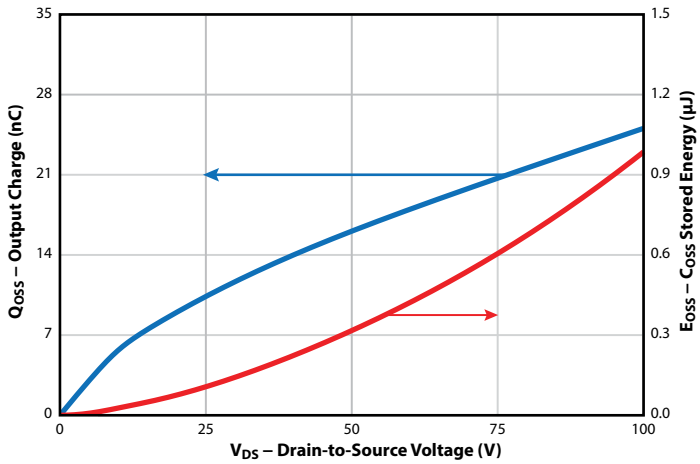
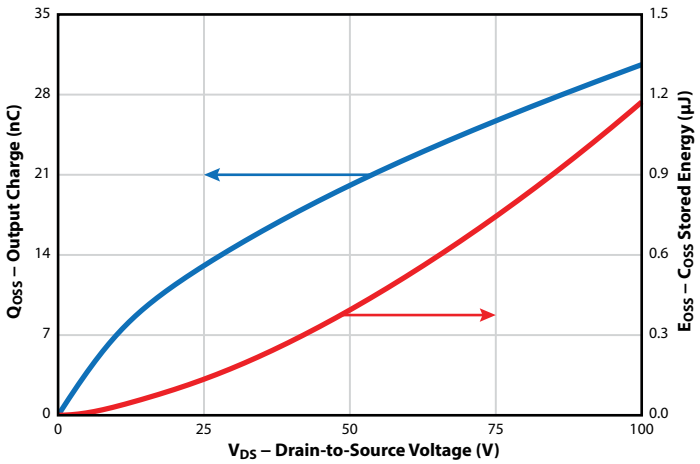


Figure 5b: Q_{OSS} and E_{OSS} of Low-Side Power GaN FET



Power GaN FETs Typical $R_{DS(on)}$ vs. Temperature

Figure 6a: High-Side FET $R_{DS(on)}$

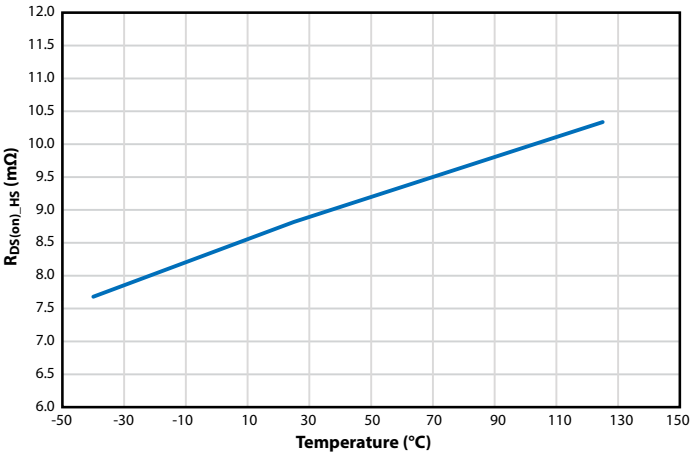
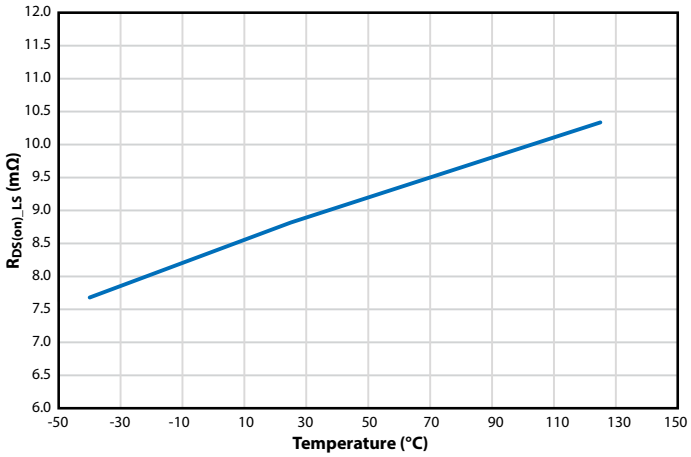


Figure 6b: Low-Side FET $R_{DS(on)}$



Truth Table

STB	V_{DD}	$V_{BOOT} - V_{PHASE}$	HS_{IN}	LS_{IN}	HS FET	LS FET
High	$<V_{DD\_POR}$	–	–	–	OFF	OFF
	$>V_{DD\_POR}$	$<V_{BOOT\_POR}$	–	0	OFF	OFF
			–	1	OFF	ON (1)
	$>V_{DD\_POR}$	$>V_{BOOT\_POR}$	0	0	OFF	OFF
			0	1	OFF	ON (1)
			1	0	ON (1)	OFF
			1	1	OFF	OFF
Low	$<V_{DD\_POR}$	–	-	-	OFF	OFF
	$>V_{DD\_POR}$	$<V_{BOOT\_POR}$	–	0	OFF	OFF
			–	1	OFF	ON
	$>V_{DD\_POR}$	$>V_{BOOT\_POR}$	0	0	OFF	OFF
			0	1	OFF	ON
			1	0	ON	OFF
			1	1	OFF	OFF

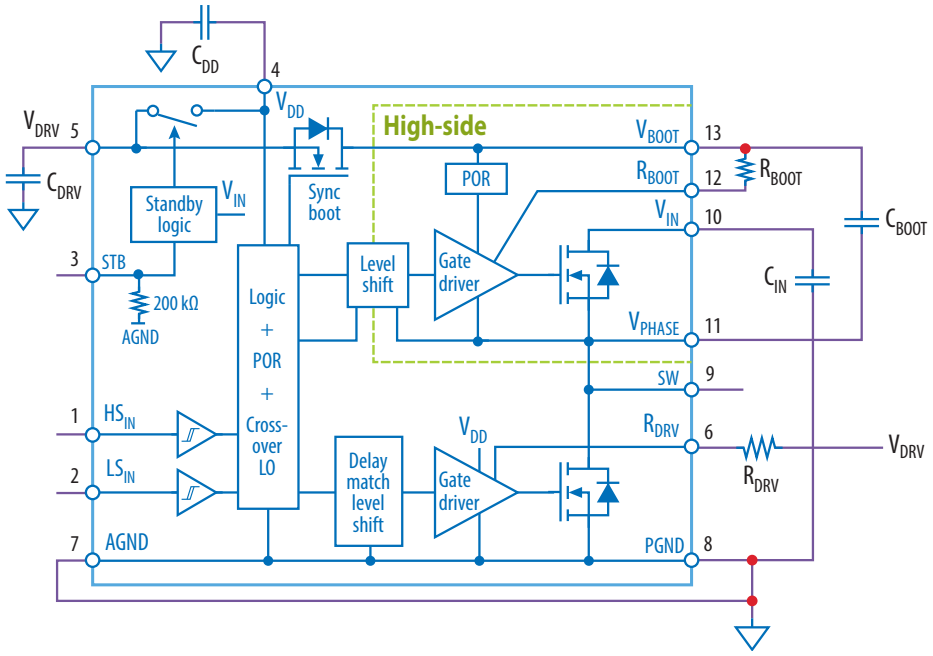
(1) STB does not directly inhibit PWM inputs. During the discharge transient of V_{DD} and V_{BOOT} capacitors, as long as $V_{DD} > V_{DD\_POR}$ and $V_{BOOT} > V_{BOOT\_POR}$, the power FETs still follow the input signals.

Application Information

General Description

The EPC23104 ePower™ Stage IC integrates a half-bridge gate driver with internal high-side and low-side FETs. Integration is implemented using EPC's proprietary GaN IC technology. The monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits controlling high-side and low-side eGaN output FETs configured as a half-bridge power stage. Robust level shifters from low-side to high-side channels are designed to operate correctly with soft and hard switching conditions even at large negative clamped voltage and to avoid false trigger from fast dv/dt transients including those driven by external sources or other phases. Internal circuits integrate the functions of charging and disabling of the logic and bootstrap power supplies. Protection features are added to protect the output FETs from unwanted turn-on at low or even complete loss of supply voltages. The single chip GaN IC is mounted inside a 3.5 x 5 mm Quad Flat No-lead (QFN) package using a flip chip on lead-frame technique. This packaging structure allows very low parasitic inductance from the power terminals to the underlying PCB solder pads. The exposed QFN pads are designed to have at least 0.6 mm spacing between high and low voltage pins to meet IPC voltage creepage rule for 100 V. Another enhancement exposes the backside of the GaN IC die on the top side of the package while completely encapsulating the rest of the GaN IC die. This allows a very low thermal resistance path from the die junction to an attached heatsink which in effect increases the allowable power dissipation and thus higher current handling capability.

Figure 7: Functional Block Diagram



Output Current Rating

Power stage output current rating is best thought of as a figure of merit for specified output current level that accounts for the maximum amount of power dissipation allowed from the IC. Total power dissipation from a power stage IC is tied to the application circuit topologies, output current demand, switching frequencies, construction, operating temperature range, thermal management technique and mechanical stress limit of the metallization imposed by electromigration. The rating is related to the respective maximum current capability of the two integrated output FETs in the half-bridge power stage but not measured the same way as individual discrete FET. For a power stage IC such as EPC23104, total power loss from the IC is the sum of the two output FETs conduction, switching and deadtime losses imposed by the application topologies at operating switching frequencies as well as power losses from the gate drive and logic circuit.

The maximum power dissipation is defined by the following formula:

$$\text{Max } P_{Diss} = (\text{Max } T_J - T_A) / R_{\theta JA}$$

where Max T_J is specified at 125 °C and the ambient temperature is specified at 25 °C. The big variable in achieving the theoretical maximum power dissipation is $R_{\theta JA}$, the thermal resistance from junction to ambient. The EPC23104 package construction allows two parallel paths of heat dissipation where the bottom path goes from junction to metallization to lead-frame then the exposed pads at the bottom of the package. $R_{\theta JB\_bottom}$ is determined by the three power bars (V_{IN}, SW and PGND) which are designed to allow maximum contact area to the underlying PCB pads. The total thermal resistance to ambient in this path of $R_{\theta JA\_bottom}$ needs to add the heat dissipation from the PCB pads through the multi-layer PCB construction then radiating to the ambient which is highly dependent on the airflow and forced cooling method. (See Figure9).

Figure 8: EPC23104 QFN package outline, pinouts and exposed backside of the GaN IC die

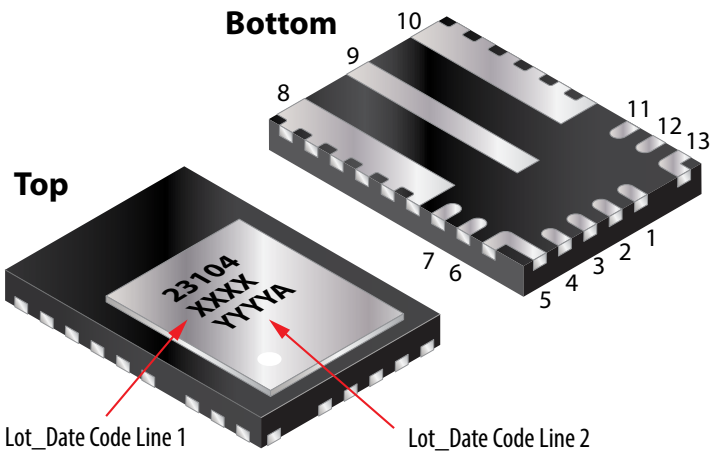
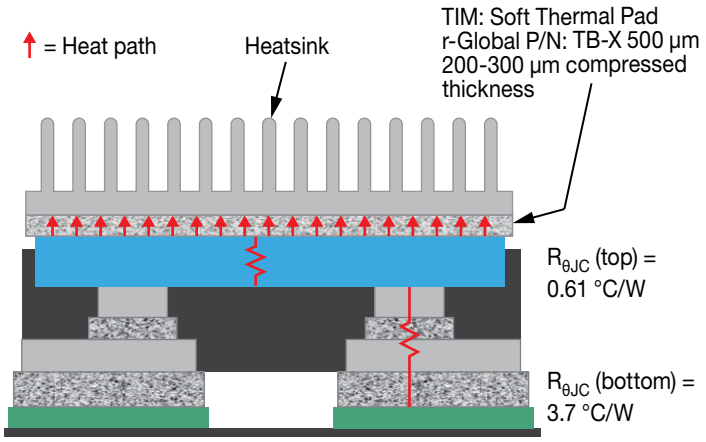


Figure 9: Parallel Thermal Resistance Paths of EPC23104 IC from Junction to Ambient



To achieve even lower effective thermal resistance, another path is provided from junction to the relatively lower thermal resistance Si substrate of the GaN IC structure to the exposed backside of the entire die at the top of the package to achieve a $R_{\theta JC\_top}$ of 0.61 °C/W. This lower PCB thermal resistance path facilitates attachment of a topside heatsink through thermal interface material (TIM) to the exposed backside of the die. Note that the backside of the die is connected to the PGND (=AGND) pins which potentially provides added benefits of using electrically conductive TIM which has >2X higher thermal conductivity and lower cost than the insulating type. Typical parameters of electrically conducting vs. insulating TIMs are shown in the table below. The resistance between the exposed backside and PGND is at least 100 Ω, due to the low doping level of the Si substrate.

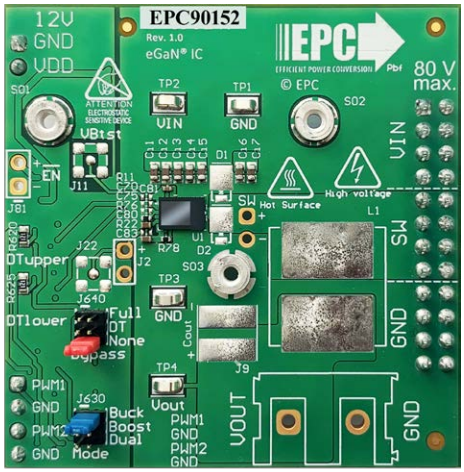
Typical parameters of electrically conducting vs. insulating TIMs		
Type of TIM	**Thermal Conductivity (W/m·K)**	**Relative Cost**
Electrically Conducting	40	1
Electrically Insulating	15	1.3

Another factor in specifying the output current rating is electromigration from a metallurgical standpoint. For EPC23104 this limit is a function of the metallization structure underlying the two output FETs plus their connection to the lead-frame and the three exposed power bars.

DC/DC Buck Converter Example

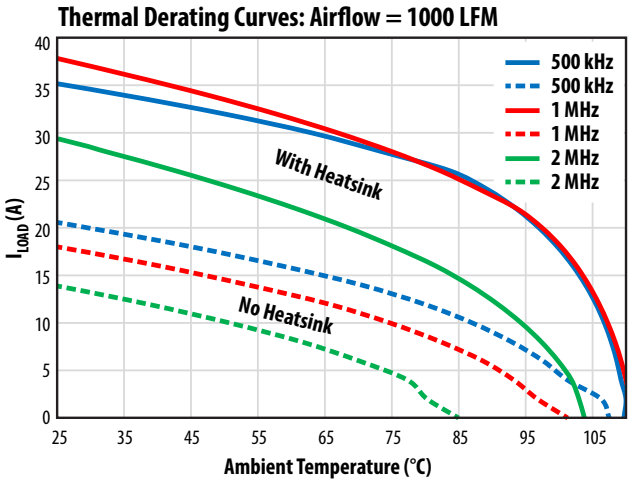
To provide real world test results, EPC uses a reference evaluation board, EPC90152 as shown in Figure 11, configured in a Buck Converter topology with the following test conditions: V_{IN} = 48 V, V_{OUT} = 12 V, PWM frequency = 0.5, 1, and 2 MHz, with and without top side heatsink, airflow = 400 and 1000 LFM, operating at ambient temperature starting at 25°C, maximum TC not to exceed 110°C (derated from 125°C to avoid thermal runaway).

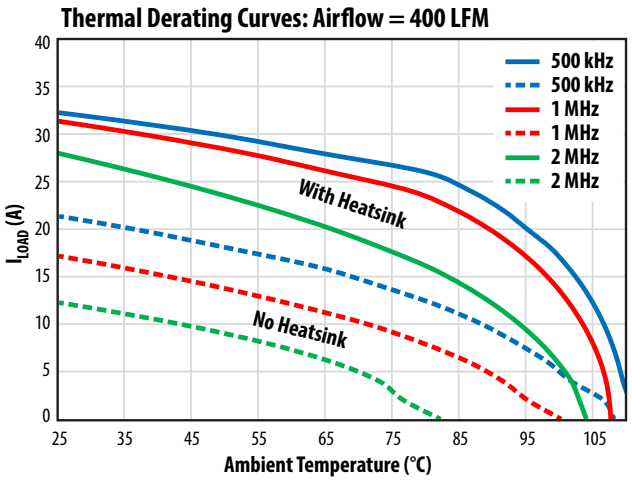
Figure 10: EPC90152 Evaluation Board (see EPC90152 Quick Start Guide for details)



Thermal derating curves in Figure 10 are derived from measurement data. The difference between curves with top side heatsink (full lines) and without (dashed lines) show the dramatic difference of using the lower $R_{\theta JC\_top}$ of the higher thermal conductive path.

Figure 11: Thermal Derating Curves for Output Current Rating of EPC23104 IC using EPC90152 Evaluation Board





Motor Drive Inverter Example

The EPC91104 evaluation board shown in Figure 12 is a 3-phase BLDC motor drive inverter board that can deliver up to 21 Apk (15 A_{RMS}) steady-state output current and up to 28 Apk (20 A_{RMS}) pulsed output current (t_{pulse}= 300 ms at 5%, 10%, and 20% of the total period). The EPC91104 contains all the necessary critical function circuits to support a complete motor drive inverter. Figure 13 depicts the steady-state thermal performance of the EPC91104 board. When operated on a motor bench at an ambient temperature of 22°C, with a 48 V_{DC} supply and natural convection, the EPC91104 can deliver 11 A_{RMS} per phase without a heatsink and 15 A_{RMS} per phase with a heatsink attached, with a temperature rise below 60°C from the IC case to ambient. Motor drive operating points at PWM = 20, 50, and 100 kHz, deadtime = 50 ns, with and without heatsink at 22°C ambient temperature, under natural convection.

Figure 12: EPC91104 Evaluation Board (see EPC91104 Quick Start Guide for details)

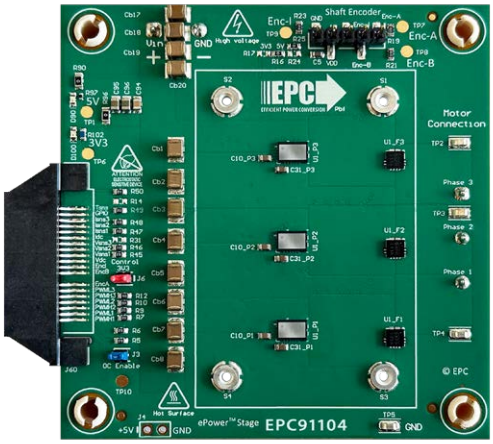
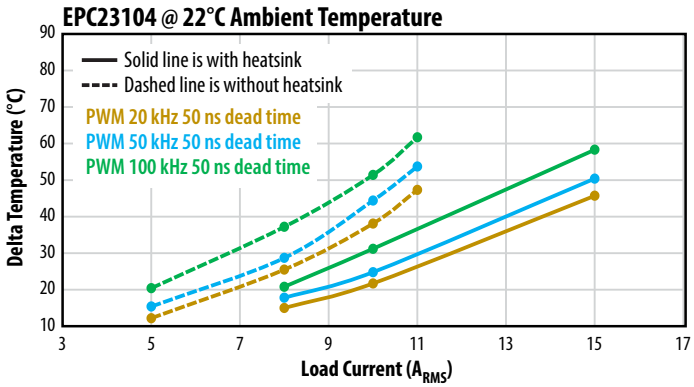


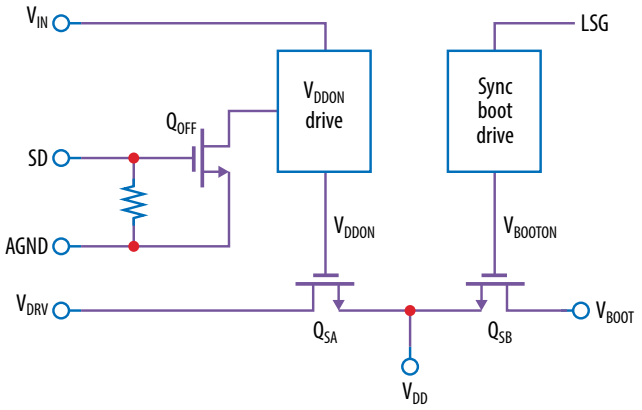
Figure 13: EPC91104 eGaN IC Temperature Increase vs. Ambient Temperature



Power Supplies – V_{IN}, V_{DRV}, V_{DD}, and V_{BOOT}

The EPC23104 IC only requires an external 5 V V_{DRV} power supply. Internal low-side and high-side power supplies, V_{DD} and V_{BOOT}, are generated from the external supply via two independent switches. Figure 14 shows the simplified circuit diagram of the different power supplies inside the IC and their interaction with each other.

Figure 14: Simplified Circuit Diagram of V_{IN}, V_{DRV}, V_{DD}, and V_{BOOT} Power Supplies



The internal supplies can be disabled to save quiescent power by turning off the series switch, Q_{SA} in Figure 14, with 5 V applied to the STB pin to engage chip standby mode. In this mode, minimum current is drawn from the external V_{DRV} supply while V_{DD} is open circuit. Whatever charge remains within the V_{DD} bypass capacitor will be discharged by the chip internal circuits by I_{DRV_Q}.

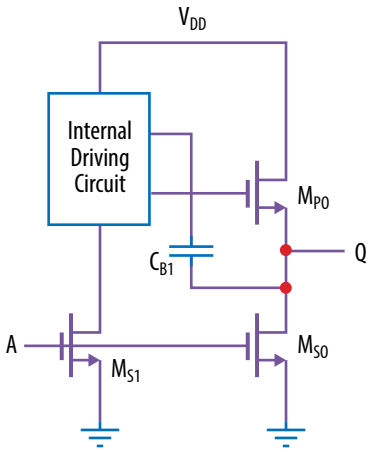
In the chip standby circuit, series switch (Q_{SA}) between V_{DRV} and V_{DD} is turned off by an internal standby circuit which itself derives its power from V_{IN} such that the chip draws a current $I_{VIN\_disable}$ from V_{IN} when standby mode is engaged. The standby function requires a minimum input voltage of $V_{IN,min}$ for the IC to be enabled. Below $V_{IN,min}$, the pass-transistor between V_{DRV} and V_{DD} will be off. To disable the standby function, and thus extend the minimum operating voltage to $V_{IN(Boot\ Mode)min}$ = 0 V, tie pins V_{DD} and V_{DRV} together.

This is mandatory in boost converter applications, when DC input voltage, applied to SW pin, is lower than 13.5 V (= V_{INmin} + $|V_{HS\_DS\_Clamp\_0V}|$). Moreover, in boost mode, if the feed-through operation mode is required, it is recommended to use a Schottky diode in parallel to the high-side GaN FET to mitigate the losses during non-switching operation (both HS_{IN} and LS_{IN} OFF, or there is no V_{DD}). The series connected high voltage synchronous bootstrap FET, Q_{SB} in Figure 14, between V_{DD} and V_{BOOT} for the high-side floating bootstrap supply is activated only after the LS FET (Q2) is turned on to avoid overcharging during deadtime. The use of GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage is the lower dropout voltage of approximately 100 mV from the synchronous FET versus typical Si bootstrap diode voltage of 0.6 V. With synchronous charging V_{BOOT} is maintained closer to the V_{DD} voltage, allowing the HS FET gate drive circuit to have similar gate drive current and delay performance as the LS FET gate drive circuit.

Gate Driver

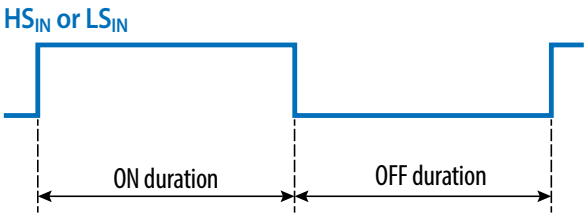
The EPC23104 IC integrates both HS and LS FET gate drivers with low impedance and high pulse current push-pull NFET output stage. Figure 15 is the simplified circuit diagram of the gate driver output stage.

Figure 15: Simplified Circuit Diagram of Gate Driver Output Stage



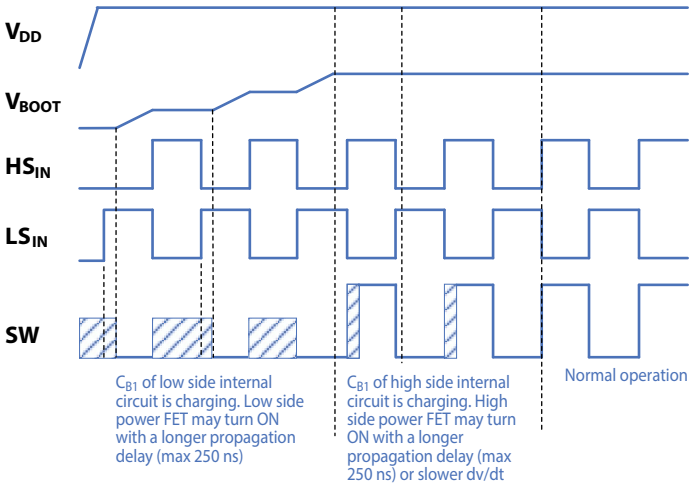
The LS and HS gate drive voltage levels are derived from their respective internal low-side (V_{DD}) and high-side (V_{BOOT}) power supplies. To ensure that the gate drive level (Q) is sufficiently close to V_{DD} or V_{BOOT}, an internal driving circuit is used to turn-on M_{PO}. Here M_{PO} and M_{SO} work similarly to the half-bridge power stage Q1 and Q2 output FETs except all the circuits are internal to the IC. C_{B1} is a representation of the internal capacitors used in the gate driving circuitry. The gate driver output (Q) cannot have 100% duty cycle to allow for C_{B1} to be refreshed, therefore the PWM input pulse width has boundaries. All dynamic characteristics are guaranteed for input pulse widths within PW_{Range} ($PW_{\_min}$ to $PW_{\_max}$), as shown in Figure 16a. At initial powerup, C_{B1} is not yet fully charged, consequently, propagation delay (from HS_{IN}, or LS_{IN}, to SW) may increase, up to 250 ns. Only the first one, or two pulses may be affected. Figure 16b illustrates this behavior.

Figure 16a: Maximum and Minimum PWM Input Pulse Width ON or OFF duration to refresh internal gate drive capacitors



Recommended operation:
30 ns < ON duration < 200 µs
30 ns < OFF duration < 200 µs

Figure 16b: Behavior before complete charging of internal gate driver capacitors

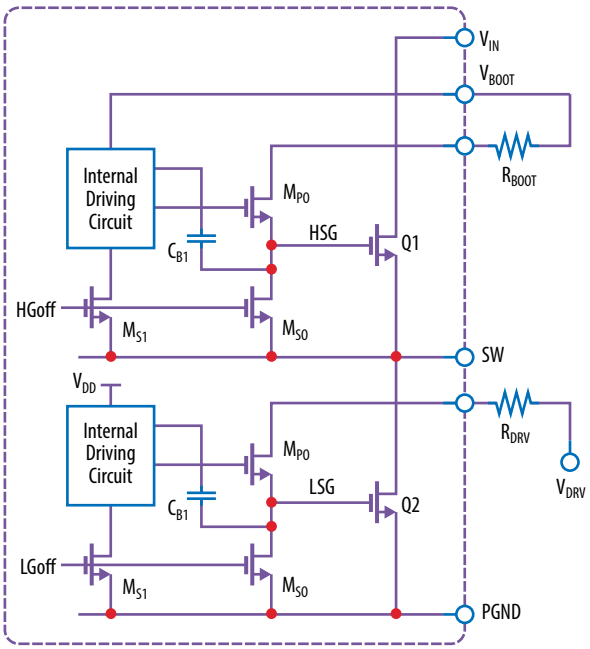


SW Node Switching Transients

The switching rate and transients at the output node, SW, are controlled by application topologies, resulting in hard or soft switching transitions. The more stressful hard switching transition needs to be controlled by a combination of tuning the gate drive turn-on and turn-off circuits for the HS FET (Q1) and LS FET (Q2), and minimizing the power loop parasitic inductances. The on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Switching times are tuned by external resistors, R_{DRV} and R_{BOOT}, as shown in Figure 17 to achieve SW switching rates of 10 to 50 V/ns spanning zero to full load current. The choice of switching rates is dictated by efficiency versus EMI mitigation. During HS FET (Q1) or LS FET (Q2) turn-on transitions with hard switching conditions, the fast di/dt of the HS FET or LS FET coupled with the power loop inductance ($V_{peak} = L_{power\ loop} \cdot di/dt$) would cause a transient over-voltage spike above V_{IN} or undervoltage spike below PGND. The EPC23104 pinouts for the three power bars (V_{IN}, SW, PGND) are coupled with the design of optimal layout techniques to achieve minimized power loop inductance.

Together with SW switching rate tuning by R_{DRV} and R_{BOOT}, the over-voltage spikes can be controlled to less than +10 V above rail and -10 V below ground during hard switching transitions.

Figure 17: Simplified circuit diagram of external tuning resistor, internal gate drivers and output FETs



The EPC90152 Evaluation Board provides guidelines for PCB layout to use the EPC23104 in DC-DC application circuits, while the EPC91104 is specific for motor drive. To control SW switching rate and transients, 2.2 Ω are used for both R_{DRV} and R_{BOOT} for high frequency DC-DC converter switching around 1 MHz and 10 Ω used for 100 kHz motor drive inverter applications.

Application	V_{DD}, V_{DRV} Capacitors	V_{BOOT} Capacitor	R_{BOOT}, R_{DRV} Resistors
DC DC	2.2 µF	100 nF	0 to 2.2 Ω
Motor Drive	2.2 µF	2.2 µF	10 Ω

Typical values of capacitors and resistors in application circuits using EPC23104.

Protection Circuits

The EPC23104 integrates driver protection circuits as well as power on reset (POR) circuits for V_{DD} and V_{BOOT}. These protection circuits allow for the proper operation of the driver as shown in the Truth Table, regardless of the power supply sequencing of V_{DRV} with respect to V_{IN}. This allows the system designer to use V_{IN} to power-up V_{DRV} without concerns on sequencing, as may be necessary in certain applications.

The Power On Reset (POR) circuit for the low-side internal V_{DD} supply will activate both the HS and LS logic paths when the V_{DD} voltage rises above the rising threshold V_{DD_POR+}. The logic paths will become inactive when the V_{DD} voltage falls by $V_{DD\_POR\_HYST}$ below the rising supply voltage threshold. The Power On Reset (POR) circuit for the high-side internal V_{BOOT} supply will activate the HS driver path only when the bootstrap supply voltage, V_{BOOT}, rises above the rising supply threshold of V_{BOOT_POR+}. The HS driver path will become inactive when the V_{BOOT} bootstrap voltage falls by $V_{BOOT\_POR\_HYST}$ below the rising supply threshold.

Logic Inputs

The EPC23104 IC is capable of interfacing to digital and analog controllers with 3.3 V or 5 V CMOS logic levels. The logic level translator at the frontend level- shifts the PWM signals, HS_{IN} and LS_{IN} respectively, to internal voltage levels that allow for proper operation of the IC.

When interfacing with analog controllers that output a 12 V PWM signal, a resistor network in series should be inserted to divide the voltage to acceptable V_{IH} level and limit the input current into the logic input pins HS_{IN} and LS_{IN} which are clamped to the V_{DD} supply by ESD protection network.

Separate and independent high-side (HS_{IN}) and low-side (LS_{IN}) logic control inputs allow external controllers to set fixed or adaptive deadtimes for optimal operating efficiency. Cross-conduction lockout logic commands both FETs off when both logic inputs are simultaneously high. Figure 18 shows how the logic inputs interact with each other. Here the timing diagram applies with the HS FET (Q1) and LS FET (Q2) in half-bridge configuration and current is in the positive direction going out of the half-bridge. When HS_{IN} and LS_{IN} are logic high at the same time, both Q1 and Q2 will shut off. A built-in deadtime of t_lockout is added, after which the current then commutes to Q2 in 3rd quadrant conduction and SW will be clamped at negative V_{SD} voltage of Q2.

Figure 18: EPC23104 Input-to-Output Timing Diagram

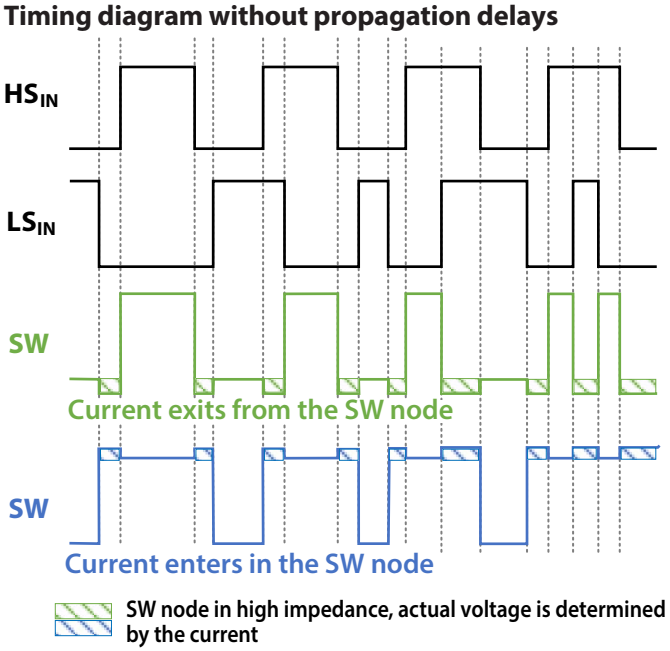


Figure 19 shows the effect of the input filter on the PWM inputs LS_{IN} and HS_{IN}. If the input pulse is smaller than t_{Filter} (15 ns typ), it does not pass through the filter and does not propagate to the respective power FET gate. Figure 20 shows the input filter linearity.

Figure 19: Input Filter Timing Diagram

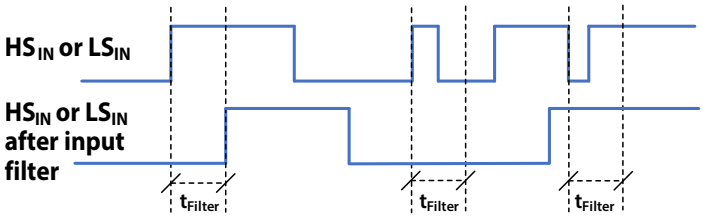


Figure 20: Input Filter Linearity

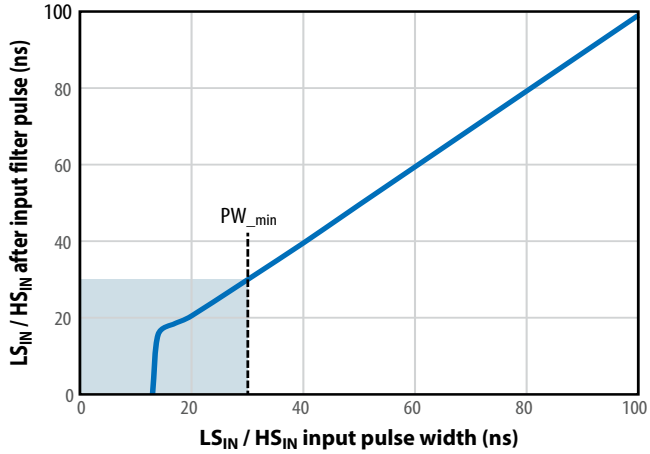
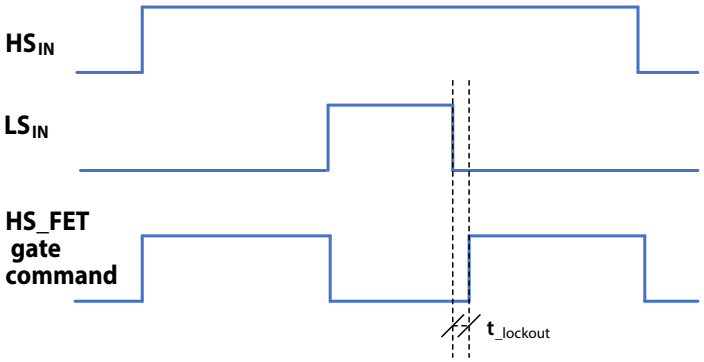
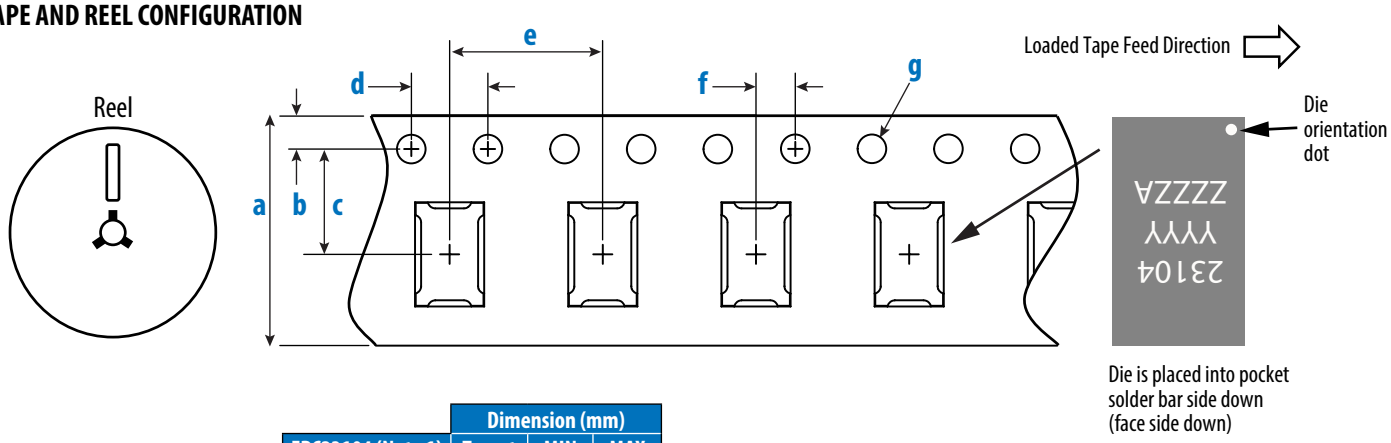


Figure 21 shows the effect of the cross-conduction lockout logic. If both inputs become active, an immediate turn-OFF signal is sent to the respective power FET gate. When the cross-conduction condition is removed (i.e., one of the inputs becomes inactive) the turn-ON signal is sent to the respective power FET gate after a $t_{\_lockout}$ delay.

Figure 21: Cross-Conduction Logic Timing Diagram



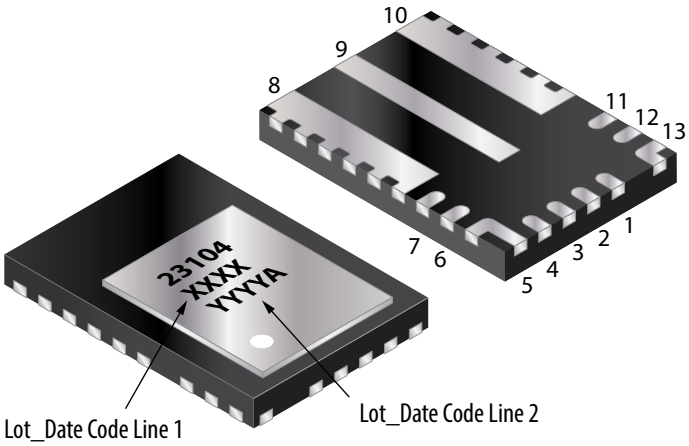
TAPE AND REEL CONFIGURATION



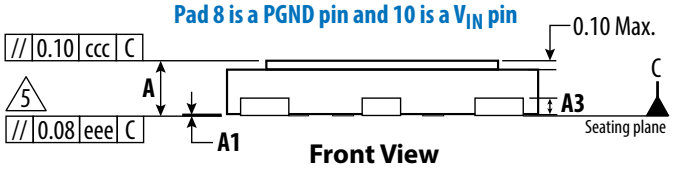
	Dimension (mm)		
EPC23104 (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

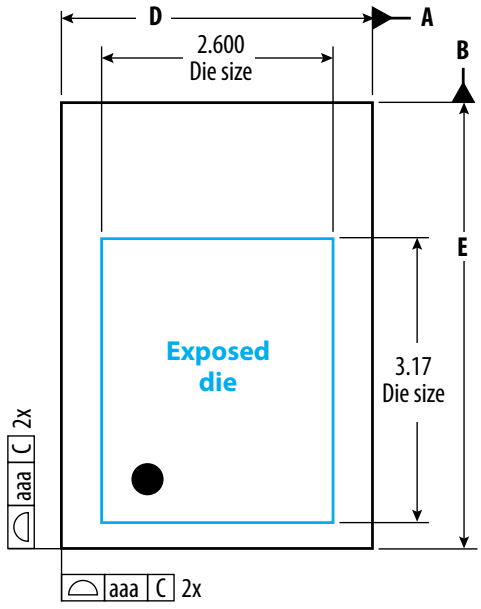
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.



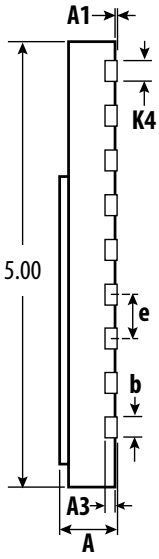
Pads 1-7, 11, 12 and 13 are IC pins;
Pad 9 is a SW pin ;
Pad 8 is a PGND pin and 10 is a V_{IN} pin



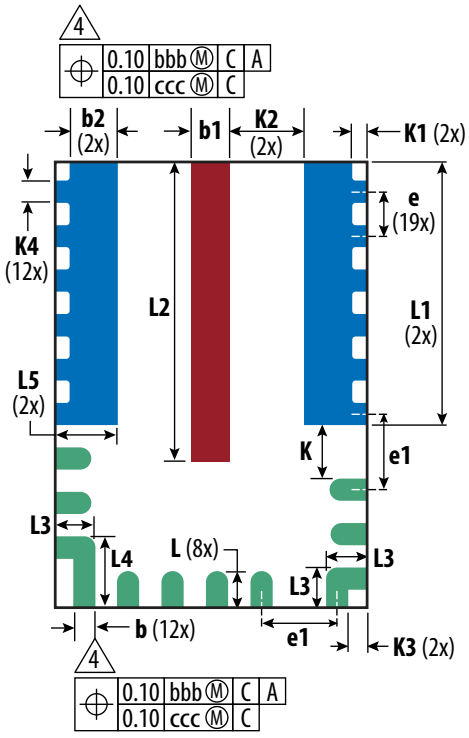
Front View



Top View



Side View 1



Bottom View

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.38	0.43	0.48	4
b2	0.49	0.54	0.59	
D	3.50 BSC			
E	5.00 BSC			
e	0.50 BSC			
e1	0.85 BSC			
K	0.60 REF			
K1	0.17 REF			
K2	0.825 REF			
K3	0.20 REF			
K4	0.25 REF			

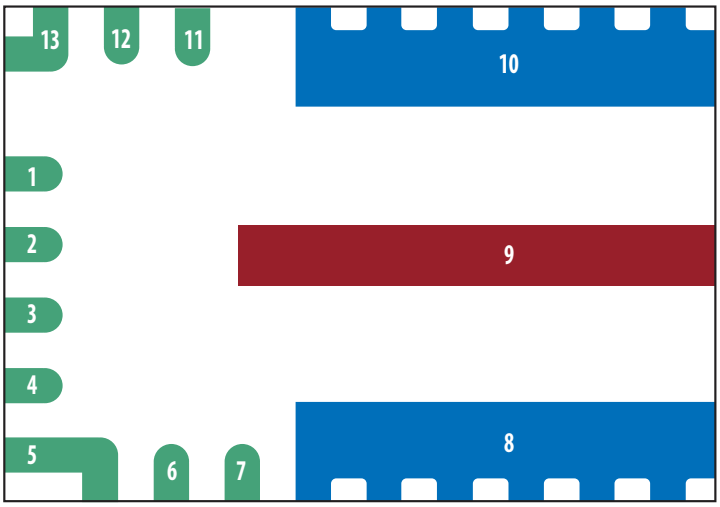
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
L	0.30	0.40	0.50	
L1	2.85	2.95	3.05	
L2	3.25	3.35	3.45	
L3	0.35	0.45	0.55	
L4	0.70	0.80	0.90	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		13		3
ND		6		5
NE		4		5
Notes		1, 2		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area
5. **ND** and **NE** refer to the number of terminals on each **D** and **E** side respectively.
6. Coplanarity applies to the terminals and all the other bottom surface metallization.

PACKAGE

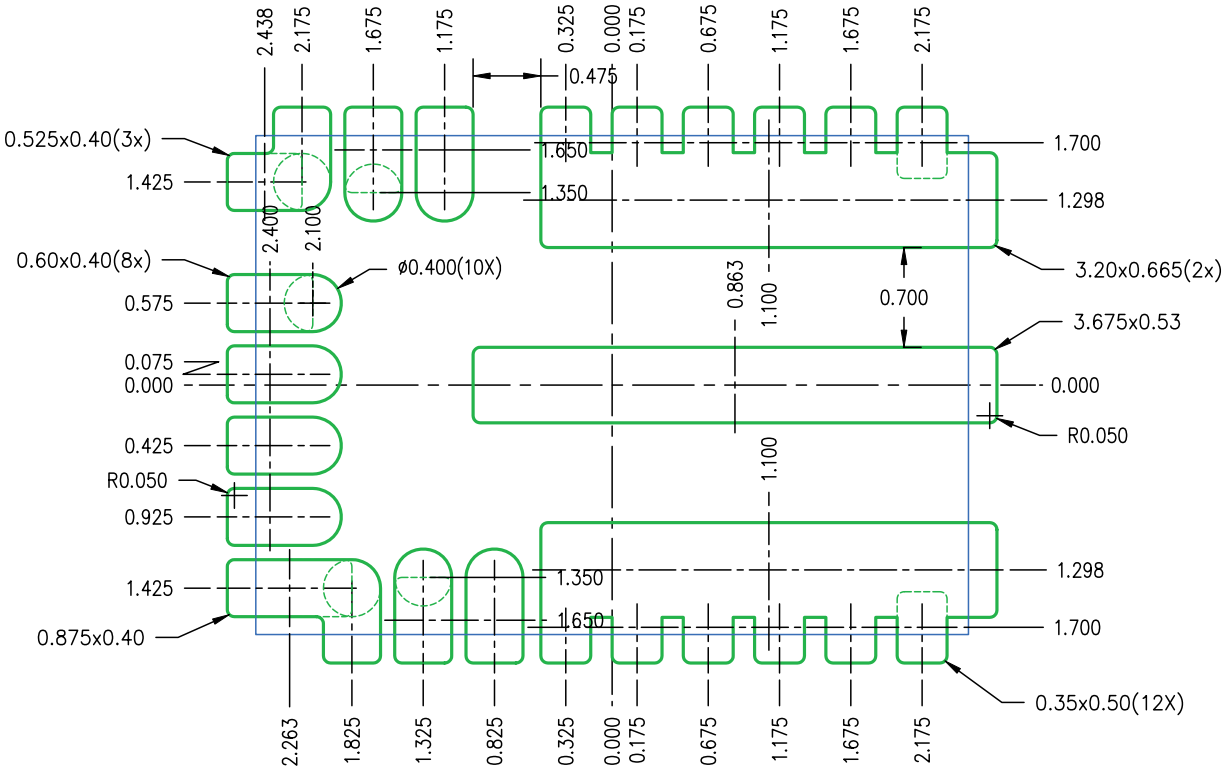
Transparent view



Pin	Description
1	HS_{IN}
2	LS_{IN}
3	STB
4	V_{DD}
5	V_{DRV}
6	R_{DRV}
7	AGND
8	PGND
9	SW
10	V_{IN}
11	V_{PHASE}
12	R_{BOOT}
13	V_{BOOT}

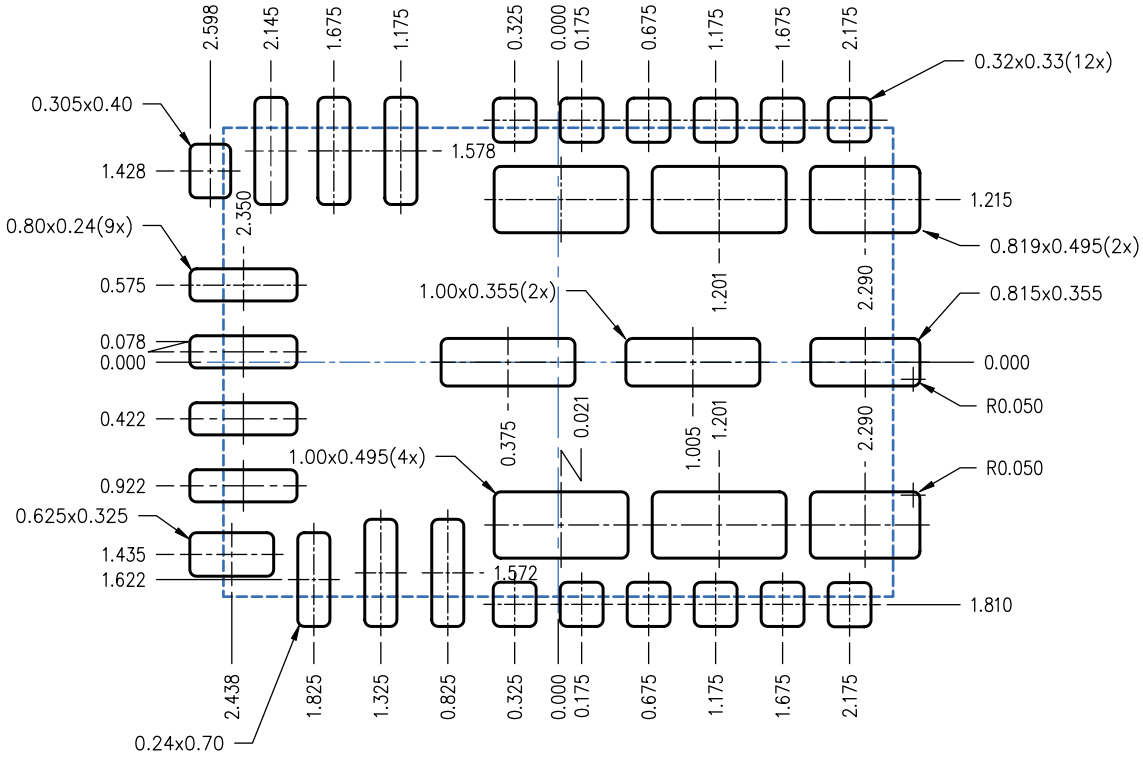
RECOMMENDED LAND PATTERN *(units in mm)*

Land pattern is solder mask defined.



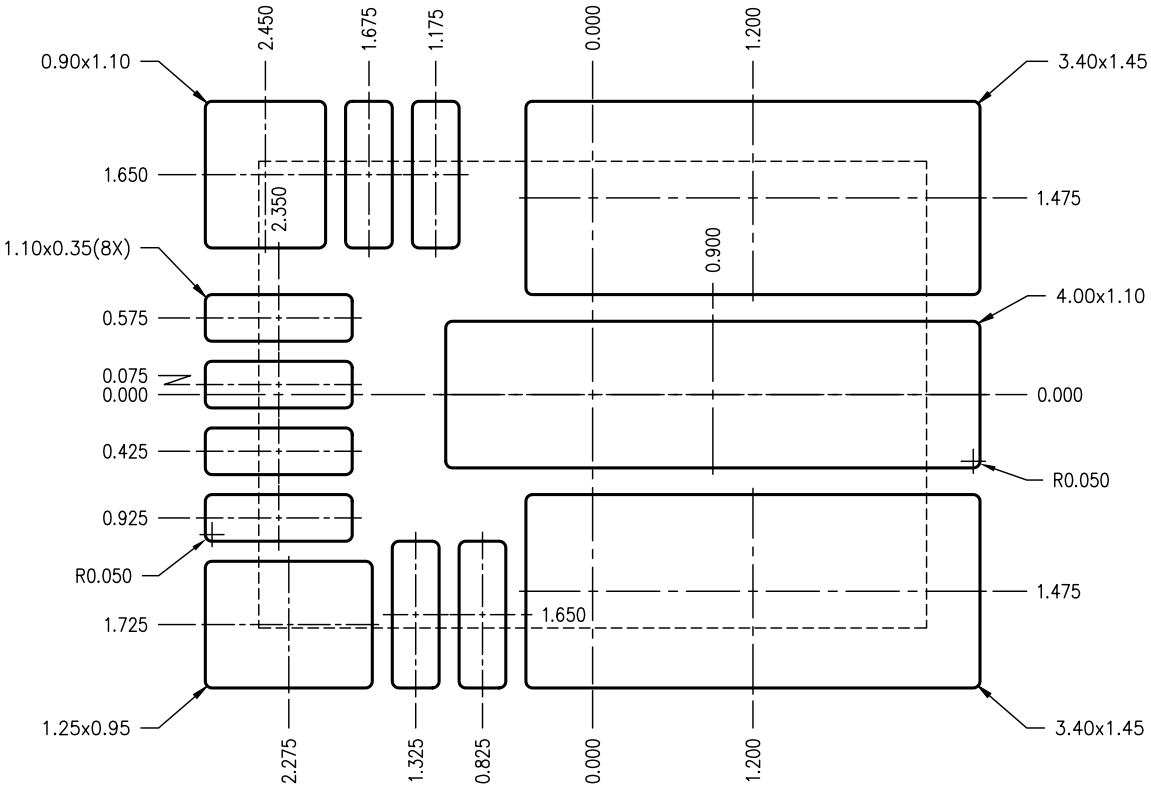
RECOMMENDED STENCIL *(units in mm)*

Recommended stencil should be 100 µm (4 mil) thick, must be laser cut, openings per drawing.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.
EPC has used this stencil design during tests.



RECOMMENDED COPPER LAYER *(units in mm)*

Copper layout provided as typical example layout.



Change Log

STATUS	VERSION	DATE	REMARK
2.1	Production	2 October 2025	Production release