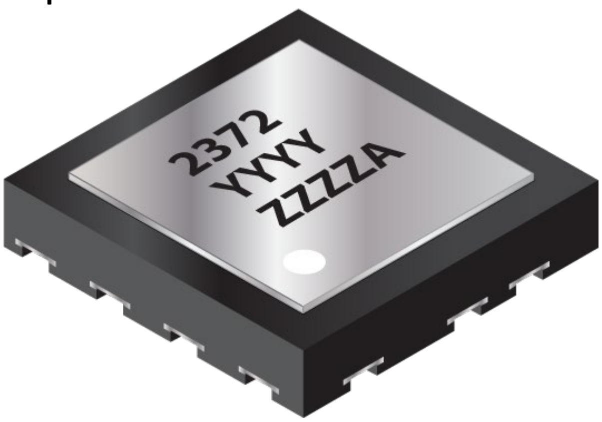
Preliminary

Die photo:



Summary:

e-GaN® 25 V, 101 A, 0.37 mΩ typ Surface Mount
Package size 3.3mm x 3.3mm

Features:

- Ultra-low Q_G for High Frequency
- PQFN Package with Backside Thermal Pad
- No reverse recovery

Application:

- High Performance, high power-density DC-DC Conversion
- High-Frequency DC-DC Converters
- Synchronous Rectifiers
- Point of Load Buck Convertor

Description:

EPC's eGaN® power switching transistors have been specifically designed for critical applications in DC-DC conversion. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging. EPC2372 has been specifically designed for synchronous rectifier applications on the secondary side of a 48V-8 or 5 V LLC converter, where it brings an industry leading low $R_{DS(on)}$ xQ_G figure of merit and enables higher frequency and higher efficiency operation. EPC2372 is also for Point of Load Buck converters.

Maximum Ratings			
Symbol	**Parameter-Conditions**	**Value**	**Units**
V_{DS}	Drain-to-Source Voltage	25	V
	Drain-to-Source Voltage (up to 10,000 5ms pulses at 150˚C)	30	
I_D	Continuous Drain Current at V_{GS} = 5 V	101	A
I_{DM}	Pulsed (25˚C, T_{PULSE} = 300 µs)	699	
V_{GS}	Gate-to-Source Voltage	6	V
V_{GS}	Gate-to-Source Voltage	-4	V
T_J,	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	C

Static Characteristics (T_J= 25˚C unless otherwise noted)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0 V, I_D = TBD	25			V
I_{DSS}	Drain to Source Leakage	V_{DS} = 25 V, V_{GS} = 0 V		0.1		mA
		V_{DS} = 25 V, V_{GS} = 0 V, T_J = 125°C			1	
I_{GSS}	Gate to Source Forward Leakage	V_{GS} = 5 V		0.1		mA
	Gate to Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.5		
	Gate to Source Reverse Leakage	V_{GS} = -2 V		300		µA
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 24 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain to Source Resistance	V_{GS} = 5 V, I_D = 20A		0.37		mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

All measurements were done with substrate shorted to source.
Defined by design. Not subject to production test.

Dynamic Characteristics #. (T_J= 25˚C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 12 V, V_{GS} = 0 V		4224		pF
C_{RSS}	Reverse Transfer Capacitance			172		
C_{OSS}	Output Capacitance			2143		
Q_G	Total Gate Charge	V_{DS} = 12 V, V_{GS} = 5 V, I_D = 20A		27		nC
Q_G Sync	Total Gate Charge Synchronous	V_{DS} = 0 V, V_{GS} = 5 V, I_D = 0A		24		
Q_{GS}	Gate-to-Source Charge	V_{DS} = 12 V, I_D = 20A		7		
Q_{GD}	Gate-to-Drain Charge			4		
Q_{OSS}	Output Charge	V_{DS} = 12 V, V_{GS} = 0 V		29		
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.
Defined by design. Not subject to production test.

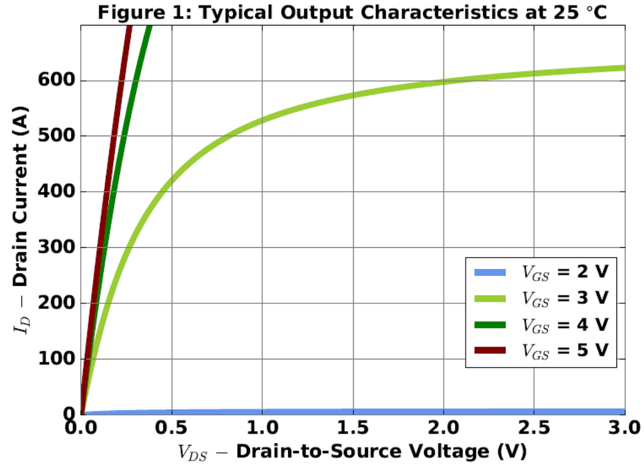


Figure 1: Typical Output Characteristics at 25 °C

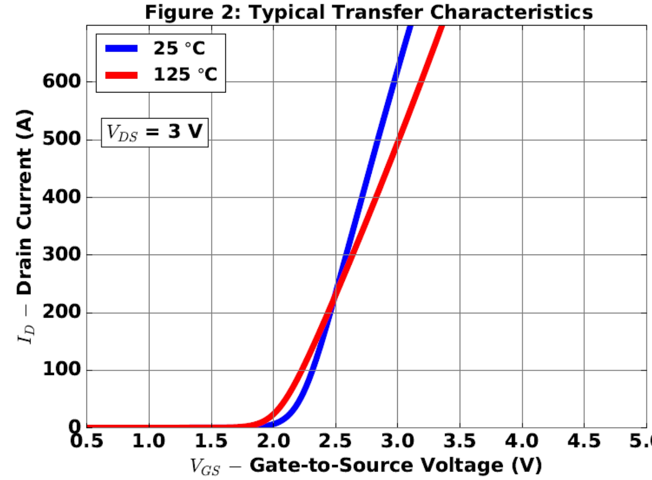


Figure 2: Typical Transfer Characteristics

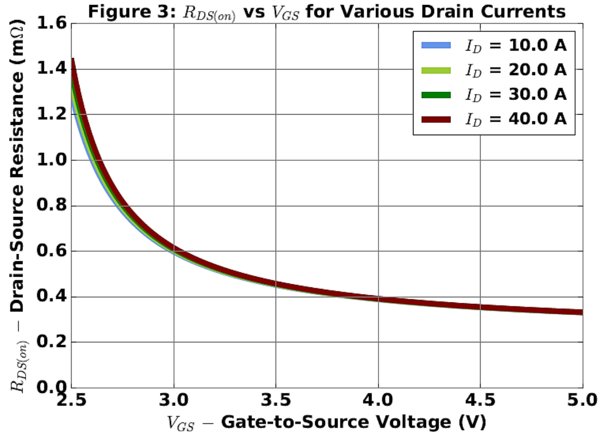


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

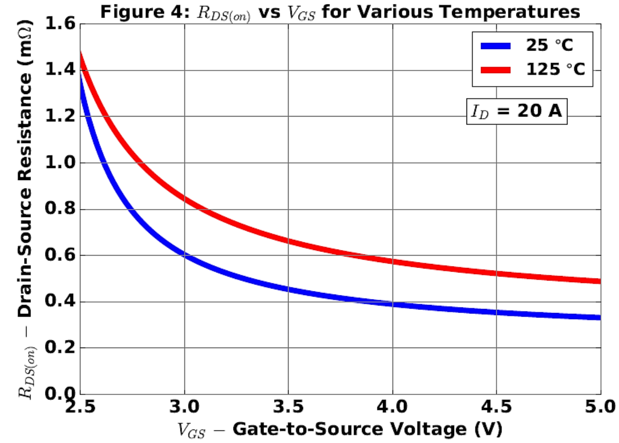


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

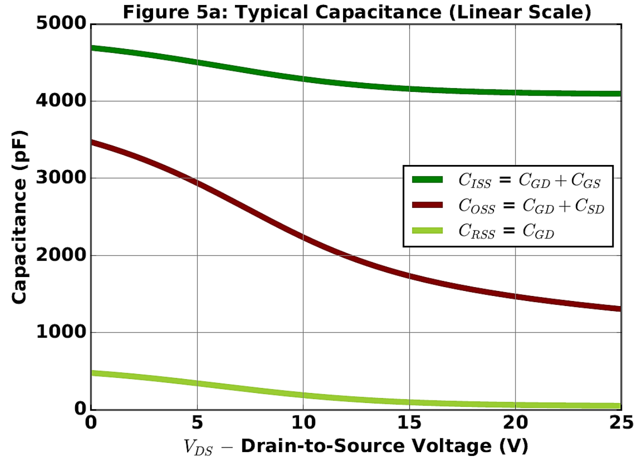


Figure 5a: Typical Capacitance (Linear Scale)

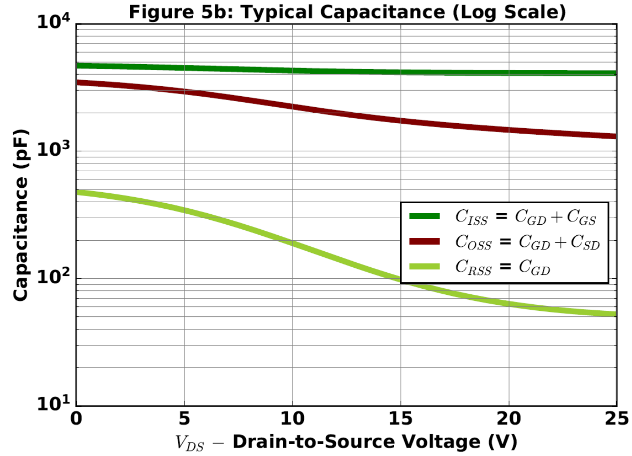


Figure 5b: Typical Capacitance (Log Scale)

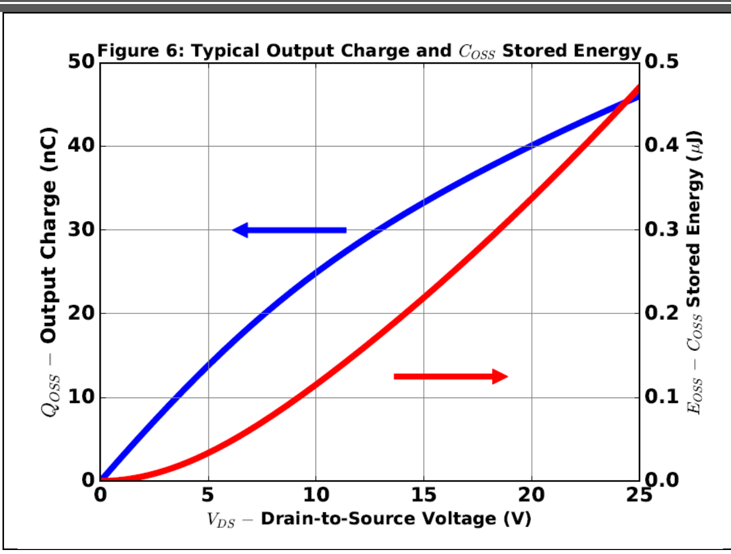


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

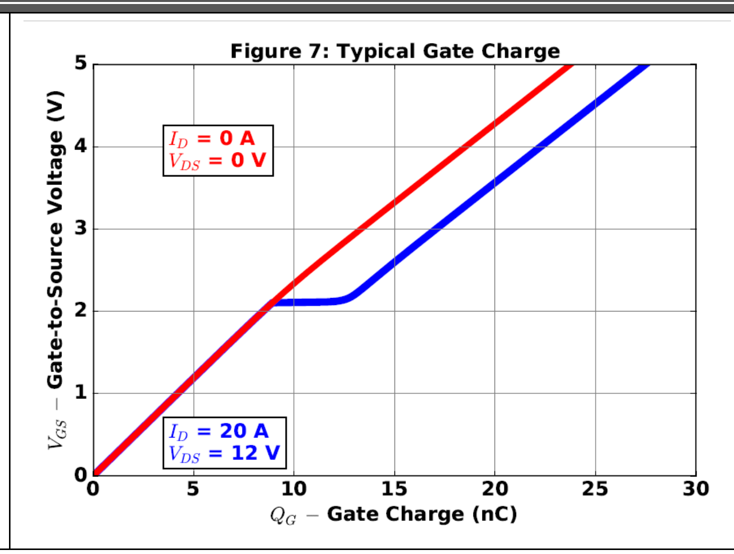


Figure 7: Typical Gate Charge

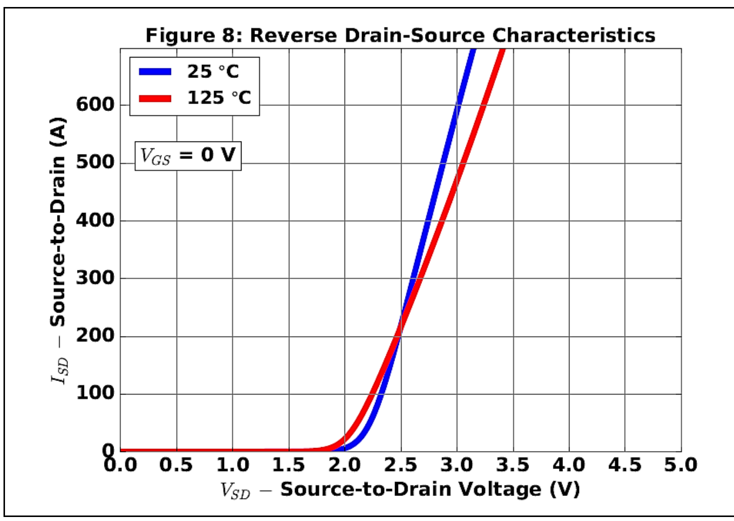


Figure 8: Reverse Drain-Source Characteristics

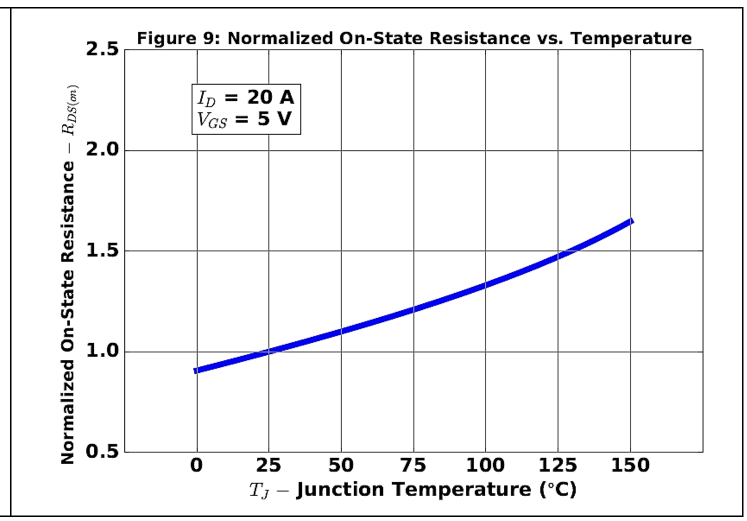


Figure 9: Normalized On-State Resistance vs. Temperature

Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

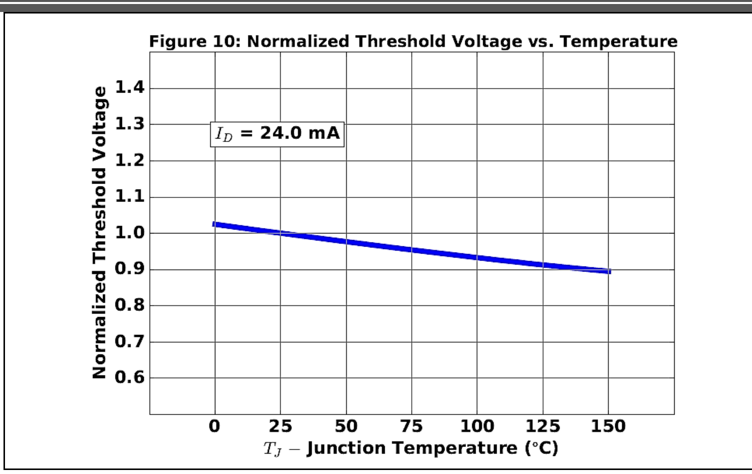
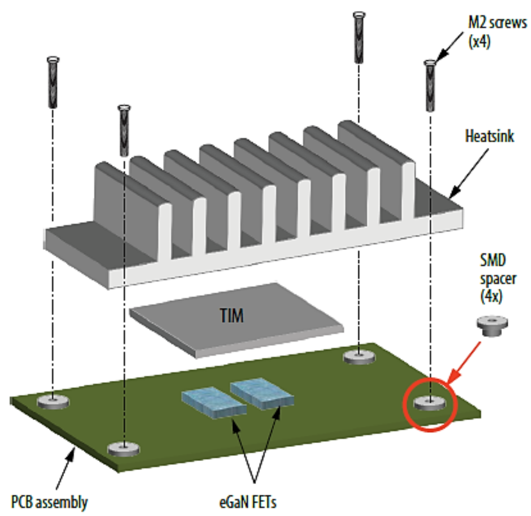


Figure 10: Normalized Threshold Voltage vs. Temperature
Normalized Threshold Voltage
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
I_D = 24.0 mA
0
25
50
75
100
125
150
T_J − Junction Temperature (°C)

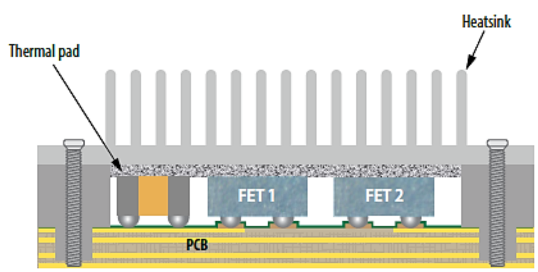
TYPICAL THERMAL CONCEPT

The EPC2372 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf (epc-co.com).](epc-co.com)



Exploded view of heatsink assembly using screws

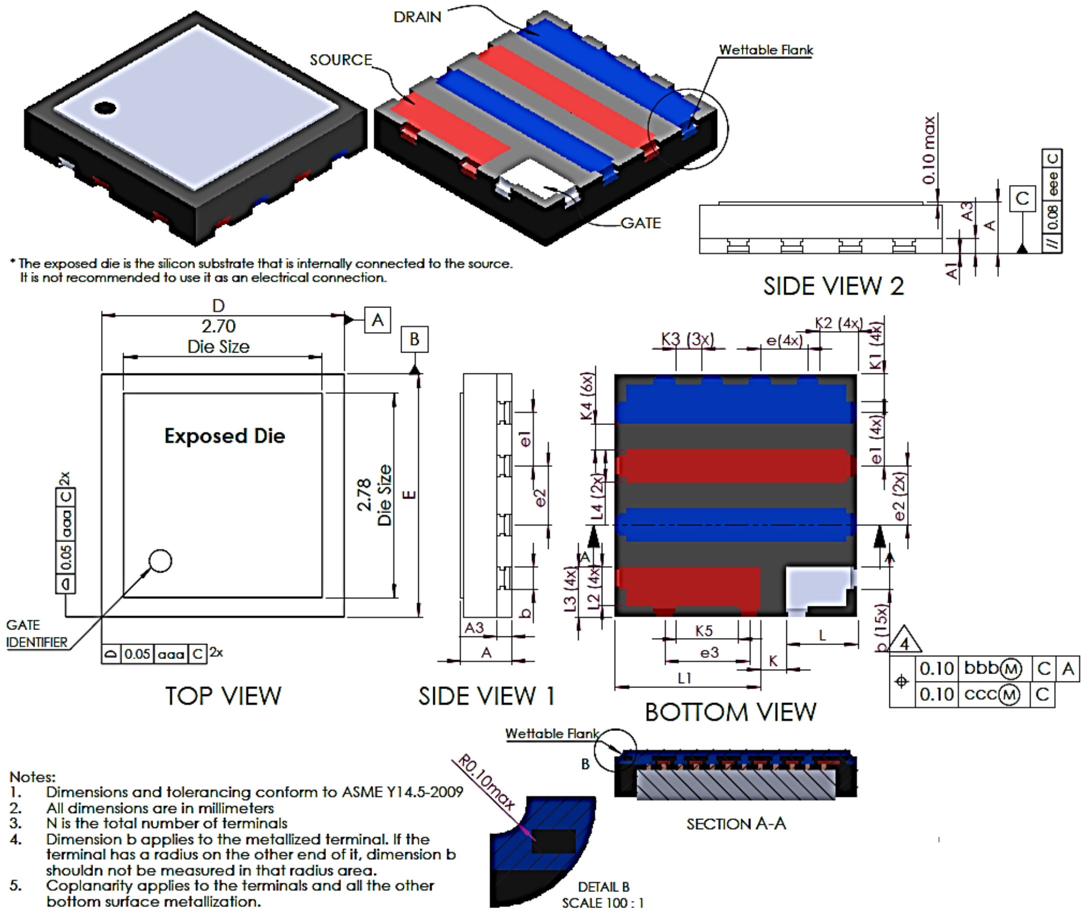


A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the GaN FET Thermal Calculator (epc-co.com)

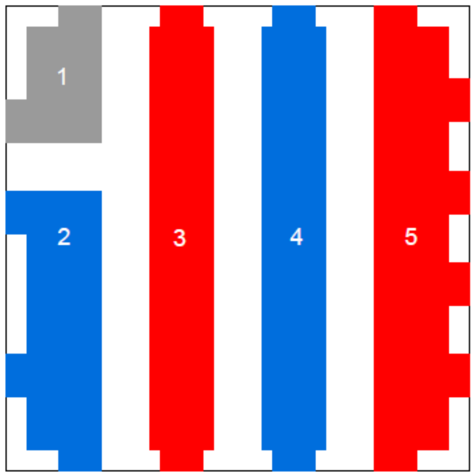
PACKAGE OUTLINE AND DIMENSIONS



DIMENSION (mm)				
SYMBOL	MIN	NOMINAL	MAX	NOTE
A	-	-	0.70	
A1	0.00	0.02	0.05	
A3	-	-	0.25	
D	3.20	3.30	3.40	
b	0.25	0.30	0.35	4
E	3.20	3.30	3.40	
e		0.650 BSC		
e1		0.725 BSC		
e2		0.800 BSC		
e3		1.150 BSC		
L	0.874	0.974	1.074	
L1	1.876	1.976	2.076	
L2	0.425	0.525	0.625	
L3	0.575	0.675	0.775	
L4	0.350	0.450	0.550	
K		0.350 REF		
K1		0.375 REF		
K2		0.525 REF		
K3		0.350 REF		
K4		0.350 REF		
K5		0.851 REF		
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		5		3

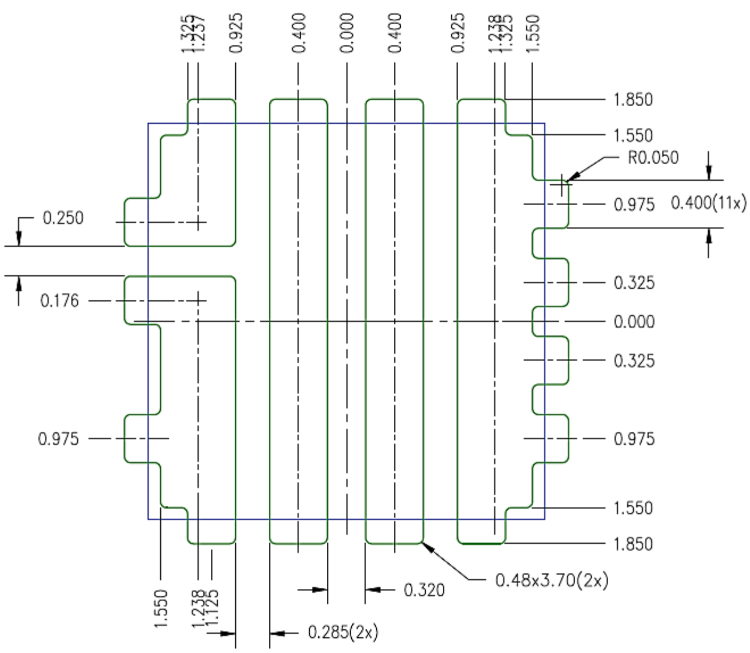
Notes:
1. Dimensions and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension b shouldn not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

TRANSPARENT VIEW:



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain

RECOMMENDED LAND PATTERN *(units in mm)*:

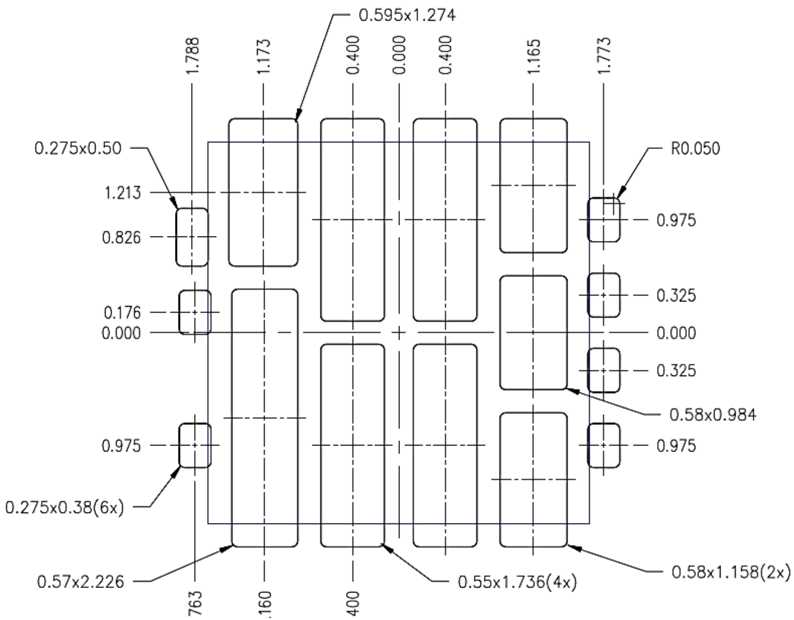


Legend:
Part outline
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING *(units in mm)*:

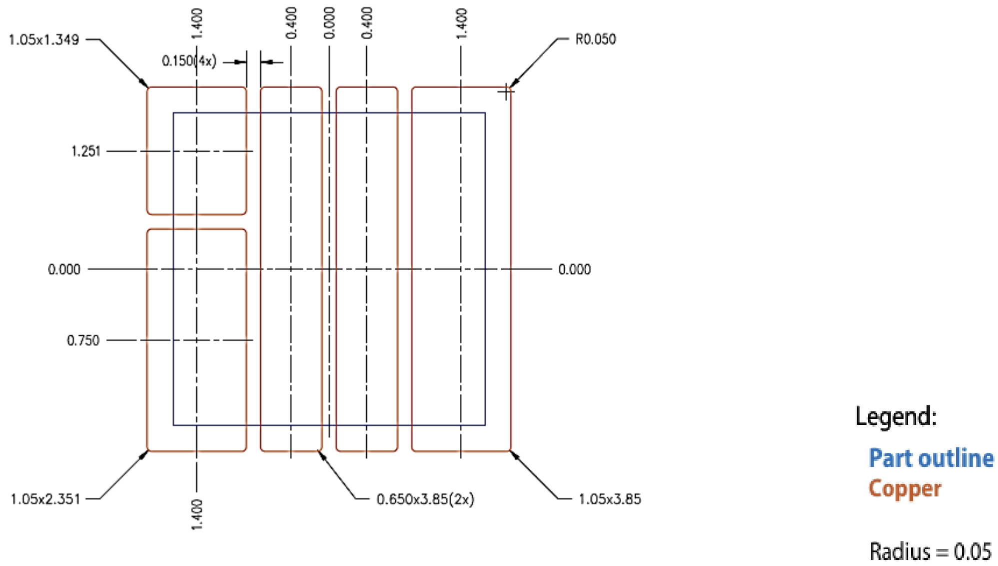


Legend:
Part Outline
Stencil Opening

The recommended stencil should be 4mils (100um) thick, must be laser cut, and have openings per drawing.
Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.

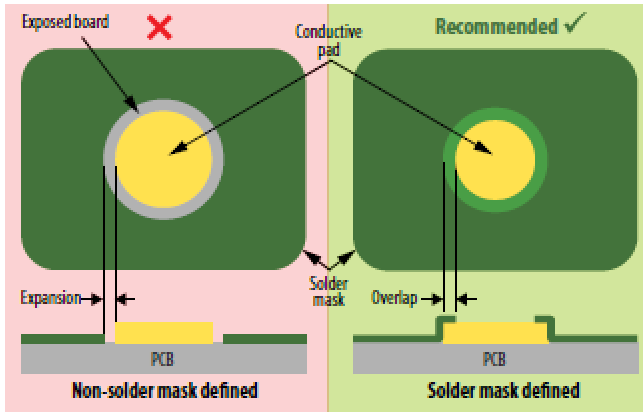
Split stencil design can be provided upon request, but EPC has tested this stencil design and not found

RECOMMENDED COPPER DRAWING *(units in mm)***:**

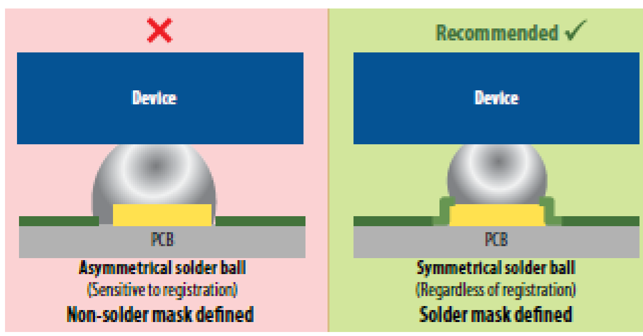


ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.



Solder mask defined versus non-solder mask defined pad



Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)

Prior to final qualification and production release, engineering samples might not meet all datasheet specifications.

Revised August, 2025