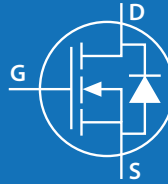


EPC2373 – Enhancement Mode Power Transistor

V_{DS} , 15 V

$R_{DS(on)}$, 0.5 mΩ typ

PRELIMINARY



Revised January 15, 2026

General Description

EPC's eGaN® power switching HEMTs have been specifically designed for critical applications in DC-DC conversion. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging.

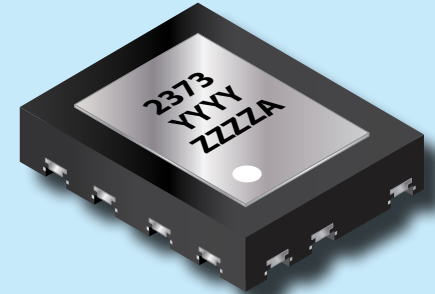
Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source



Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	15	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	18	
I_D	Continuous ($T_J < 125^\circ\text{C}$)	88	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	447	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.8	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	54	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90174 EVB)	26	



EPC2373

Package size: 3.3 x 2.6 mm

Features

- Ultra-low Q_G
- Very low on-resistance $R_{DS(on)}$
- Logic level
- Light weight
- PQFN package with backside thermal pad

Applications

- High speed DC-DC conversion
- Synchronous rectification
- Servers
- Artificial intelligence

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2373>

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = \text{TBD}$	15			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}$		100		μA
		$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, T_J = 125^\circ\text{C}$				
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		25		μA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$				
	Gate-to-Source Reverse Leakage	$V_{GS} = -2\text{ V}$		200		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 15\text{ mA}$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		0.5		$\text{m}\Omega$
V_{SD}	Source-to-Drain Forward Voltage [#]	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$		1.4		V

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}$		4153		pF
C_{RSS}	Reverse Transfer Capacitance			77		
C_{OSS}	Output Capacitance			964		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related	$V_{DS} = 0\text{ to }8\text{ V}, V_{GS} = 0\text{ V}$		1312		pF
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related			1474		
Q_G	Total Gate Charge	$V_{DS} = 8\text{ V}, V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		23		nC
$Q_{G_{sync}}$	Total Gate Charge	$V_{DS} = 0\text{ V}, V_{GS} = 5\text{ V}, I_D = 0\text{ A}$		21		
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 8\text{ V}, I_D = 20\text{ A}$		8.8		
Q_{GD}	Gate-to-Drain Charge			1.5		
$Q_{G(TH)}$	Gate Charge at Threshold			6.4		
Q_{OSS}	Output Charge		$V_{DS} = 8\text{ V}, V_{GS} = 0\text{ V}$		12	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

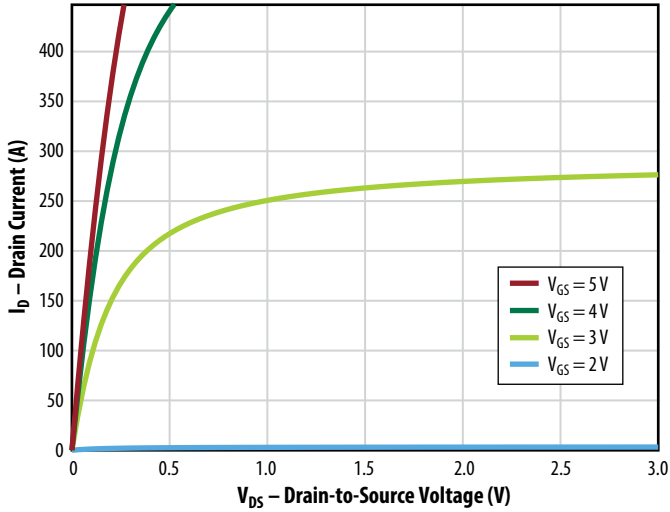


Figure 2: Typical Transfer Characteristics

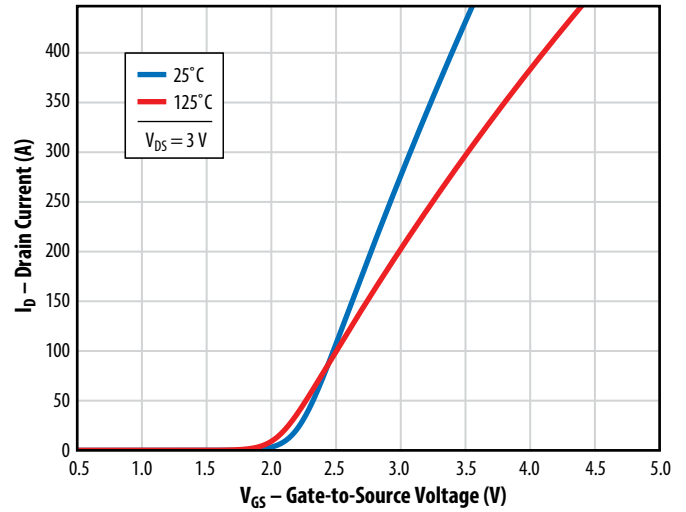


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

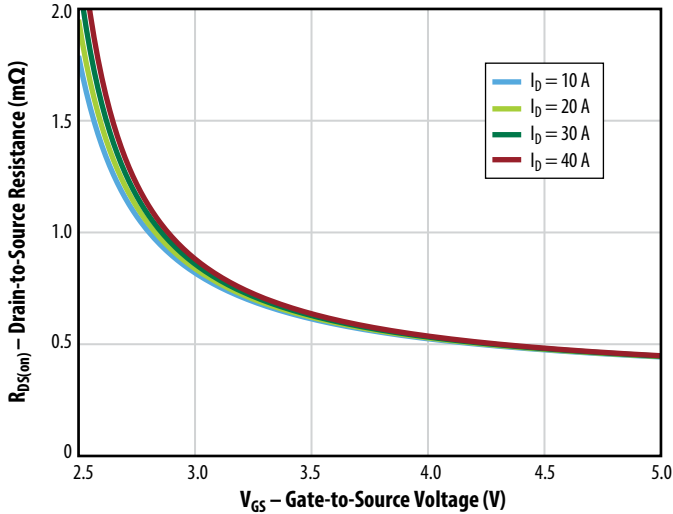


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

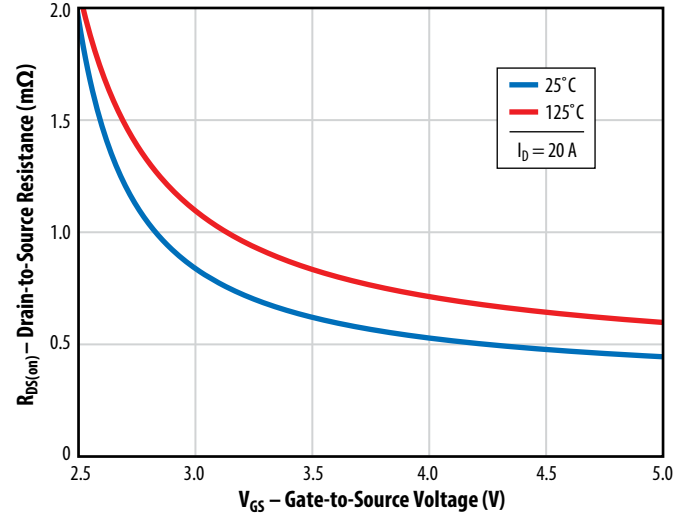


Figure 5a: Typical Capacitance (Linear Scale)

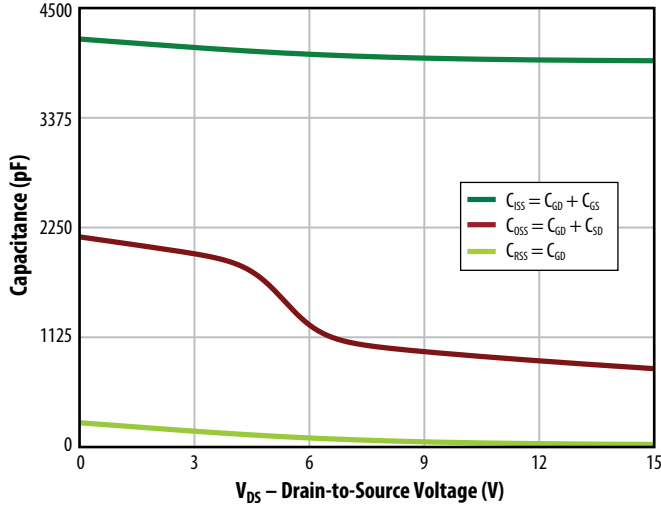


Figure 5b: Typical Capacitance (Log Scale)

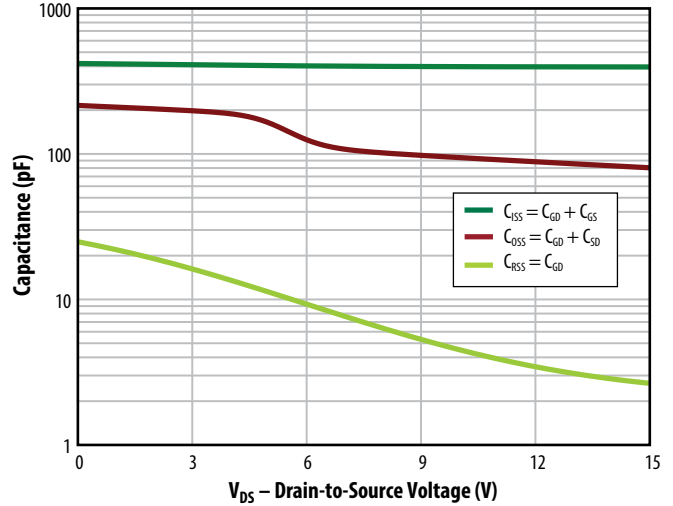


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

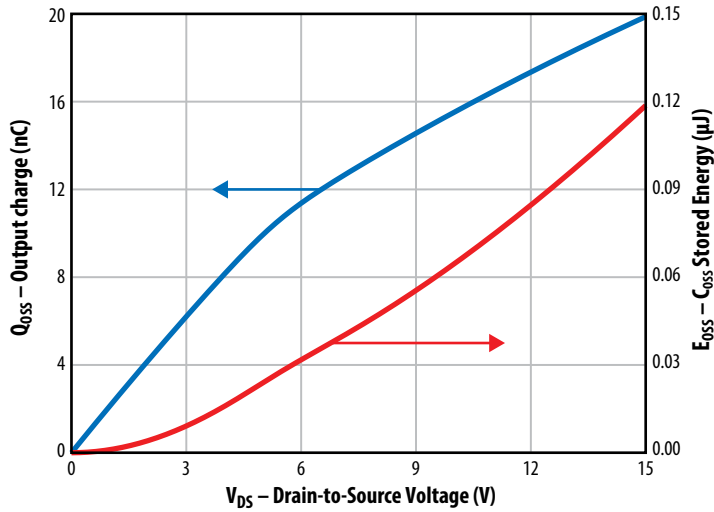


Figure 7: Typical Gate Charge

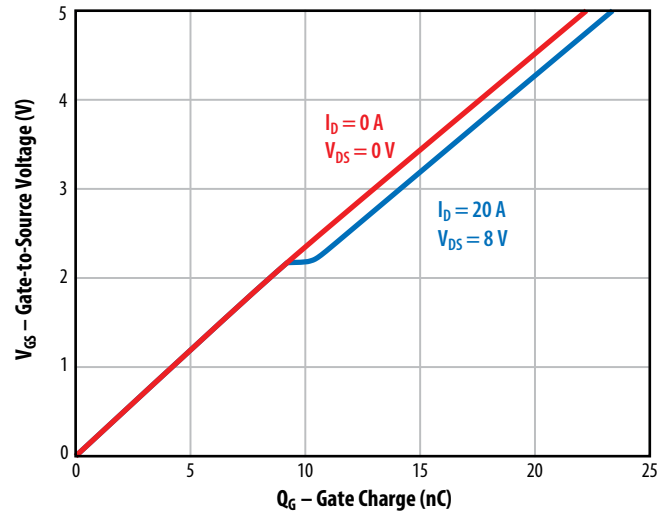
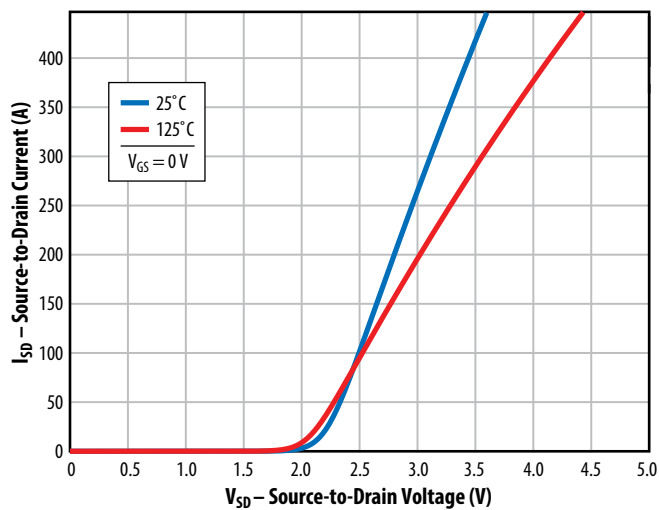


Figure 8: Typical Reverse Drain-Source Characteristics



Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0V for OFF

Figure 9: Typical Normalized On-State Resistance vs. Temp.

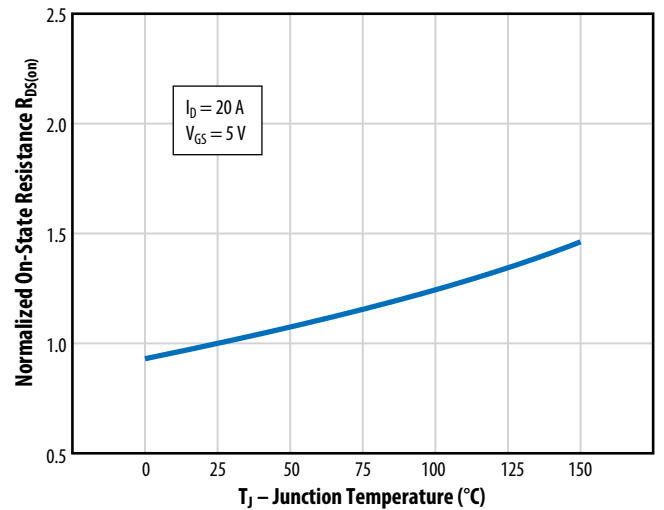


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

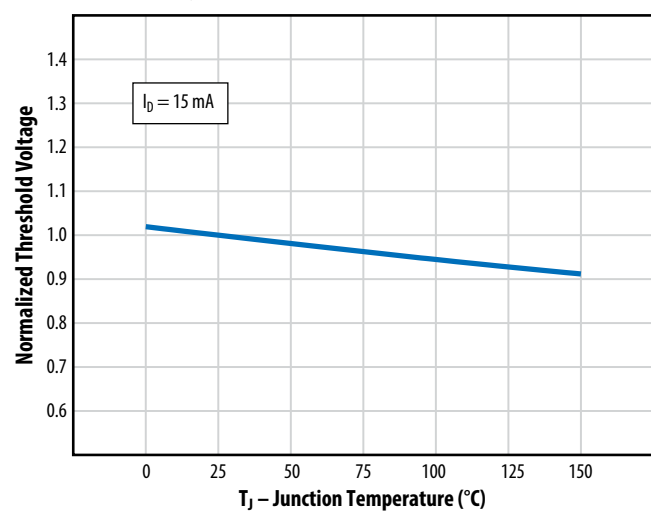


Figure 11: Safe Operating Area

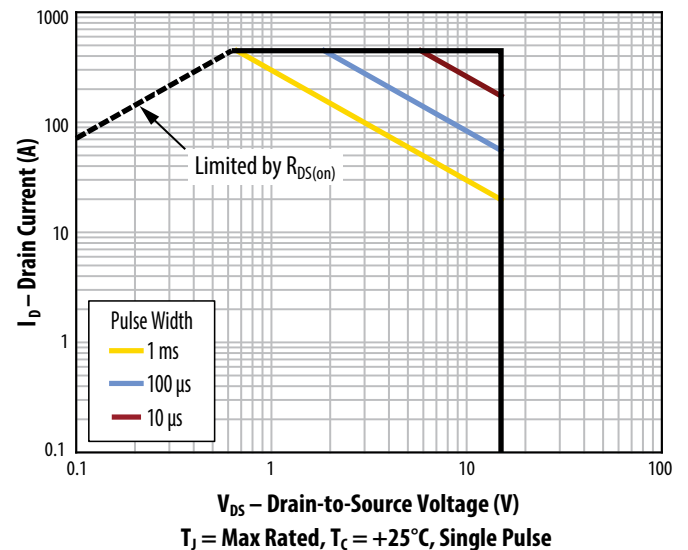
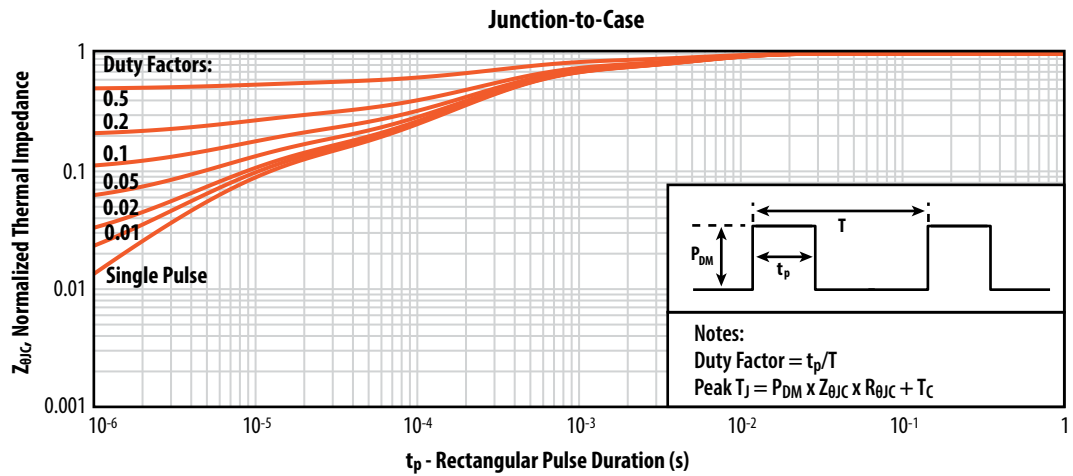
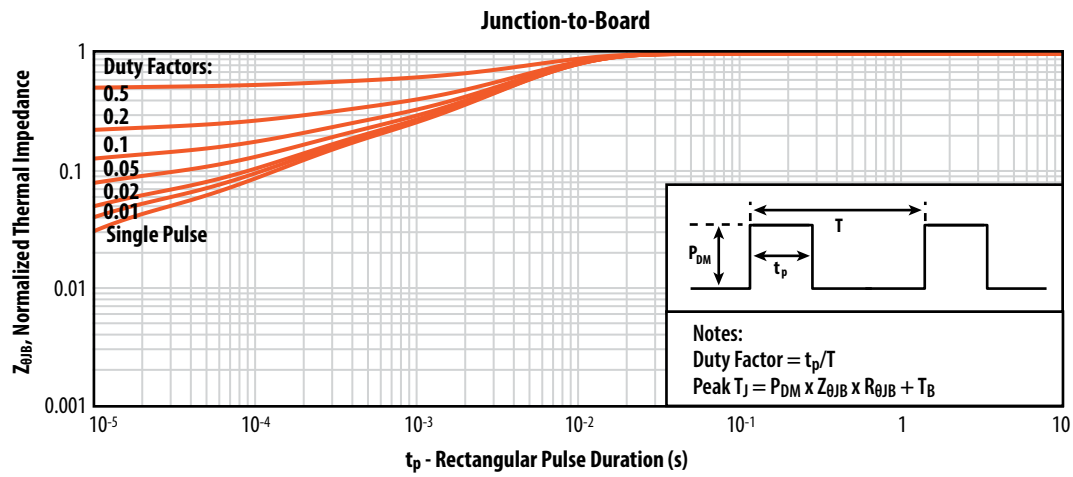


Figure 12: Typical Transient Thermal Response Curves



TYPICAL THERMAL CONCEPT

The EPC2373 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. **Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.**

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

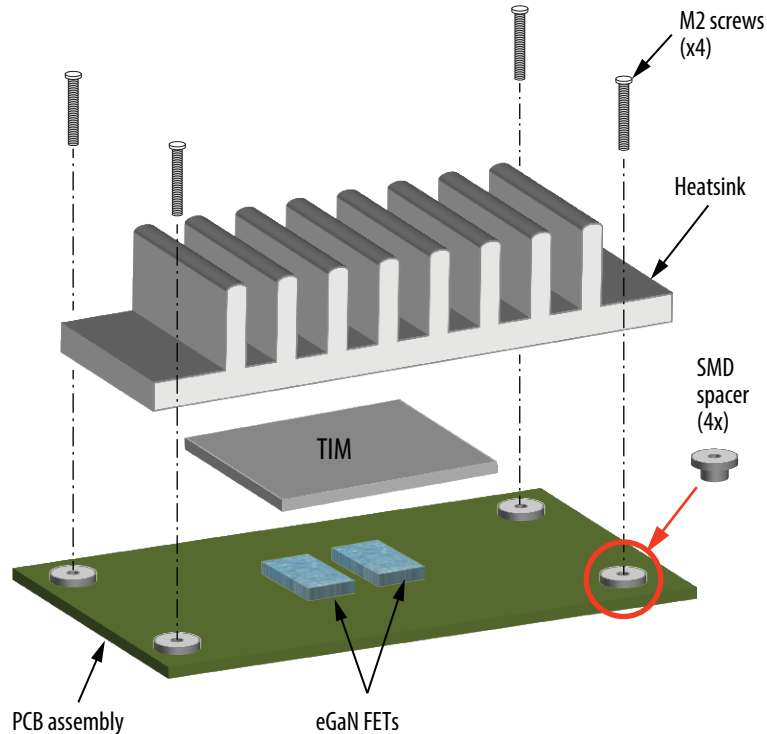


Figure 13: Exploded view of heatsink assembly using screws

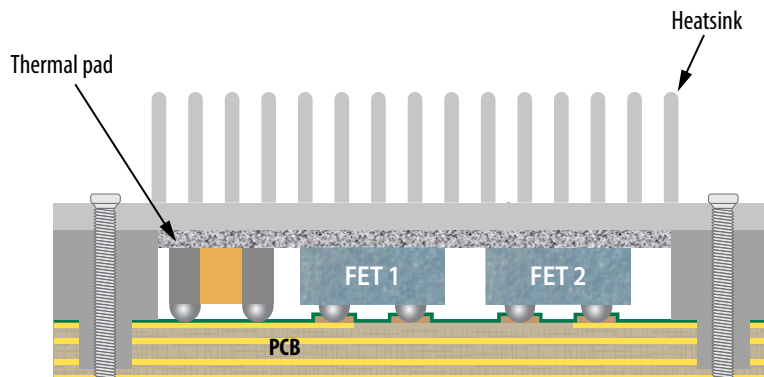


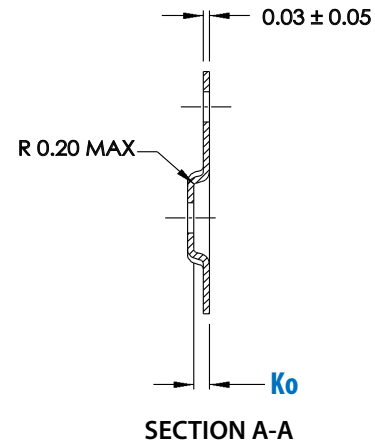
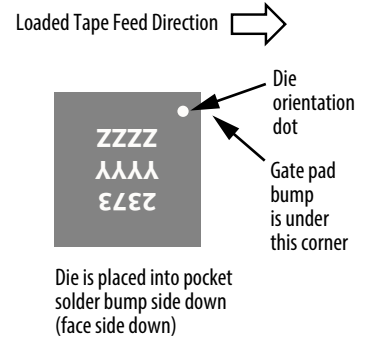
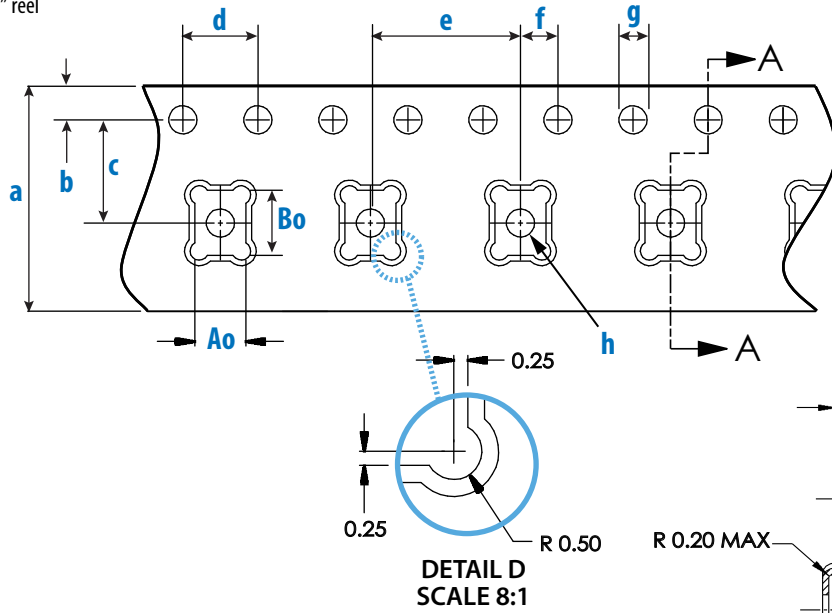
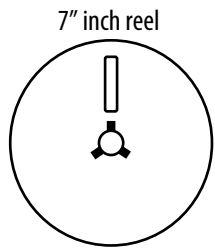
Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

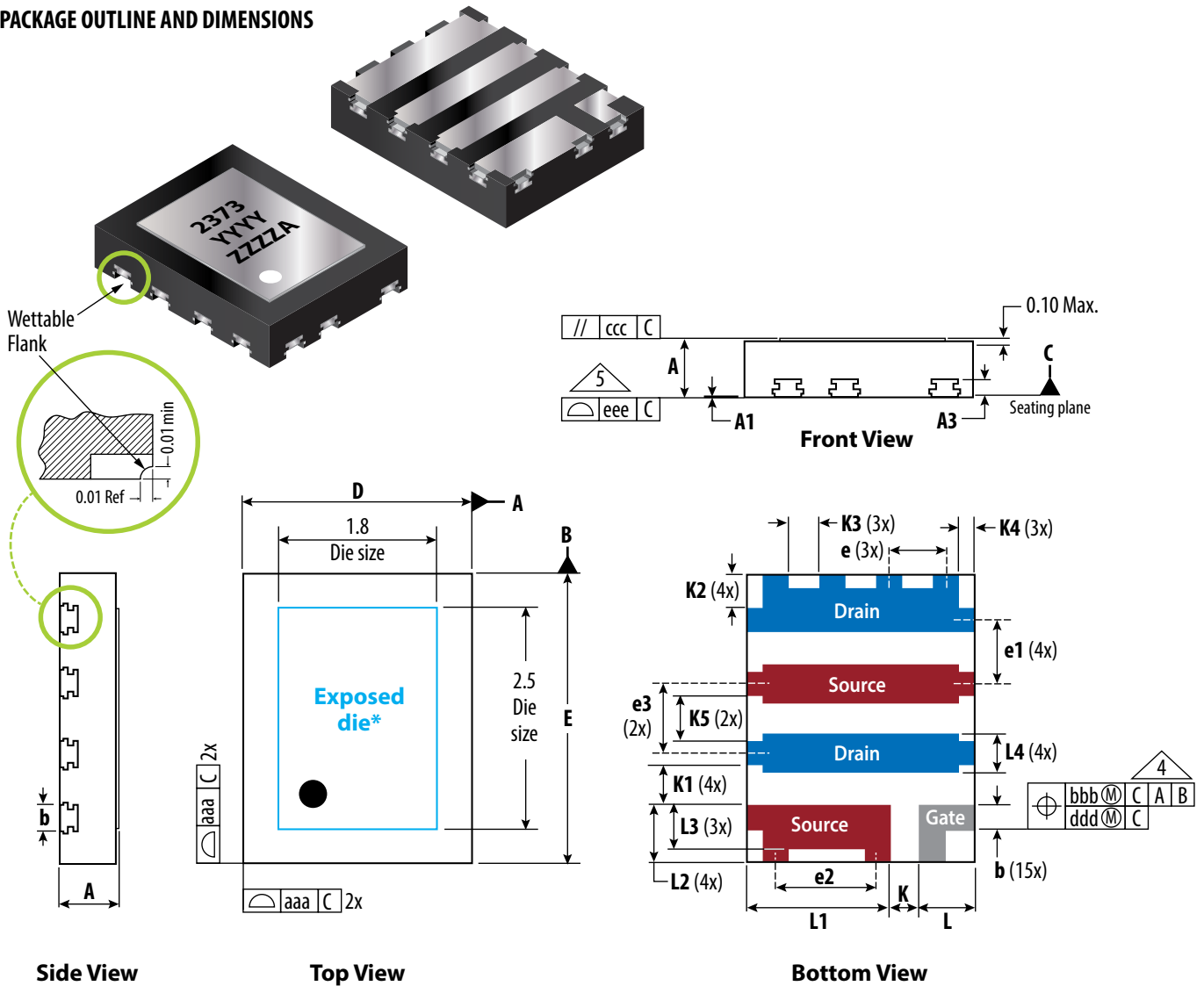


EPC2373 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.60
Ao	2.73	2.63	2.83
Bo	3.47	3.37	3.57
Ko	0.78	0.68	0.88

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

PACKAGE OUTLINE AND DIMENSIONS



*The exposed die is the silicon substrate that is internally connected to the source. It is not recommended to use it as an electrical connection

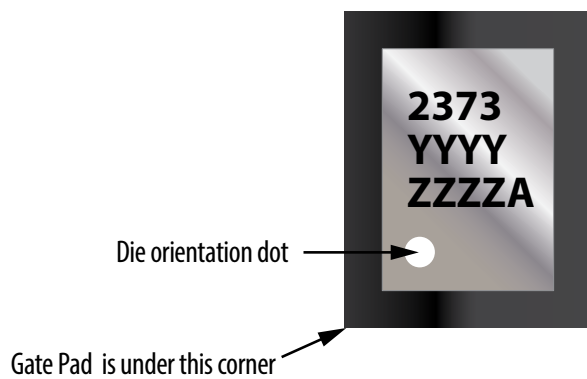
SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
A			0.70	
A1	0.00	0.02	0.05	
A3	0.20 Ref			
b	0.25	0.30	0.35	4
D	2.50	2.60	2.70	
E	3.20	3.30	3.40	
e		0.65 BSC		
e1		0.725 BSC		
e2		1.151 BSC		
e3		0.80 BSC		
L	0.524	0.624	0.724	
L1	1.526	1.626	1.726	
L2	0.575	0.675	0.775	
L3	0.425	0.525	0.625	
L4	0.350	0.450	0.550	

SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
K		0.350 Ref		
K1		0.425 Ref		
K2		0.375 Ref		
K3		0.350 Ref		
K4		0.175 Ref		
K5		0.500 Ref		
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		5	3	
Notes		1, 2		

Notes:

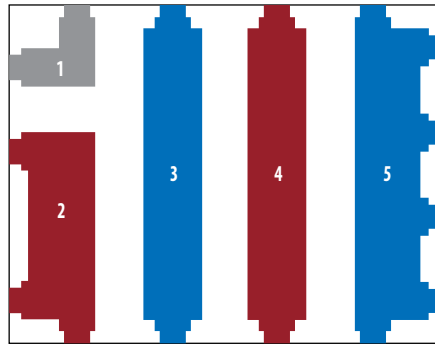
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

Part Marking



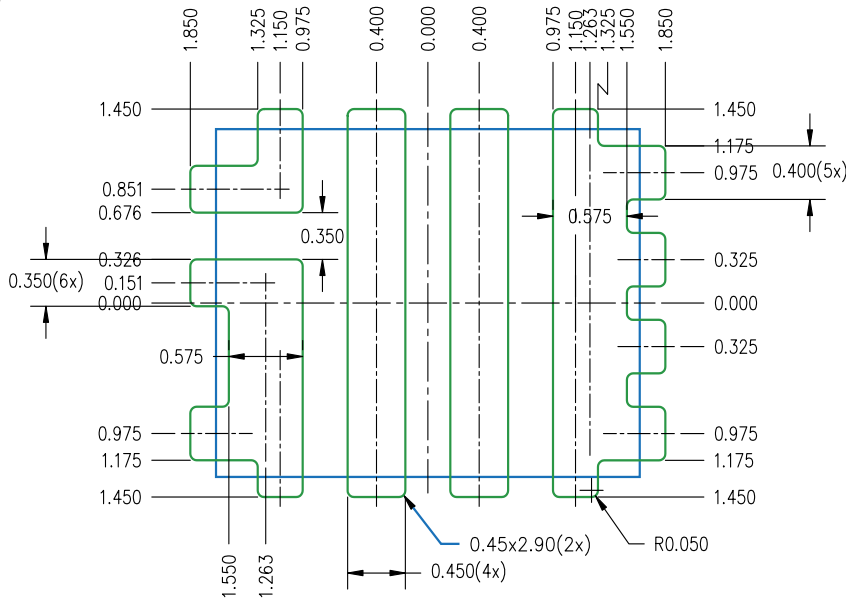
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2373	2373	YYY Y	ZZZA

TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain

RECOMMENDED LAND PATTERN
(units in mm)



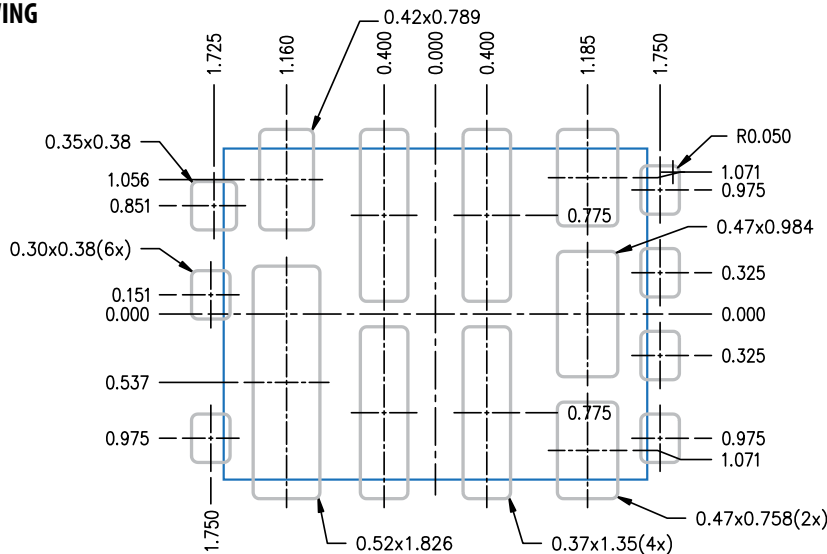
Legend:

Part outline
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING
(units in mm)



Legend:

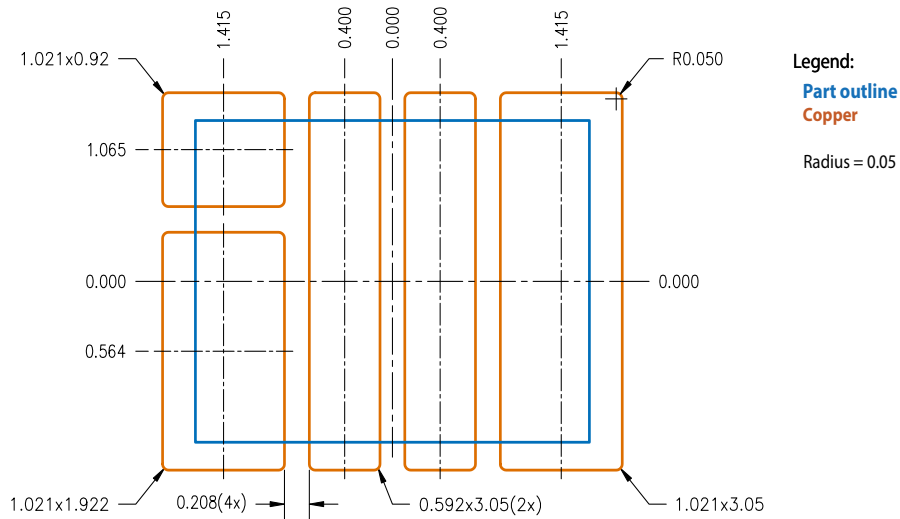
Part outline
Stencil opening

The recommended stencil should be 4mils (100 μm) thick, must be laser cut, and have openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found and scooping issues.

**RECOMMENDED
COPPER DRAWING**
(units in mm)



ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

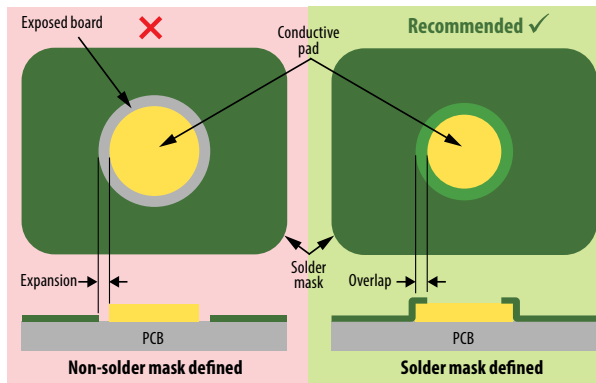


Figure 15: Solder mask defined versus non-solder mask defined pad

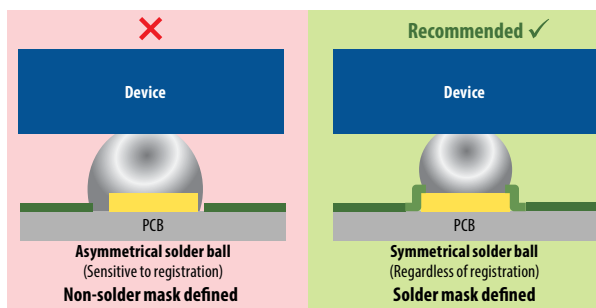


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

Prior to final qualification and production release, engineering samples might not meet all datasheet specifications.

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EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

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