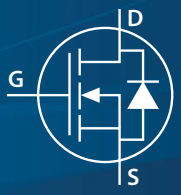
EPC29215_55 – Enhancement Mode Power Transistor

V_{DS}, 200 V
$R_{DS(on)}$, 8 mΩ
I_D, 32 A
95% Pb/5% Sn Solder



EFFICIENT POWER CONVERSION

Halogen-Free

Revised March 25, 2024

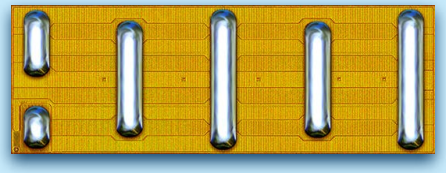
Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous (T_A = 25°C)	32	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	162	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	52	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



Die size: 4.6 x 1.6 mm

EPC29215_55 eGaN® FETs

Applications

- DC-DC converters
- BLDC motor drives
- Sync rectification for AC/DC and DC-DC
- Multi-level AC/DC power supplies
- Wireless power
- Solar micro inverters
- Robotics
- Class-D audio

Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low Q_G
- Small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC29215_55

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.6 mA	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 160 V		0.15	0.48	mA
		V_{GS} = 0 V, V_{DS} = 160 V, T_J = -55°C		0.008	0.048	
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.006	1	
		V_{GS} = 5 V, T_J = -55°C		0.0002	0.1	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.14	8.7	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.05	0.48	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 6 mA	0.8	1.2	2.5	V
		V_{DS} = V_{GS}, I_D = 6 mA, T_J = -55°C		1.3	2.6	
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 20 A		6.3	8	mΩ
		V_{GS} = 5 V, I_D = 20 A, T_J = -55°C		4.2	7.5	
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.6		V

Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 100 V		1356	1790	pF
C_{RSS}	Reverse Transfer Capacitance			2.0		
C_{OSS}	Output Capacitance			390	585	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 100 V		556		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			699		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 100 V, I_D = 20 A		13.6	17.7	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 100 V, I_D = 20 A		3.3		
Q_{GD}	Gate-to-Drain Charge			2.1		
$Q_{G(TH)}$	Gate Charge at Threshold			2.4		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 100 V		69	104	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

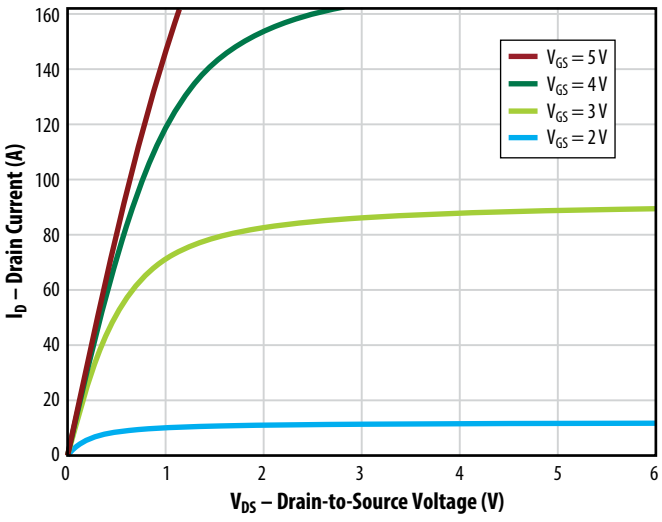


Figure 2: Typical Transfer Characteristics

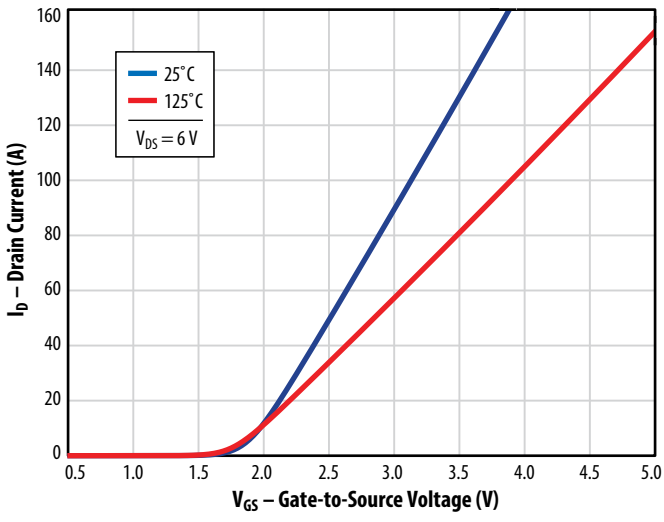


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

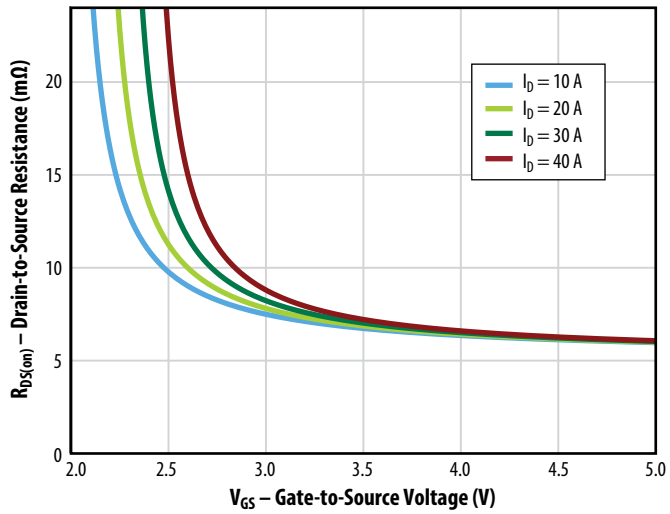


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

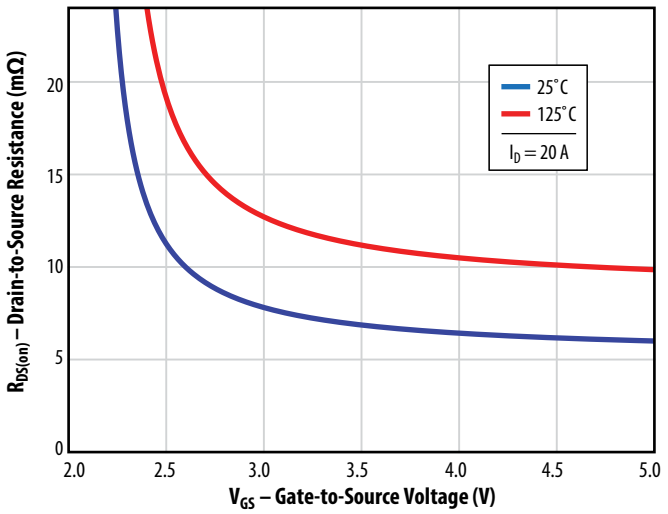


Figure 5a: Typical Capacitance (Linear Scale)

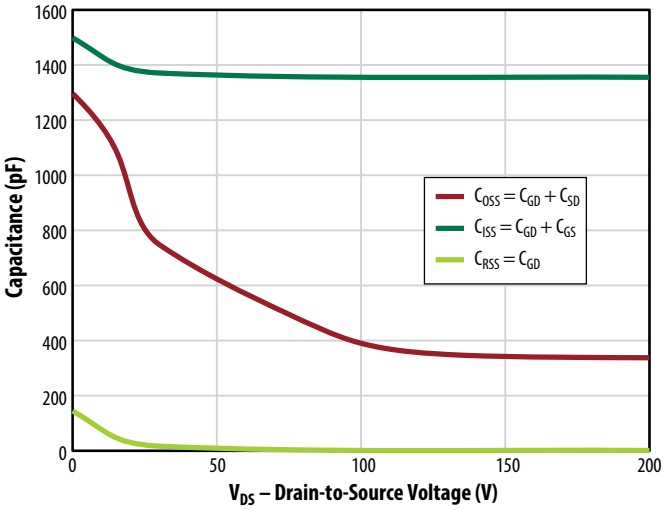


Figure 5b: Typical Capacitance (Log Scale)

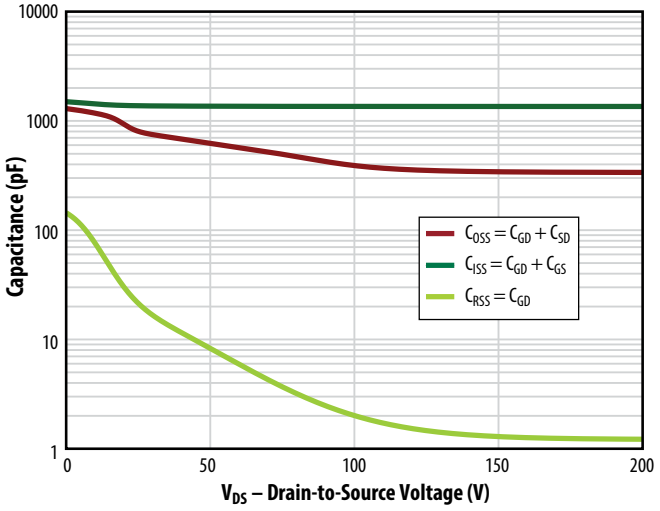


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

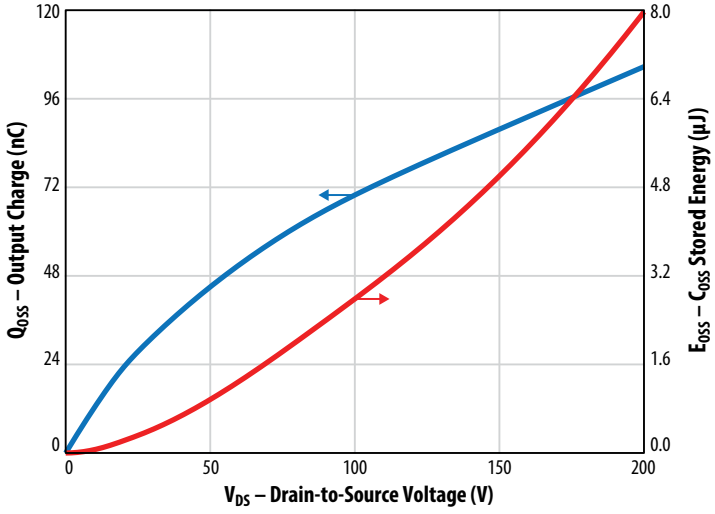


Figure 7: Typical Gate Charge

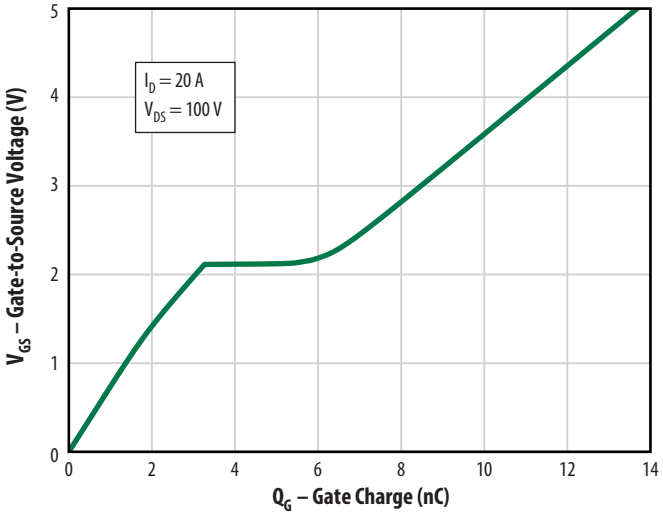
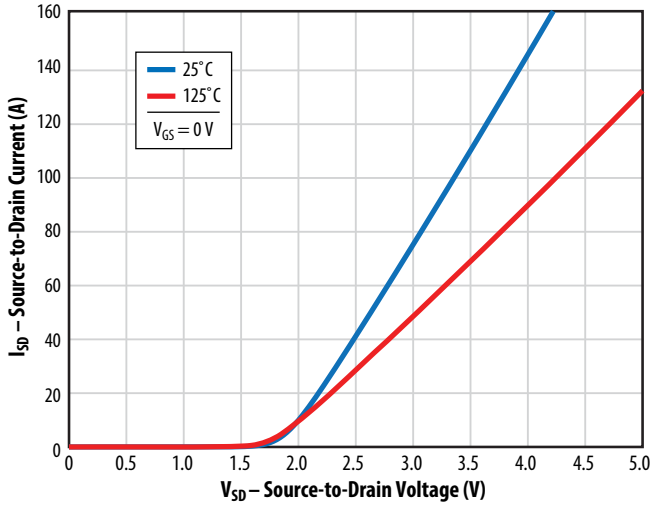


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

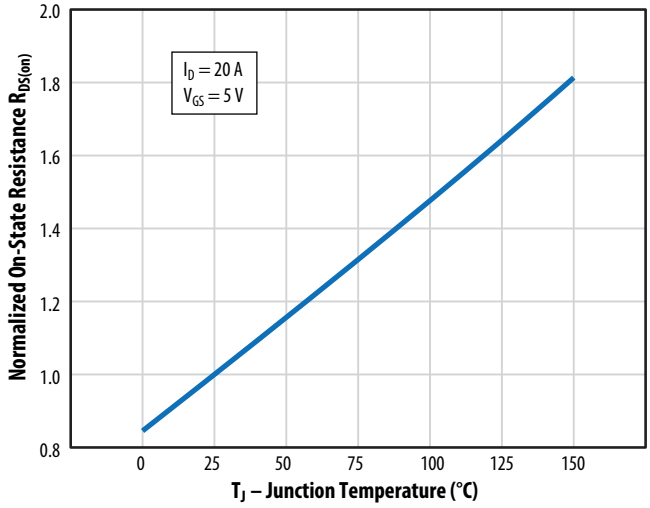


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

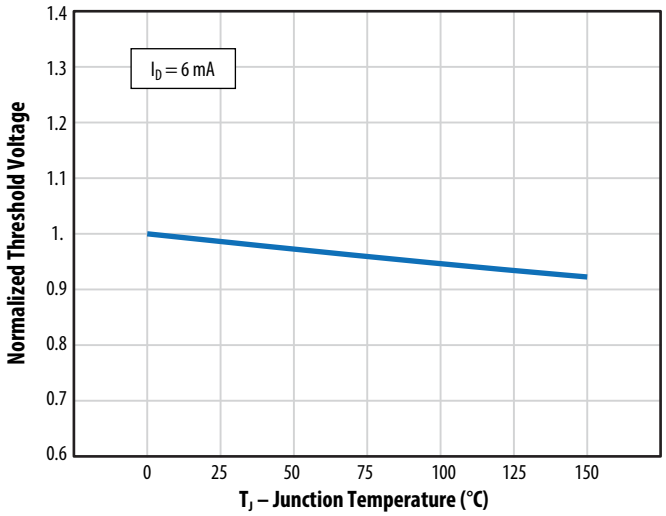
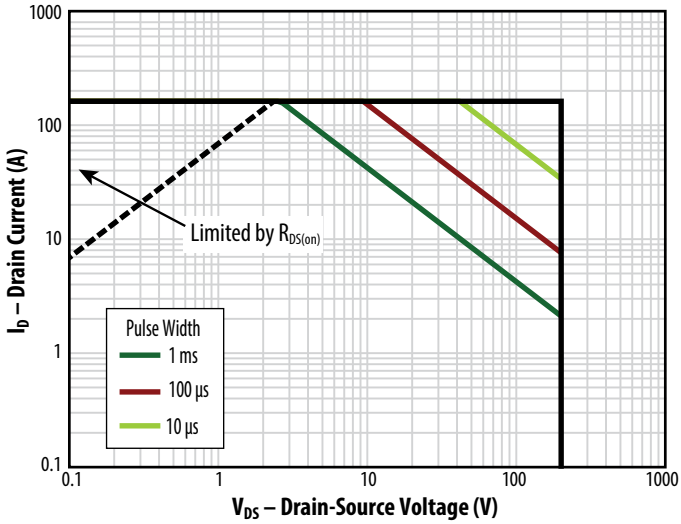
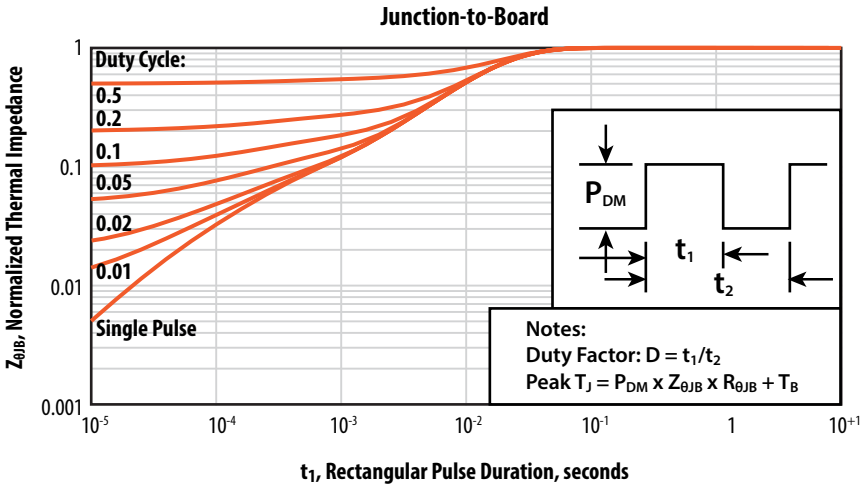


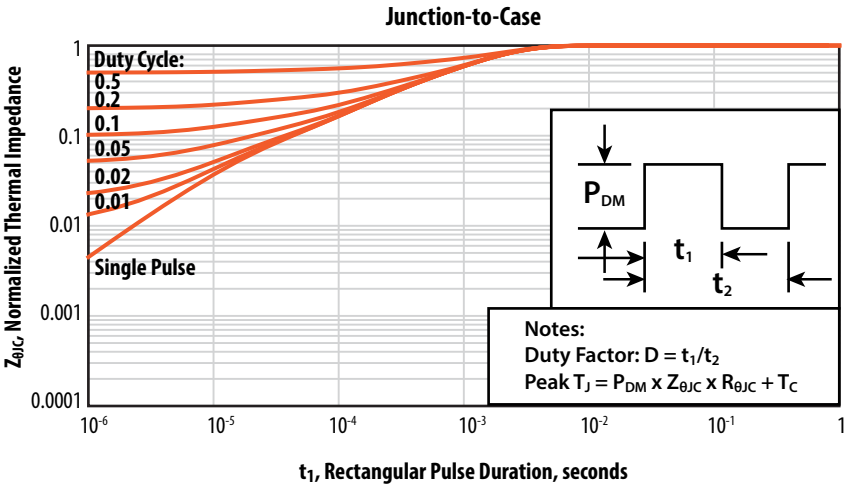
Figure 11: Safe Operating Area



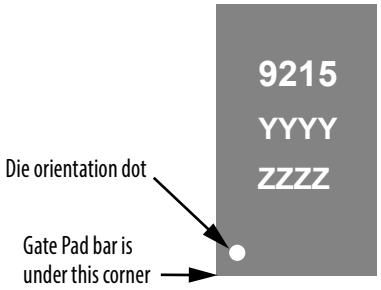
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves





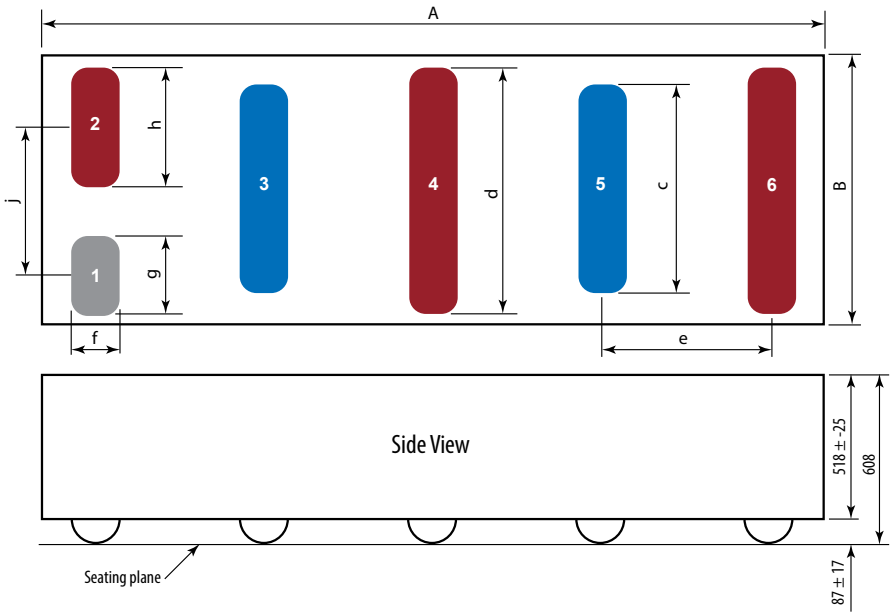
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC29215_55	9215	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

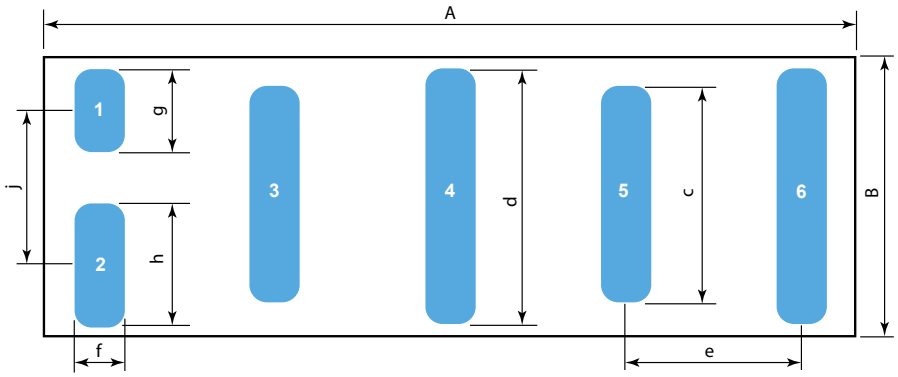


DIM	Micrometers		
	MIN	Nominal	MAX
A	4570	4600	4630
B	1570	1600	1630
c		1210	
d		1450	
e		1000	
f		275	
g		450	
h		700	
j		875	

Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN

(units in µm)



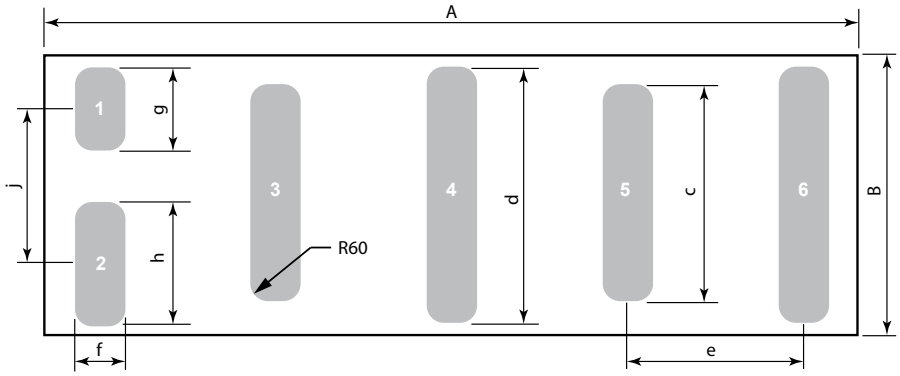
Land pattern is solder mask defined.

Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

DIM	Nominal
A	4600
B	1600
c	1210
d	1450
e	1000
f	275
g	450
h	700
j	875

RECOMMENDED STENCIL DRAWING

(units in µm)



DIM	Nominal
A	4600
B	1600
c	1210
d	1450
e	1000
f	275
g	450
h	700
j	875

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/design-support