EPC33110 – Three-Phase ePower™ Stage IC

V_{IN} , 100 V

I_{Load} , 20 A

PRELIMINARY

Halogen-Free

March 18, 2026

The ePower™ Stage IC Product Family integrates input logic interface, high-side level shifting, synchronous bootstrap charging, and gate drivers along with eGaN output FETs into one monolithic integrated circuit in an MSL1 QFN package, using EPC's proprietary GaN IC technology. The result is a Power Stage IC that translates logic level control signals into a high voltage and high current power stage, which is simpler to design, smaller in size and easier to manufacture while being more efficient to operate.

Questions:
Ask a GaN Expert

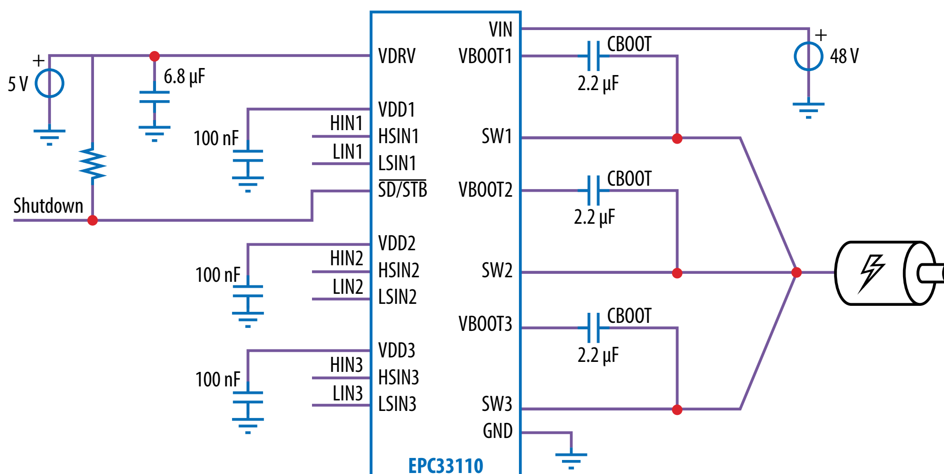
Key Parameters		
PARAMETER	**VALUE**	**UNIT**
Continuous power stage load current T_J = 25°C	20	A
Maximum operating PWM frequency	3	MHz
Absolute maximum input voltage	100	V
Operating input voltage range	80	V
Nominal bias supply voltage	5	V

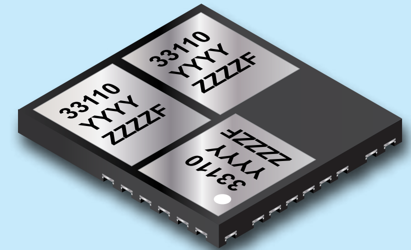
Output current and PWM frequency ratings are specified at ambient temperature of 25°C. See the application information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

Device Information		
PART NUMBER	**Rated $R_{DS(on)}$ for HS and LS FETs at 25 °C**	**QFN Package Size (mm)**
EPC33110	11.7 mΩ + 13 mΩ typ	6.5 x 6

All exposed pads feature wettable flanks that allow side wall solder inspection. High voltage and low voltage pads are separated by 0.6 mm spacing to meet IPC rules.

Figure 1: Typical Application





EPC33110 3-Phase ePower™ Stage IC
Package size: 6.5 x 6 mm

Applications

- Motor drive inverters

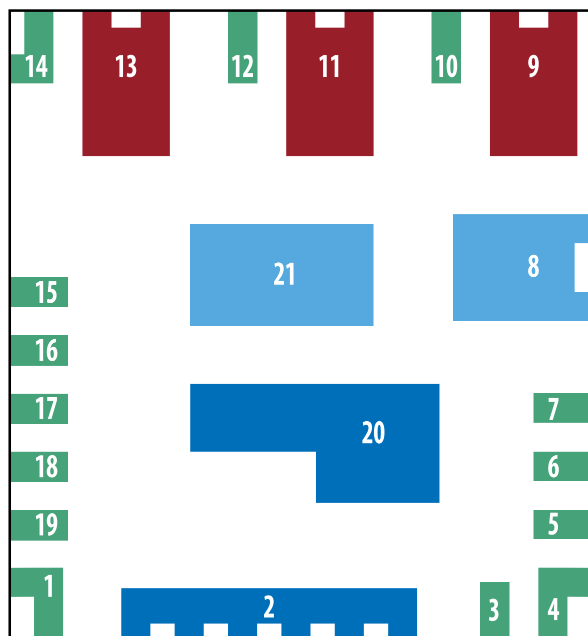
Features

- Three-phase integrated power module
- Each phase Integrates high-side and low-side eGaN® FET with internal gate driver and level shifter
- Single 5 V external bias supply
- 3.3 V or 5 V CMOS input logic levels
- Independent high-side and low-side control inputs for all phases
- Logic lockout commands both FETs off when inputs are both high at same time
- Robust level shifter operation for hard and soft switching conditions
- Synchronous charging for high-side bootstrap supplies
- Standby function for low quiescent current mode
- Fast PWM Shutdown when ($\overline{SD/STB}$) pulled low
- Power-on-reset for low-side and high-side power supplies
- Power stage high impedance guaranteed in absence of V_{DRV} / V_{BOOT} supplies
- 0% and 100% duty capable
- Thermally enhanced QFN package with exposed top

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC33110

Figure 2: EPC33110 Quad Flat No-Lead (QFN) Package (Transparent Top View)



EPC33110 Pinout Description

Pin	Pin Name	Pin Type	Description
1	$V_{DD}2$	S	Phase 2 internal power supply referenced to GND, connect a bypass capacitor from $V_{DD}2$ to GND.
2, 20	V_{IN}	P	Power DC input. Connected to drain terminal of three high-side FETs. Connect power loop capacitors from V_{IN} to GND.
3	$\overline{(SD/STB)}$	L	$V_{DD}1$, $V_{DD}2$ and $V_{DD}3$ standby and PWM fast shutdown input. $V_{DD}x$ are disabled when $\overline{(SD/STB)}$ is pulled down or driven low. Internal pull-up resistors disable the standby function by default. If $\overline{(SD/STB)}$ is pulled low, the PWM inputs are immediately inhibited, and all power GaN FETs are switched OFF.
4	V_{DRV}	S	External 5 V power supply referenced to GND, connect a bypass capacitor from V_{DRV} to GND.
5	$HS_{IN}3$	L	Phase 3 high-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $HS_{IN}3$ and GND.
6	$LS_{IN}3$	L	Phase 3 low-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $LS_{IN}3$ and GND.
7	$V_{DD}3$	S	Phase 3 internal power supply referenced to GND, connect a bypass capacitor from $V_{DD}3$ to GND.
8, 21	GND	P	Power ground. Connected to the source terminal of the low-side FET.
9	SW3	P	Phase 3 switching node. Connected to phase 3 half-bridge power stage output.
10	$V_{BOOT}3$	S	Phase 3 floating bootstrap power supply referenced to SW3. Connect an external bootstrap capacitor, $C_{BOOT}3$, between $V_{BOOT}3$ and SW3.
11	SW2	P	Phase 2 switching node. Connected to phase 2 half-bridge power stage output.
12	$V_{BOOT}2$	S	Phase 2 floating bootstrap power supply referenced to SW2. Connect an external bootstrap capacitor, $C_{BOOT}2$, between $V_{BOOT}2$ and SW2.
13	SW1	P	Phase 1 switching node. Connected to phase 1 half-bridge power stage output.
14	$V_{BOOT}1$	S	Phase 1 floating bootstrap power supply referenced to SW1. Connect an external bootstrap capacitor, $C_{BOOT}1$, between $V_{BOOT}1$ and SW1.
15	$HS_{IN}1$	L	Phase 1 high-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $HS_{IN}1$ and GND.
16	$LS_{IN}1$	L	Phase 1 low-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $LS_{IN}1$ and GND.
17	$V_{DD}1$	S	Phase 1 internal power supply referenced to GND, connect a bypass capacitor from $V_{DD}1$ to GND.
18	$HS_{IN}2$	L	Phase 2 high-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $HS_{IN}2$ and GND.
19	$LS_{IN}2$	L	Phase 2 low-side PWM logic input referenced to GND. Internal pull-down resistor is connected between $LS_{IN}2$ and GND.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs

Note: The standby function can be disabled by tying each $V_{DD}x$ to V_{DRV}. In this case, only the PWM fast shutdown function is enabled.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise. The letter x indicates the phase: V_{DD}x corresponds to V_{DD}1, V_{DD}2, and V_{DD}3; SWx corresponds to SW1, SW2, and SW3; et cetera.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
V_{IN}	DC Power input voltage		100	
$SWx_{(continuous)}$	Output switching node voltage, continuous		100	
V_{DRV}	External bias supply voltage (V_{DRV} to AGND)		6	
V_{DD}x	Internal low-side supply voltage (V_{DD} to AGND)		6	V
V_{BOOT}x – SWx	Internal high-side supply voltage (V_{BOOT} to V_{PHASE}), V_{PHASE} = SW		6	
HS_{IN}x, LS_{IN}x	PWM logic input voltage	-1	5.5	
$\overline{SD}$/STB	V_{DD} disable input voltage – standby, PWM shutdown function	-1	5.5	
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-55	150	

ESD Ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)[1]	+/-500		V
CDM	Charged-device model (JEDEC JESD22-C101)[2]	+/-500		

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

Thermal Characteristics

$R_{θJA_JEDEC}$ is measured using JESD51-2 standard setup with 1 cubic foot enclosure with no forced air cooling, heat dissipated only through natural convection. The test used JEDEC Standard 4-layers PCB with 2 oz top and bottom surface layers and 1oz buried layers. $R_{θJA_EVB}$ is measured using EPC91122 EVB with no forced air cooling, this rating is more indicative of actual application environment.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{θJC_Top}$	Thermal resistance, junction-to-case (Top surface of exposed die substrate)	0.61	
$R_{θJB_Bottom}$	Thermal resistance, junction-to-board (At solder joints of V_{IN}, SW and PGND pads)	3.7	°C/W
$R_{θJA_JEDEC}$	Thermal resistance, junction-to-ambient (using JEDEC 51-2 PCB)	TBD	
$R_{θJA_EVB}$	Thermal resistance, junction-to-ambient (using EPC91122 EVB)	TBD	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. If used outside the recommended operating conditions but within the absolute maximum ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device's lifetime. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise. The letter x indicates the phase: V_{DD}x corresponds to V_{DD}1, V_{DD}2, and V_{DD}3; et cetera.

Recommended Operating Conditions					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	DC power input voltage - V_{DRV} not tied to V_{DD}	10		80	
$V_{IN\ (Boost\ Mode)}$	DC power input voltage - V_{DRV} tied to V_{DD}x [3]	0			
$SWx_{(Q3\ Mode)}$	Phase x Output switch node, 3rd quadrant mode	-2.5		V_{IN} + 2.5	
$SWx_{(pulse2ns)}$	Phase x Output switch node, transient pulse < 2 ns	-10		V_{IN} + 10	
V_{DRV}	External supply voltage (V_{DRV} to GND)	4.75	5	5.5	V
V_{DD}x	Internal low-side supply voltage (V_{DD}x to GND)	4.75	5	5.5	
V_{BOOT}x – SWx	Internal high-side supply voltage (V_{BOOT} to SWx)	4.75	5	5.5	
HS_{IN}x, LS_{IN}x	PWM logic input voltage	0		5	
$\overline{SD}$/STB	V_{DD} disable input voltage – standby [3], PWM shutdown function	0		5	
$T_{J,op}$	Operating junction temperature	-40		125	°C

(3) Tie V_{DD} and V_{DRV} together to disable the standby function, while maintaining the fast PWM shutdown, as shown in figure 13.

Electrical Characteristics

Nominal V_{IN} = 48 V, V_{DRV} = V_{DD} = 5 V and (V_{BOOT} – V_{PHASE}) = 5 V. All typical ratings are specifed at T_A = 25˚C unless otherwise indicated. All voltage parameters are absolute voltages referenced to PGND unless indicated otherwise. AGND and PGND are internally connected. Parameters that show only the typical value are guaranteed by design and not tested in production. The letter x indicates the phase: V_{DD}x corresponds to V_{DD}1, V_{DD}2, and V_{DD}3; et cetera..

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Low-side Power Supply						
I_{DRV_Q}	OFF state total quiescent current	HS_{IN}x/LS_{IN}x/$\overline{STB}$ = 0 V, SW floating		30		mA
I_{DRV_100kHz}	Total operating current @100 kHz	PWM = 100 kHz, 50% ON-time, includes bootstrap current		48		mA
I_{DRV_1MHz}	Total operating current @1 MHz	PWM = 1 MHz, 50% ON-time, includes bootstrap current		69		mA
Standby Current						
$I_{VIN_standby}$	V_{IN} current in standby mode	$\overline{SD/STB}$ = 0 V		330	480	µA
$I_{DRV_standby}$	V_{DRV} current in standby mode	$\overline{SD/STB}$ = 0 V		300	450	µA
Bootstrap Power Supply per each phase						
I_{BOOT_Q}	OFF state bootstrap supply current	HS_{IN}x/LS_{IN}x/ = 0 V, $\overline{SD/STB}$ = 5 V	4	6	8	mA
I_{BOOT_100kHz}	Bootstrap supply current @100 kHz	HS PWM = 100 kHz, 50% ON-time		7		mA
I_{BOOT_1MHz}	Bootstrap supply current @1 MHz	HS PWM = 1 MHz, 50% ON-time		12		mA
$R_{ON_SYNC_BOOT}$	ON resistance of sync-boot FET	I_{SYNC_BOOTx} = 25 mA	1	1.7	2.6	Ω
Power On Reset per each phase						
V_{DD_POR+}	POR trip level V_{DD} rising	LS_{IN} = 5 V, V_{DD} ramps up			4.25	V
$V_{DD_POR_HYST}$	POR V_{DD} falling hysteresis	LS_{IN} = 5 V, V_{DD} ramps down		0.15		V
V_{BOOT_POR+}	POR trip level (V_{BOOT} - V_{PHASE}) rising	HS_{IN} = 5 V, V_{BOOT} ramps up			4.25	V
$V_{BOOT_POR_HYST}$	POR (V_{BOOT} - V_{PHASE}) falling hysteresis	HS_{IN} = 5 V, V_{BOOT} ramps down		0.15		V
Logic Input Pins						
V_{IH}	High-level logic threshold	HS_{IN}, LS_{IN} rising	2.4			V
V_{IL}	Low-level logic threshold	HS_{IN}, LS_{IN} falling			0.8	V
V_{IHYST}	Logic threshold hysteresis	V_{IH} rising – V_{IL} falling	0.3			V
R_{IN}	HS_{IN} and LS_{IN} pull-down resistance	HS_{IN}, LS_{IN} = 5 V		5		kΩ
V_{DD} Disable - Standby Function and PWM disable Function						
$V_{SD\text{-}STB_H}$	High-level $\overline{SD/STB}$ logic threshold	$\overline{SD/STB}$ rising	2.4			V
$V_{SD\text{-}STB_L}$	Low-level $\overline{SD/STB}$ logic threshold	$\overline{SD/STB}$ falling			0.8	V
R_{STB}	STB pull-up resistance	$\overline{SD/STB}$ = 0 V		22		kΩ
High-Side Internal Power FET (HS_FET)						
$R_{DS(on)_HS1}$	Phase 1 high-side FET $R_{DS(on)}$	I_{SW1} = +/-1 A, HS_{IN1} = 5 V, LS_{IN1} = 0 V (2)		11.7	14.8	mΩ
$R_{DS(on)_HS2}$	Phase 2 high-side FET $R_{DS(on)}$	I_{SW2} = +/-1 A, HS_{IN2} = 5 V, LS_{IN2} = 0 V (2)		12.2	15.4	mΩ
$R_{DS(on)_HS3}$	Phase 3 high-side FET $R_{DS(on)}$	I_{SW3} = +/-1 A, HS_{IN3} = 5 V, LS_{IN3} = 0 V (2)		12	15.2	mΩ
$V_{HS_DS_Clamp}$	High-side 3rd quadrant clamp	I_{SW} = -1 A, HS_{IN} = LS_{IN} = 0 V (2)	-2.1	-1.7		V
$V_{HS_DS_Clamp_0V}$	High-side 3rd quadrant clamp	I_{SW} = -1 A, HS_{IN} = LS_{IN} = 0 V, V_{BOOT} – V_{PHASE} = 0 V (2)		-3.5		V
C_{OSS_HSFET}	Output capacitance (V_{IN} to SW)	HS_{IN} = 0 V, SW = 0 V		189		pF
Q_{OSS_HSFET}	Output charge (V_{IN} to SW)	HS_{IN} = 0 V, SW = 0 V		15		nC
E_{QOSS_HSFET}	Output capacitance stored energy	HS_{IN} = 0 V, SW = 0 V		0.27		µJ
Low-Side Internal Power FET (LS_FET)						
$R_{DS(on)_LS1}$	Phase 1 low-side FET $R_{DS(on)}$	I_{SW1} = +/-1 A, LS_{IN1} = 5 V, HS_{IN1} = 0 V (2)		13	16.4	mΩ
$R_{DS(on)_LS2}$	Phase 2 low-side FET $R_{DS(on)}$	I_{SW2} = +/-1 A, LS_{IN2} = 5 V, HS_{IN2} = 0 V (2)		17.5	22.2	mΩ
$R_{DS(on)_LS3}$	Phase 3 low-side FET $R_{DS(on)}$	I_{SW3} = +/-1 A, LS_{IN3} = 5 V, HS_{IN3} = 0 V (2)		13.4	16.9	mΩ
$V_{LS_DS_Clamp}$	Low-side 3rd quadrant clamp	I_{SW} = 1 A, HS_{IN} = LS_{IN} = 0 V (2)	-2.1	-1.7		V
$V_{LS_DS_Clamp_0V}$	Low-side 3rd quadrant clamp	I_{SW} = 1 A, HS_{IN} = LS_{IN} = 0 V, V_{DD} = 0 V (2)		-3.5		V
C_{OSS_LSFET}	Output capacitance (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		221		pF
Q_{OSS_LSFET}	Output charge (SW to PGND)	LS_{IN} = 0 V, SW = 48 V		19		nC
E_{QOSS_LSFET}	Output capacitance stored energy	LS_{IN} = 0 V, SW = 48 V		0.34		µJ

Electrical Characteristics *(continued)*

Electrical Characteristics# (continued)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power FETs Quiescent Currents per each phase – include internal biasing circuits[3]						
$I_{Q_VIN\text{-}SWx}$	Quiescent current (V_{IN} to SW)	$HS_{IN}x$ = 0 V, V_{IN} = 100 V, SWx = 0 V			230	µA
$I_{Q_SWx\text{-}GND}$	Quiescent current (SWx to GND)	$LS_{IN}x$ = 0 V, V_{IN} = 100 V, SWx = 100 V			2.7	mA
$I_{Q_VIN\text{-}GND}$	Quiescent current (V_{IN} to GND)	$HS_{IN}x$ = 0 V, V_{IN} = 100 V		119	230	µA
		$HS_{IN}x$ = 0 V, V_{IN} = 48 V			160	
Dynamic Characteristics (Logic Input to Output Switching Node SWx) (See Figure 3 for Timing Diagram)						
$PW_{_min}$	Minimum pulse width	50% to 50% width, $LS_{IN}x$ and $HS_{IN}x$ [5]		30 [1]		ns
t_{Filter}	Input filter cutoff time	50% to 50% width, $LS_{IN}x$ and $HS_{IN}x$		15		ns
$t_{Shutdown}$	Shutdown propagation delay	50% to 50% width, HS and LS FET turn-OFF		36		
$t_delay_{HS_on}$	High-side ON propagation delay	SW = 0 V and HS FET turn-ON		36		
$t_delay_{LS_on}$	Low-side ON propagation delay	SW = 48 V and LS FET turn-ON		36		
$t_delay_{HS_off}$	High-side OFF propagation delay	SW = 48 V and HS FET turn-OFF		36		
$t_delay_{LS_off}$	Low-side OFF propagation delay	SW = 0 V and LS FET turn-OFF		36		
t_match_{on}	Delay matching LS_{off} to HS_{on}	LS turn-OFF to HS turn-ON		0		
t_match_{off}	Delay matching HS_{off} to LS_{on}	HS turn-OFF to LS turn-ON		0		
t_lockout	Cross-conduction lockout time	LS turn-OFF to HS turn-ON or HS turn-OFF to LS turn-ON – no dead time on $LS_{IN}x$ $HS_{IN}x$ inputs		5		
$t_rise_{SW_HS10}$	SW rise time at high-side FET turn-ON (motor drive, hard switching)	HS turn-ON current exiting from SW node, 0 V to 48 V, R_{BOOT} = 10 Ω, I_{LOAD} = 5 A [4]		5		
$t_fall_{SW_LS10}$	SW fall time at low-side FET turn-ON (motor drive, hard switching)	LS turn-ON current entering the SW node, 48 V to 0 V, R_{DRV} = 10 Ω, I_{LOAD} = 5 A [4]		5		

(1) Not tested, guaranteed by design

(2) $I_{SW}x$ is positive when exiting from SWx node. Resistance includes the contribute due to copper traces within the package.

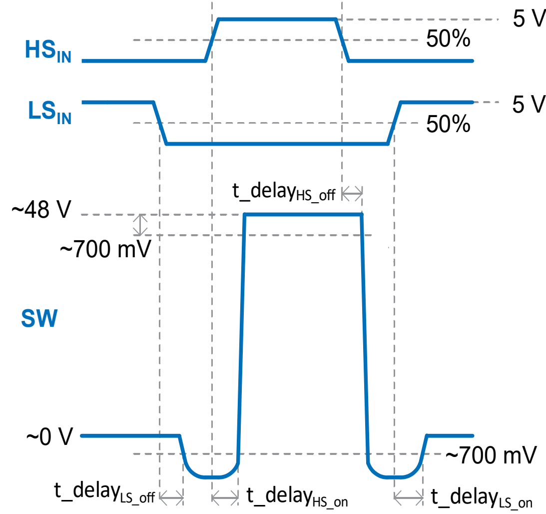
(3) The quiescent currents include the power FET I_{DSS} as well as the internal circuits biasing currents

(4) Measured on application board EPC91122

(5) There is no max limit for the pulse width length in time, as long as the voltage supply is not below the power on reset threshold limit. PW_max for the high-side FET depends also on the external bootstrap capacitance value. If the C_{BOOT} voltage falls below power on reset threshold voltage, the high-side GaN FET is switched OFF. The high-side circuit can be biased from an external 5 V floating voltage supply to allow infinite turn on of the high-side FET.

Dynamic Characteristics Parameter Definition

Figure 3: Logic Input to Output Switching Node Timing Diagram (current exiting from SW node)



Output Capacitance vs. Drain-to-Source Voltage

Figure 4a: C_{OSS_HSFET} of high-side Power GaN FET

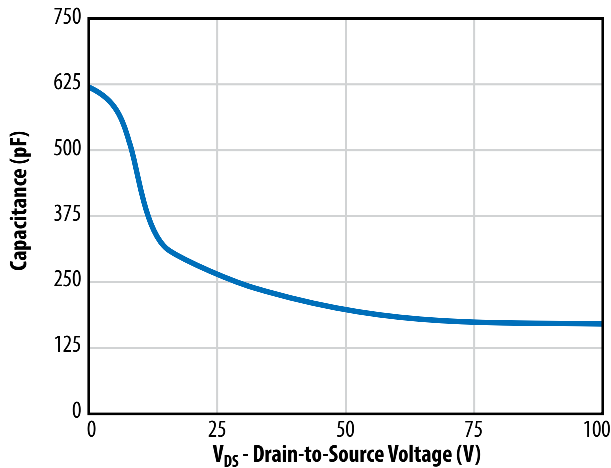
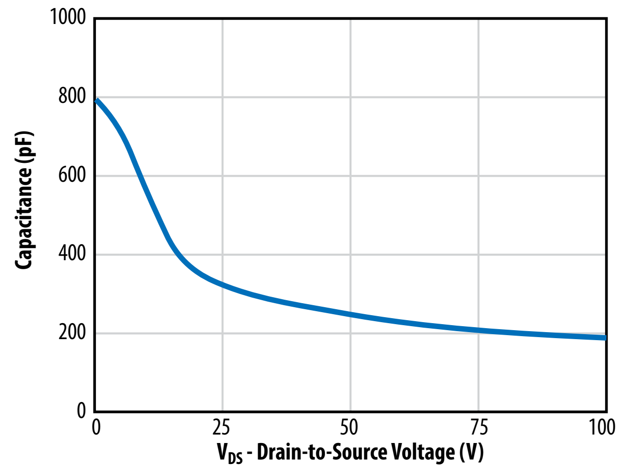


Figure 4b: C_{OSS_LSFET} for low-side Power GaN FET



Typical Output Charge and C_{OSS} Stored Energy

Figure 5a: Q_{OSS} and E_{OSS} of High-Side Power GaN FET

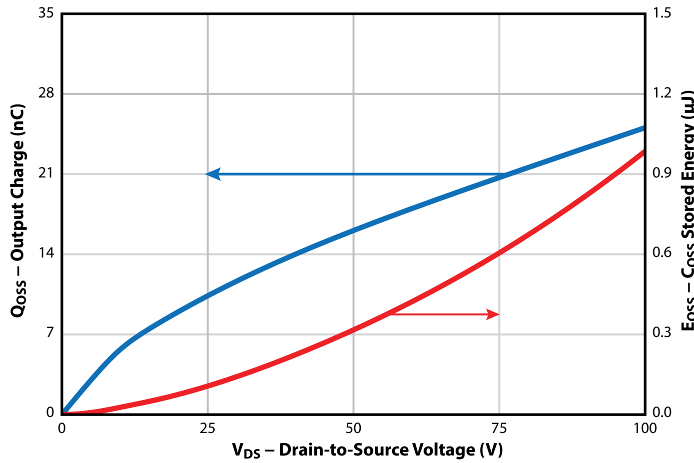
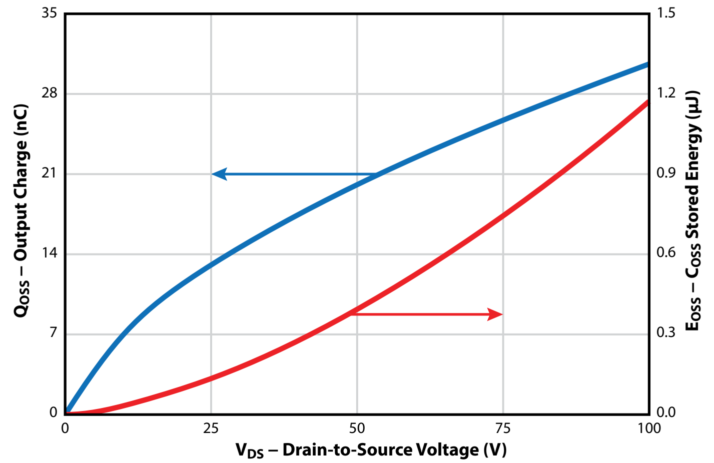


Figure 5b: Q_{OSS} and E_{OSS} of Low-Side Power GaN FET



Power GaN FETs Typical $R_{DS(on)}$ vs. Temperature

Figure 5a: High Side FET Normalized $R_{DS(on)}$

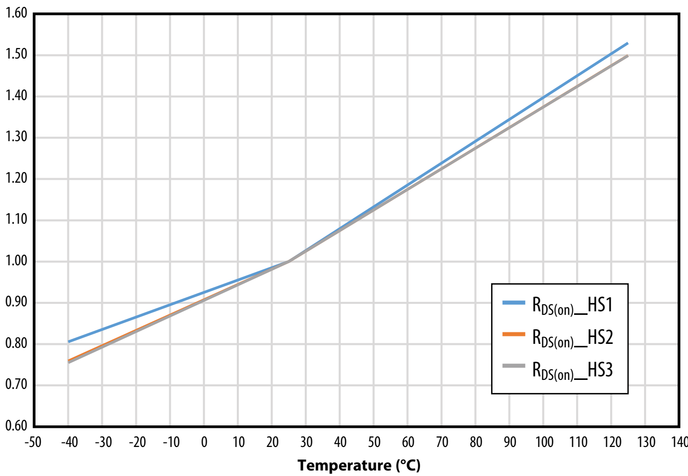
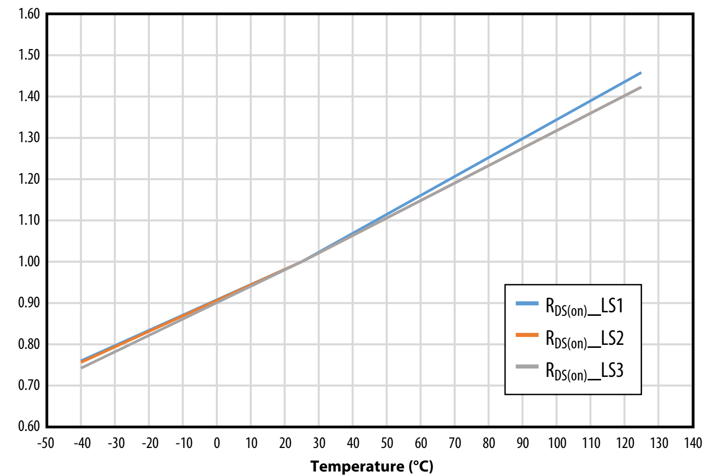


Figure 5b: Low Side FET Normalized $R_{DS(on)}$



Truth Table

$\overline{SD}/STB$	$V_{DD}x$	$V_{BOOT}x – SWx$	$HS_{IN}x$	$LS_{IN}x$	HS FET Phase x	LS FET Phase x
Low(1)	–	–	–	–	OFF	OFF
High	$<V_{DD_POR}$	–	-	-	OFF	OFF
	$>V_{DD_POR}$	$<V_{BOOT_POR}$	–	0	OFF	OFF
			–	1	OFF	ON
	$>V_{DD_POR}$	$>V_{BOOT_POR}$	0	0	OFF	OFF
			0	1	OFF	ON
			1	0	ON	OFF
			1	1	OFF	OFF

(1) $\overline{SD}/STB$ immediately inhibits PWM inputs when pulled low.

Application Information

General Description

The EPC33110 three-phase module ePower™ Stage integrates three half-bridges gate drivers with internal high-side and low-side FETs. Integration is implemented using EPC's proprietary GaN IC and packaging technology. Each of the three monolithic chips integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits controlling high-side and low-side eGaN output FETs configured as a half-bridge power stage to drive one phase. Robust level shifters from low-side to high-side channels are designed to operate correctly with soft and hard switching conditions even at large negative clamped voltage and to avoid false trigger from fast dv/dt transients including those driven by external sources or other phases. Internal circuits integrate the functions of charging and disabling of the logic and bootstrap power supplies. Protection features are added to protect the output FETs from unwanted turn-on at low or even complete loss of supply voltages. The three GaN ICs are mounted inside a 6.5 x 6 mm Quad Flat No-lead (QFN). This packaging structure allows very low parasitic inductance from the power terminals to the underlying PCB solder pads. The exposed QFN pads are designed to have at least 0.6 mm spacing between high and low voltage pins to meet IPC voltage creepage rule for 100 V. Another enhancement exposes the backside of the GaN IC dies on the top side of the package while completely encapsulating the rest of the three GaN ICs. This allows a very low thermal resistance path from each die junction to an attached heatsink which in effect increases the allowable power dissipation and thus higher current handling capability.

Output Current Rating

The three phase power output current rating is best thought of as a figure of merit for specified output current level that accounts for the maximum amount of power dissipation allowed from each of the three ICs. The total power dissipation from a three phase power module is tied to the application circuit topologies, output current demand, switching frequencies, construction, operating temperature range, thermal management technique and mechanical stress limit of the metallization imposed by electromigration. The rating is related to the respective maximum current capability of the six integrated output FETs in the three half-bridge power stages but not measured the same way as individual discrete FET. For a three phase power module such as EPC33110, total power loss from the ICs is the sum of the output FETs conduction, switching and deadtime losses imposed by the application topologies at operating switching frequencies as well as power losses from the gate drive and logic circuit. Figure 6 shows the functional block diagram of one of the three phases. The inputs V_{IN}, GND, $\overline{SD/STB}$ and V_{DRV} are common to all phases, while the inputs with the x subscript are specific for each phase (i.e.: x = 1,2,3).

The maximum power dissipation is defined by the following formula:

$$\text{Max } P_{Diss} = (\text{Max } T_J - T_A) / R_{\theta JA}$$

where Max T_J is specified at 125 °C and the ambient temperature is specified at 25 °C. The big variable in achieving the theoretical maximum power dissipation is $R_{\theta JA}$, the thermal resistance from junction to ambient. The EPC33110 package construction allows two parallel paths of heat dissipation where the bottom path goes from junction to metallization to lead-frame then the exposed pads at the bottom of the package. $R_{\theta JB_bottom}$ is determined by the bottom power pads (V_{IN}, SWx and GND) which are designed to allow maximum contact area to the underlying PCB. The total thermal resistance to ambient in this path of $R_{\theta JA_bottom}$ needs to add the heat dissipation from the PCB pads through the multi-layer PCB construction then radiating to the ambient which is highly dependent on the airflow and forced cooling method. (See Figure 8).

Figure 6: Functional Block Diagram of one phase

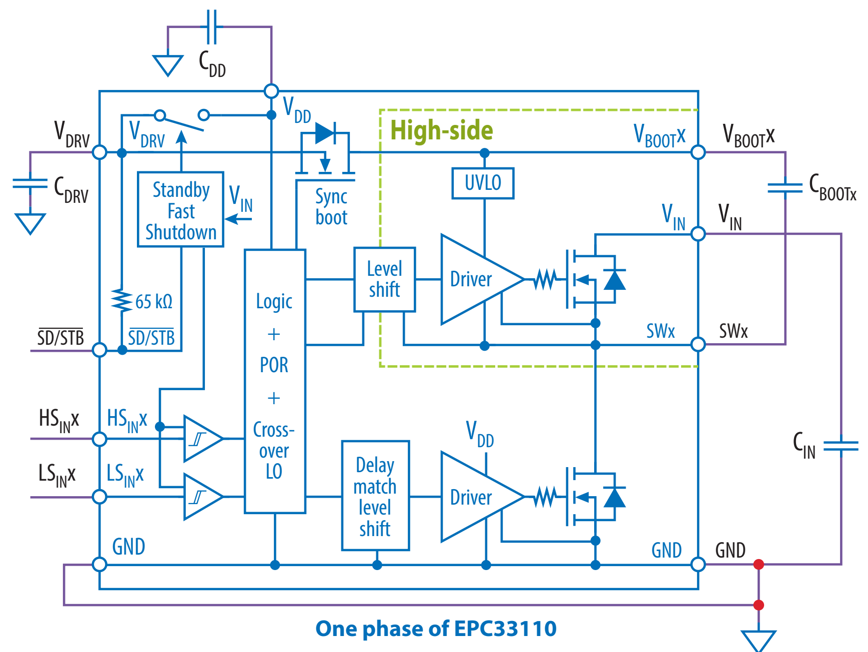


Figure 7: EPC33110 QFN package outline, pinouts and exposed backside of the GaN IC dies

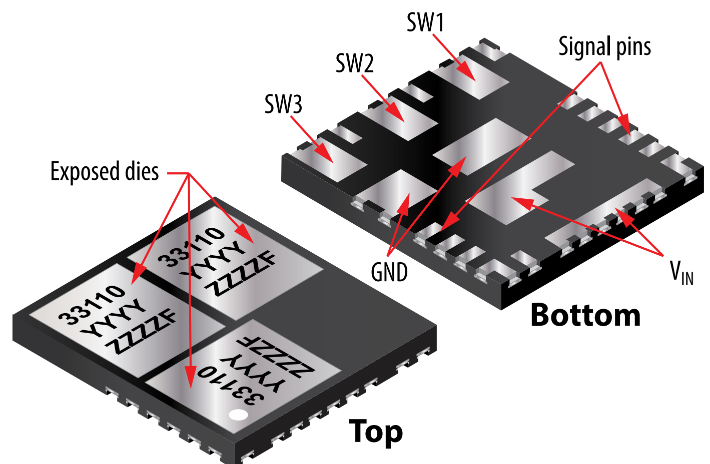
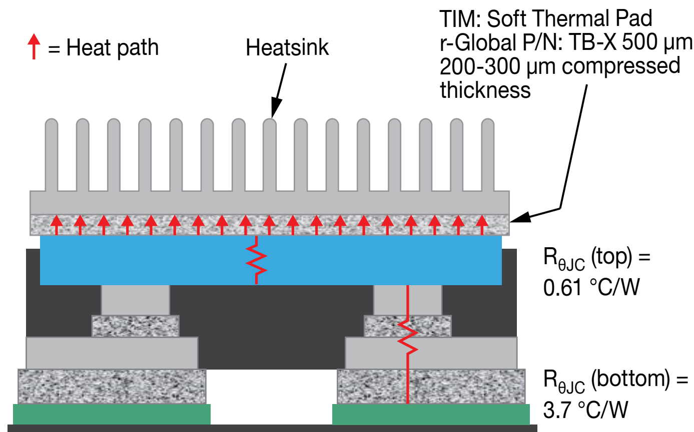


Figure 8: Parallel Thermal Resistance Paths of EPC33110 IC from Junction to Ambient



To achieve even lower effective thermal resistance, another path is provided from junction to the relatively lower thermal resistance Si substrate of the GaN IC structure to the exposed backside of the entire die at the top of the package to achieve a $R_{θJC_top}$ of 0.61 °C/W. This lower PCB thermal resistance path facilitates attachment of a topside heatsink through thermal interface material (TIM) to the exposed backside of the die. Note that the backside of the die is connected to the PGND (=AGND) pins which potentially provides added benefits of using electrically conductive TIM which has >2X higher thermal conductivity and lower cost than the insulating type. Typical parameters of electrically conducting vs. insulating TIMs are shown in the table below. The resistance between the exposed backside and PGND is at least 100 Ω, due to the low doping level of the Si substrate.

Typical parameters of electrically conducting vs. insulating TIMs		
Type of TIM	**Thermal Conductivity (W/m·K)**	**Relative Cost**
Electrically Conducting	40	1
Electrically Insulating	15	1.3

Another factor in specifying the output current rating is electromigration from a metallurgical standpoint. For EPC33110 this limit is a function of the metallization structure underlying the two output FETs plus their connection to the lead-frame and the three exposed power bars.

Motor Drive Inverter Application

The EPC91122 evaluation board shown in Figure 9 is a 3-phase BLDC motor drive inverter board that can deliver up to 11 A_{RMS} steady-state output current and up to 20 A_{RMS} pulsed output current (t_{pulse}= 300 ms at 5%, 10%, and 20% of the total period). The EPC91122 contains all the necessary critical function circuits to support a complete motor drive inverter. Figure 10 depicts the steady-state thermal performance of the EPC91122 board. When operated on a motor bench at an ambient temperature of 22°C, with a 48 V_{DC} supply and natural convection, the EPC91122 can deliver 5 A_{RMS} per phase without a heatsink and 13 A_{RMS} per phase with a heatsink attached, with a temperature rise below 60°C from the IC case to ambient. Motor drive operating points at PWM = 50, and 100 kHz, deadtime = 50 ns, with and without heatsink at 22°C ambient temperature, under natural convection.

Figure 9: EPC91122 Evaluation Board (see EPC91122 Quick Start Guide for details)

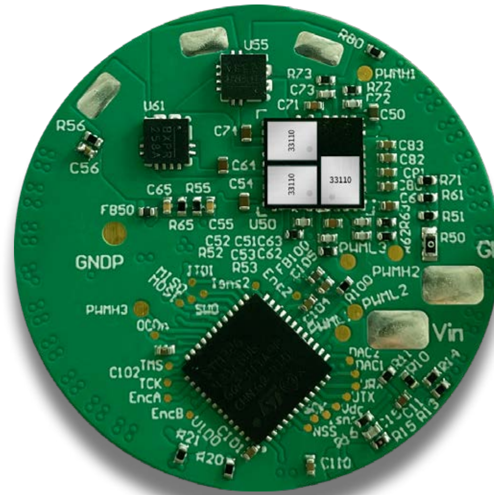
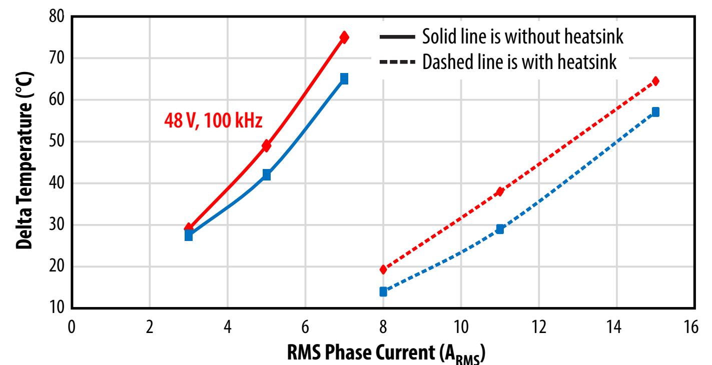


Figure 10: EPC91122 eGaN IC Temperature Increase vs. Ambient Temperature



Power Supplies – V_{IN}, V_{DRV}, V_{DD}x, and V_{BOOT}x

The EPC33110 IC only requires an external 5 V V_{DRV} power supply. Internal low-side and high-side power supplies, V_{DD} and V_{BOOT}, are generated from the external supply via two independent switches. Figure 11 shows the simplified circuit diagram of the different power supplies inside the IC and their interaction with each other.

Figure 11: Simplified Circuit Diagram of V_{IN}, V_{DRV}, V_{DD}x, and V_{BOOT}x Power Supplies. Only one phase is shown.

The internal supplies can be disabled to save quiescent power by turning off the series switch, QSA in Figure 11, with 0 V applied to the (SD/STB) pin to engage chip standby mode. In this mode, minimum current is drawn from the external V_{DRV} supply while all the three V_{DD}x are open circuits. Whatever charge remains within the V_{DD}x bypass capacitors will be discharged by the chips internal circuits by I_{DRV_Q}. In the chip standby circuits, the series switches (QSA) between V_{DRV} and V_{DD}x are turned off by an internal standby circuit which itself derives its power from V_{IN} such that the chip draws a current $I_{VIN_disable}$ from V_{IN} when standby mode is engaged. The standby function requires a minimum input voltage of $V_{IN,min}$ for the IC to be enabled. Below $V_{IN,min}$, the pass-transistors between V_{DRV} and V_{DD}x will be off. To disable the standby function, and thus extend the minimum operating voltage to $V_{IN(Boost\ Mode)}$min = 0 V, tie the three pins V_{DD}x (x=1,2,3) and V_{DRV} together. This is mandatory in multi-phase boost converter applications, when DC input voltage, applied to SWx pin, is lower than 13.5 V (= V_{INmin} + $|V_{HS_DS_Clamp_0V}|$). Moreover, in multi-phase boost mode, if the feed-through operation mode is required, it is recommended to use three Schottky diodes in parallel to the three high-side GaN FETs to mitigate the losses during non-switching operation (all HS_{IN}x and LS_{IN}x OFF, or there is no V_{DD}x). The series connected high voltage synchronous bootstrap FETs, Q_{SB} in Figure 11, between V_{DD}x and V_{BOOT}x for each high-side floating bootstrap supply are activated only after the respective LS FET (Q2) is turned on to avoid overcharging during deadtime on each phase. The use of GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage is the lower dropout voltage of approximately 100 mV from the synchronous FET versus typical Si bootstrap diode voltage of 0.6 V. With synchronous charging all V_{BOOT}x are maintained closer to the V_{DD}x voltage, allowing the HS FET gate drive circuits to have similar gate drive current and delay performance as the LS FET gate drive circuits.

Gate Driver

The EPC33110 power module integrates three HS and LS FET gate drivers with low impedance and high pulse current push-pull NFET output stages. Figure 12 is the simplified circuit diagram of the gate driver output stage of one phase.

Figure 12: Simplified Circuit Diagram of Gate Driver Output Stage

The LS and HS gate drive voltage levels are derived from their respective internal low-side (V_{DD}x) and high-side (V_{BOOT}x) power supplies. To ensure that the gate drive level (Q) is sufficiently close to V_{DD}x or V_{BOOTx}, an internal driving circuit is used to turn-on MPO. Here MPO and MSO work similarly to the half-bridge power stage Q1 and Q2 output FETs except all the circuits are internal to the IC. CB1 is a representation of the internal capacitors used in the gate driving circuitry. Each gate driver output (Q) is designed to reach 100% duty cycle, therefore the PWM input pulse width has no maximum boundaries, as long as V_{DD}x and/or V_{BOOT}x are above the power on reset threshold limit. The high side circuit V_{BOOT}x can be supplied by an external floating voltage to allow infinite ON time for the high-side FET. At initial powerup, CB1 is not yet fully charged, consequently, propagation delay (from HS_{IN}x, or LS_{IN}x, to SWx) may increase, up to 250 ns. Only the first one, or two pulses may be affected. Figure 13 illustrates this behavior.

Figure 13: Behavior before complete charging of internal gate driver capacitors

SWx Node Switching Transients

The switching rate and transients at the output nodes, SWs, are controlled by application topologies, resulting in hard or soft switching transitions. The more stressful hard switching transition needs to be controlled by a combination of tuning the gate drive turn-on and turn-off circuits for the HS FET (Q1) and LS FET (Q2), and minimizing the power loop parasitic inductances. The on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Switching times are internally tuned to achieve SW switching rates of 10 V/ns spanning zero to full load current. The choice of switching rates is dictated by efficiency versus EMI mitigation. During HS FET (Q1) or LS FET (Q2) turn-on transitions with hard switching conditions, the fast di/dt of the HS FET or LS FET coupled with the power loop inductance ($V_{peak} = L_{power\ loop} \cdot di/dt$) would cause a transient over-voltage spike above V_{IN} or undervoltage spike below GND. Together with SW switching rate tuning, the over-voltage spikes can be controlled to less than +10 V above rail and -10 V below ground during hard switching transitions.

The EPC91122 Reference Design Board provides guidelines for PCB layout to use the EPC33110 in motor drives application circuits.

Application	C_{DRV}	C_{DD}	V_{BOOT} Capacitor	R_{BOOT}, R_{DRV} Resistors
Motor Drive	6.8 µF	100 nF	2.2 µF	embedded 10 Ω

Typical values of capacitors and resistors in application circuits using EPC33110.

Protection Circuits

The EPC33110 integrates driver protection circuits as well as power on reset (POR) circuits for V_{DD}x and V_{BOOT}x. These protection circuits allow for the proper operation of the drivers as shown in the Truth Table, regardless of the power supply sequencing of V_{DRV} with respect to V_{IN}. This allows the system designer to use V_{IN} to power-up V_{DRV} without concerns on sequencing, as may be necessary in certain applications. The Power On Reset (POR) circuit for the low-side internal V_{DD}x supply will activate all the HS and LS logic paths only when each V_{DD}x voltage rises above the rising threshold V_{DD_POR+}. The logic paths will become inactive when the V_{DD}x voltage falls by $V_{DD_POR_HYST}$ below the rising supply voltage threshold. The Power On Reset (POR) circuit for the high-side internal V_{BOOT}x supply will activate the HS driver path only when each bootstrap supply voltage, V_{BOOT}x, rises above the rising supply threshold of V_{BOOT_POR+}. The HS driver path will become inactive when the V_{BOOT}x bootstrap voltage falls by $V_{BOOT_POR_HYST}$ below the rising supply threshold.

Logic Inputs

The EPC33110 IC is capable of interfacing to digital and analog controllers with 3.3 V or 5 V CMOS logic levels. The logic level translators at the frontend level-shift the six PWM signals, HS_{IN}x and LS_{IN}x respectively, to internal voltage levels that allow for proper operation of the power module.

Separate and independent high-side (HS_{IN}x) and low-side (LS_{IN}x) logic control inputs allow external controllers to set fixed or adaptive deadtimes for optimal operating efficiency. Cross-conduction lockout logic per each phase commands both FETs off when the phase logic inputs are simultaneously high. Figure 14 shows how the logic inputs of one phase interact with each other. Here the timing diagram applies with the HS FET (Q1) and LS FET (Q2) in half-bridge configuration and current is in the positive direction going out of the half-bridge. When HS_{IN} and LS_{IN} are logic high at the same time, both Q1 and Q2 will shut off. A built-in deadtime of $t_{_lockout}$ is added, after which the current then commutes to Q2 in 3rd quadrant conduction and SW will be clamped at negative V_{SD} voltage of Q2.

Figure 14: EPC33110 Input-to-Output Timing Diagram

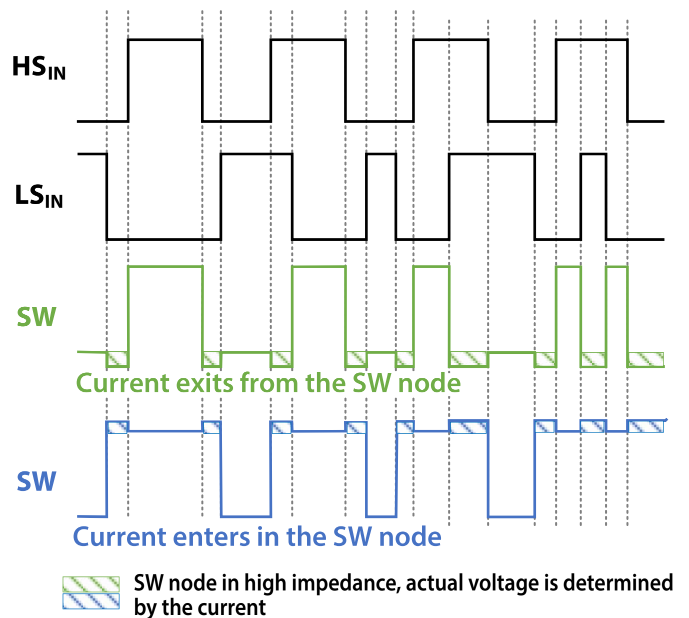


Figure 15 shows the effect of the input filters on the PWM inputs LS_{IN}x and HS_{IN}x. If the input pulses are smaller than t_{Filter} (15 ns typ), they do not pass through the filter and do not propagate to the respective power FET gates. Figure 16 shows the input filter linearity.

Figure 15: Input Filter Timing Diagram

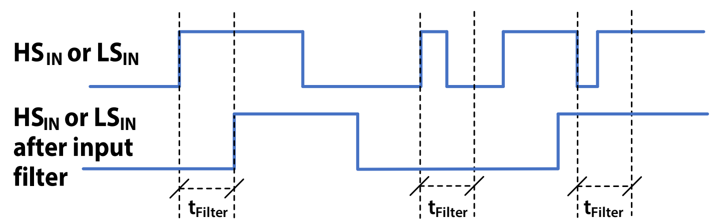


Figure 16: Input Filter Linearity

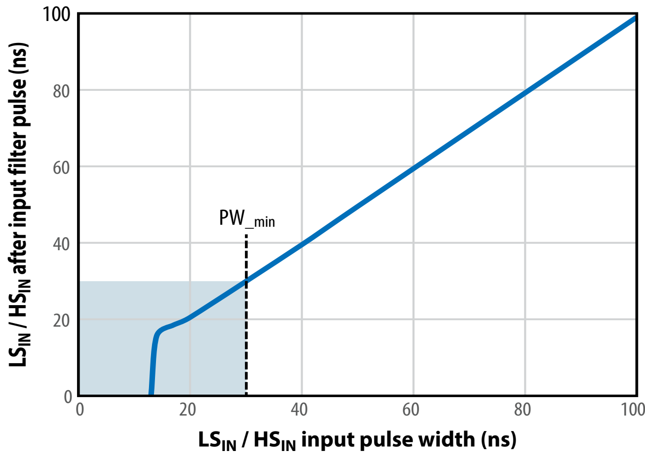


Figure 17 shows the effect of the cross-conduction lockout logic. If both inputs become active, an immediate turn-OFF signal is sent to the respective power FET gate. When the cross-conduction condition is removed (i.e., one of the inputs becomes inactive) the turn-ON signal is sent to the respective power FET gate after a $t_{_lockout}$ delay.

Figure 17: Cross-Conduction Logic Timing Diagram

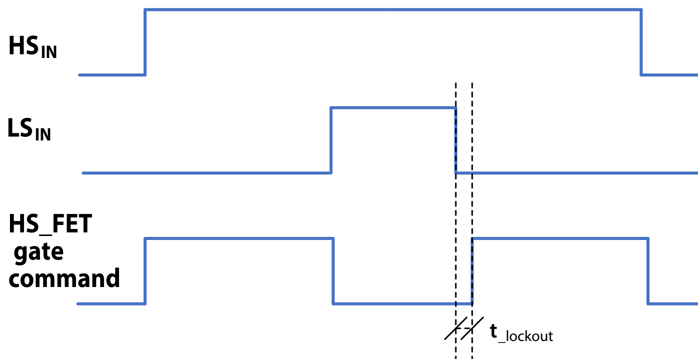
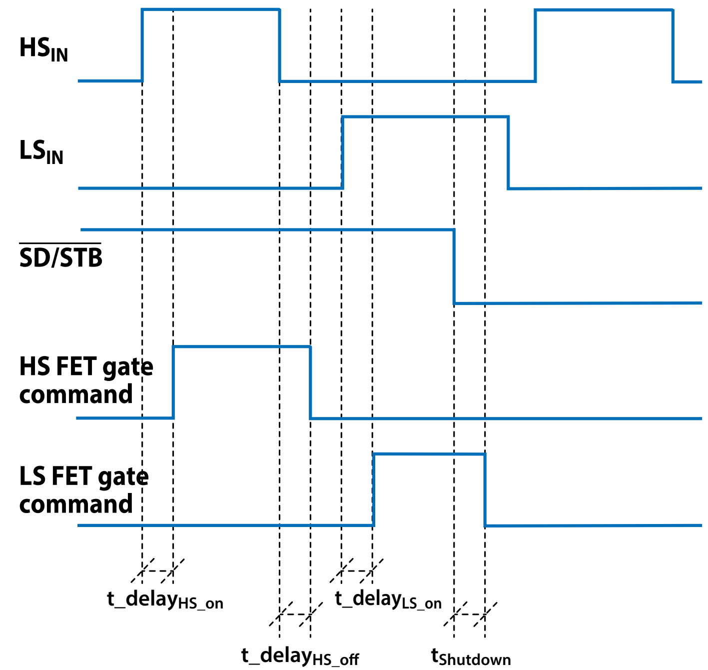
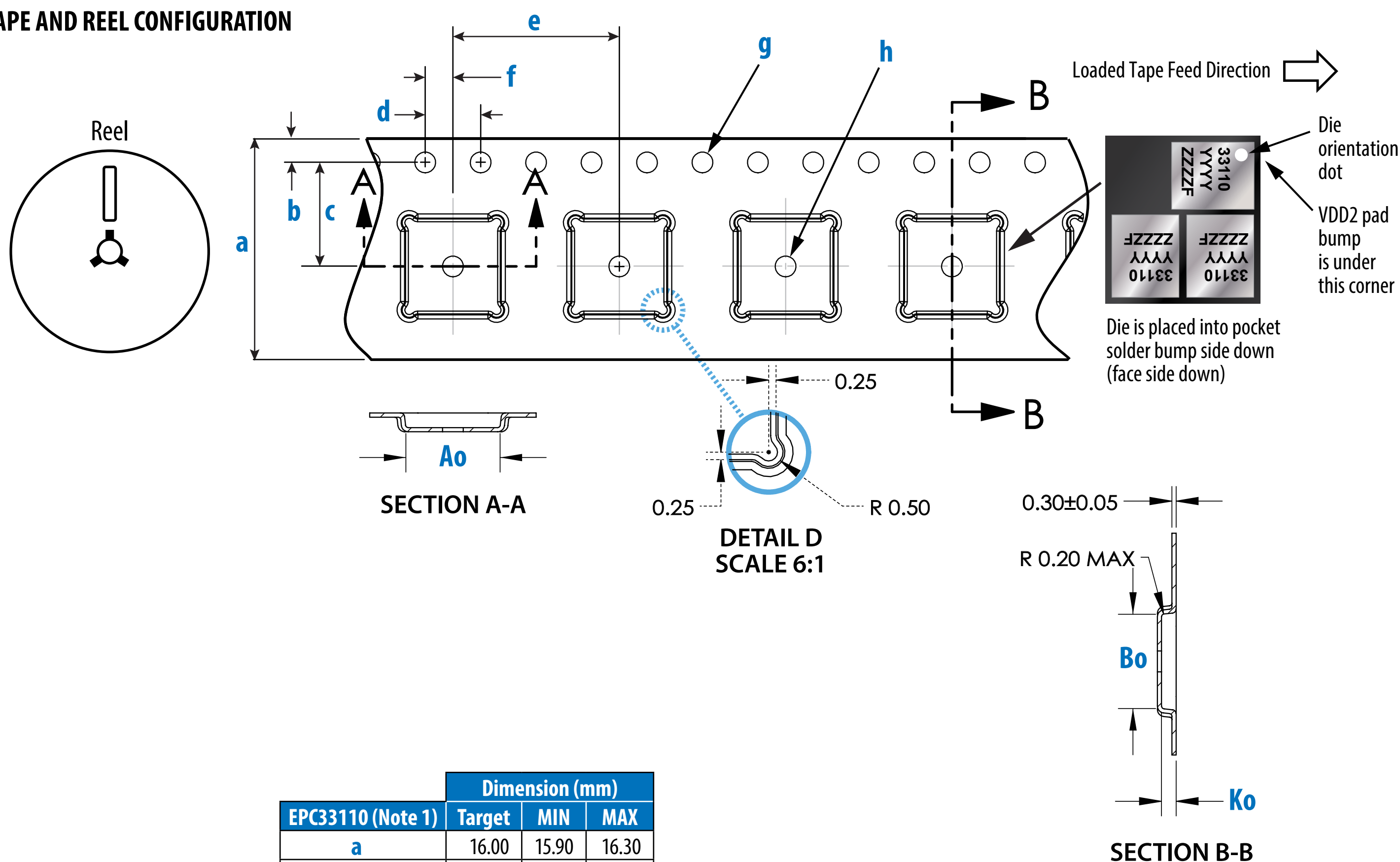


Figure 18 illustrates qualitatively the propagation delay between the PWM input pins of one phase and the corresponding power FET gate commands. It also displays the shutdown function timing. It should be noted that the propagation delay, as indicated in the dynamic characteristics table, is measured between the PWM input pins of one and the respective SW pin output.

Figure 18: Propagation Delays Timing Diagram



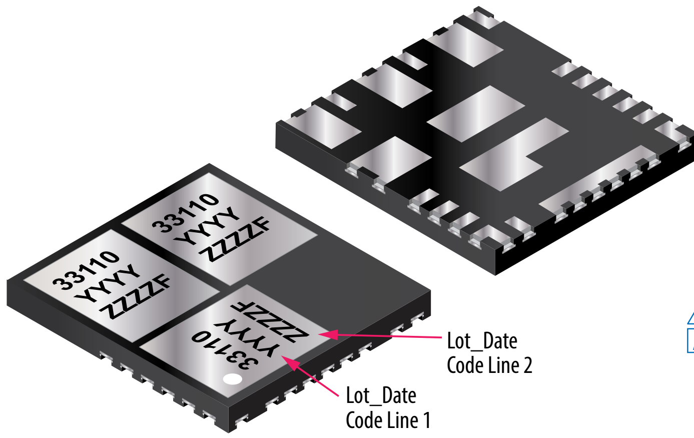
TAPE AND REEL CONFIGURATION

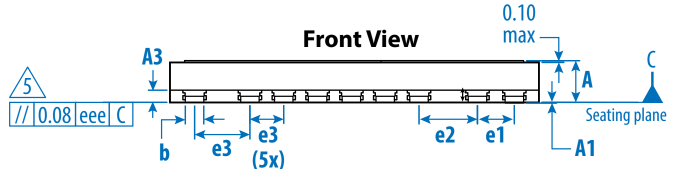


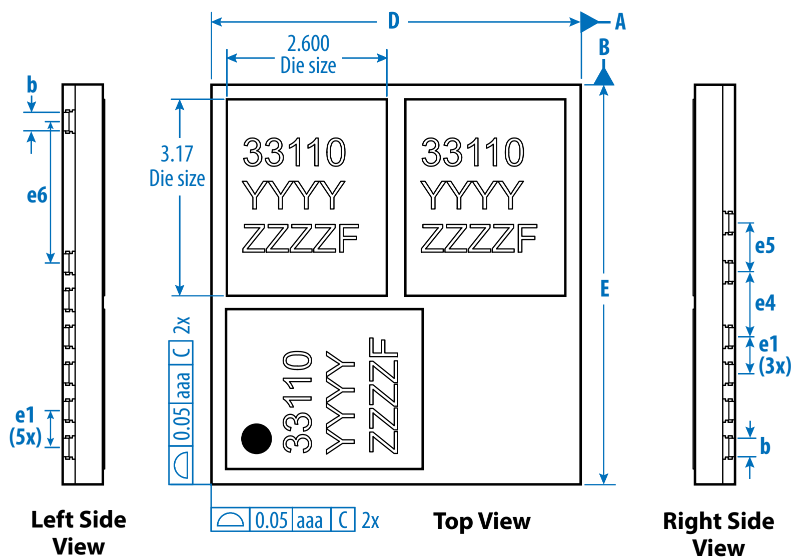
EPC33110 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	16.00	15.90	16.30
b	1.75	1.65	1.85
c (Note 2)	7.50	7.45	7.55
d	4.00	3.90	4.10
e	12.00	11.90	12.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.60
Ao	6.80	6.75	6.85
Bo	6.80	6.75	6.85
Ko	1.05	1.00	1.15

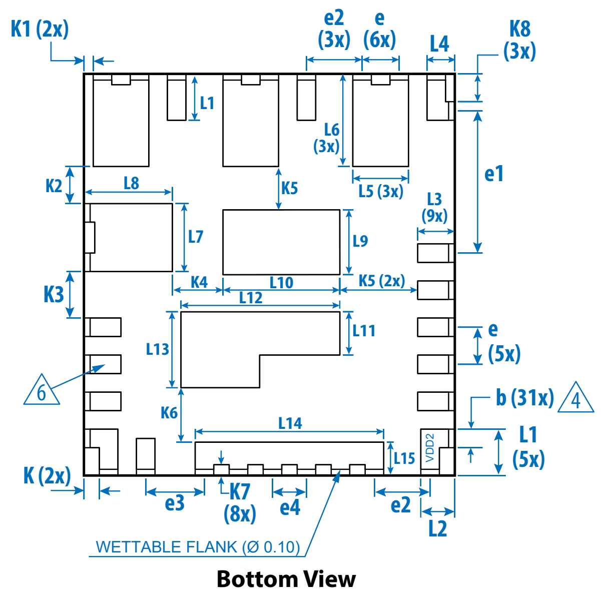
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.









SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.25	0.30	0.34	4
D	5.90	6.00	6.10	
E	5.6.40	6.50	6.60	
e		0.60		BSC
e1		2.30		BSC
e2		0.90		BSC
e3		0.95		BSC
e4		0.55		BSC
K		0.25		REF
K1		0.15		REF
K2		0.60		REF
K3		0.75		REF
K4		0.82		REF
K5		1.26		REF
K6		0.88		REF
K7		0.175		REF
K8		0.450		REF

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
L1	0.65	0.75	0.85	
L2	0.45	0.55	0.65	
L3	0.50	0.60	0.70	
L4	0.35	0.45	0.55	
L5	1.10	0.90	1.00	
L6	1.40	1.50	1.60	
L7	1.00	1.10	1.20	
L8	1.33	1.43	1.53	
L9	0.95	1.05	1.15	
L10	1.79	1.89	1.99	
L11	0.60	0.70	0.80	
L12	2.47	2.57	2.67	
L13	1.13	1.23	1.33	
L14	2.95	3.05	3.15	
L15	0.44	0.54	0.64	
aaa		0.05		
eee		0.08		
N		21		3

Notes:

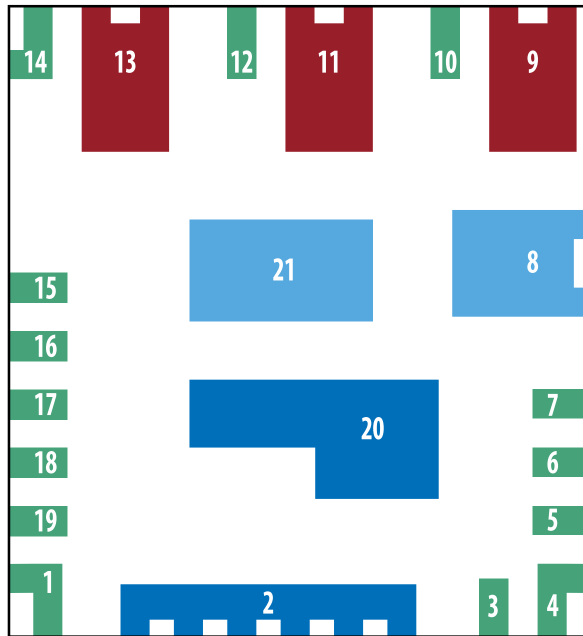
1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals

4\. (△) Dimension **b** applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area

5\. (△) Coplanarity applies to the terminals and all the other bottom surface metallization.

6\. (△) Lead plating is NiPdAu (1.5/0.01/0.005 µm min.) Au as the finish.

PACKAGE
Transparent view



Pin	Description
1	$V_{DD}2$
2	V_{IN}
3	$\overline{SD/STB}$
4	V_{DRV}
5	$HS_{IN}3$
6	$LS_{IN}3$
7	$V_{DD}3$
8	GND
9	SW3
10	$V_{BOOT}3$
11	SW2

Pin	Description
12	$V_{BOOT}2$
13	SW1
14	$V_{BOOT}1$
15	$HS_{IN}1$
16	$LS_{IN}1$
17	$V_{DD}1$
18	$HS_{IN}2$
19	$LS_{IN}2$
20	V_{IN}
21	GND

RECOMMENDED LAND PATTERN *(units in mm)*

1.00x1.75(3x)
0.40x1.00(2x)
0.40x1.00 (11X)
R0.050
0.70x0.40
1.15x1.99
1.68x1.20
0.85x0.40(8x)
2.67x0.80
0.85x0.40(2x)
1.372x0.53
3.15x0.79
0.80x0.40 (2X)
0.40x0.79 (6X)

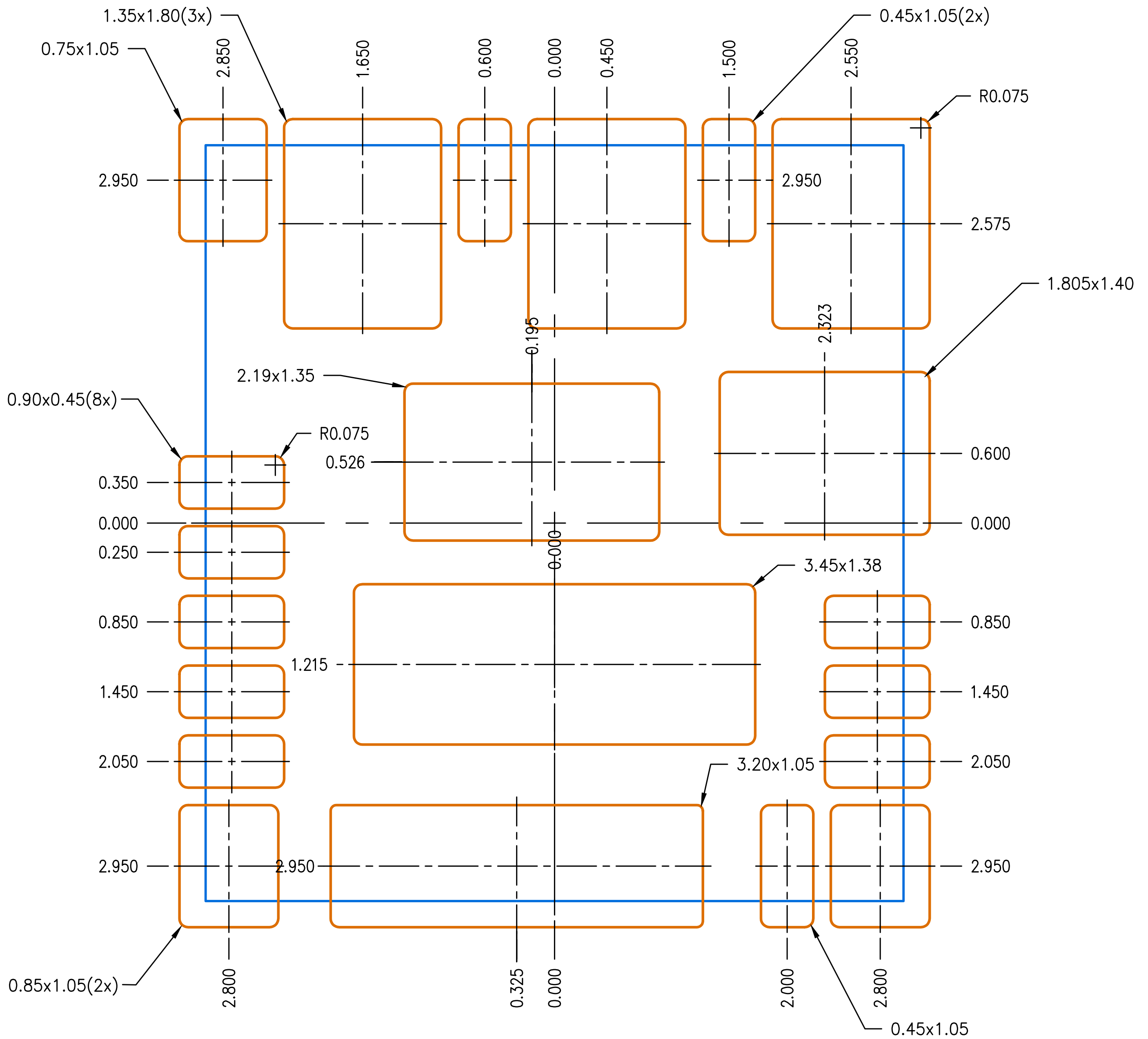
RECOMMENDED STENCIL *(units in mm)*

Recommended stencil should be 100 µm (4 mil) thick, must be laser cut, openings per drawing.
Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.
EPC has used this stencil design during tests.

0.46x1.85(3x) 0.42x1.85(2x) 0.42x1.00(2x)
0.41x1.85
0.47x1.10
2.865 2.715 2.095 1.480 0.600 0.000 0.620 1.500 2.100 2.720
R0.050
2.950 2.950
2.650 2.575 2.575
0.77x0.50
0.195 2.360
2.09x0.535(2x) 1.78x0.56(2x)
0.95x0.42(8x)
0.883 0.970
0.350 0.168 0.230
0.000 1.295x0.90 0.592 0.885 2.775 0.000
0.250 1.295x0.625(2x)
0.850 0.813 0.850
0.950
1.450 1.618 1.450
1.183
2.050 0.532 2.315 2.050
0.95x0.525 1.535x0.475(2x) 0.87x0.525
2.703 2.805 2.703
3.025
3.323 3.350 3.321
0.60x0.355(2x)
2.775 2.600 1.700 1.150 0.600 0.050 0.000 0.500 1.050 1.975 2.680
0.37x0.285(6x) 0.45x0.95

RECOMMENDED COPPER LAYER *(units in mm)*

Copper layout provided as typical example layout.



Change Log

STATUS	VERSION	DATE	REMARK
1.0	Preliminary datasheet	18 March 2026	Preliminary data before release to production

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