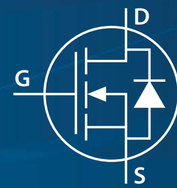
EPC7002 – Rad Hard Power Transistor

V_{DS} , 40 V
$R_{DS(on)}$, 14.5 mΩ max
I_D , 62 A
95% Pb/5% Sn Solder

Preliminary



EFFICIENT POWER CONVERSION

Halogen-Free

Rad Hard eGaN® transistors have been specifically designed for critical applications in the high reliability or commercial satellite space environments. GaN transistors offer superior reliability performance in a space environment because there are no minority carriers for single event, and as a wide band semiconductor there is less displacement for protons and neutrons, and additionally there is no oxide to breakdown. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact designs.

Maximum Ratings

	PARAMETER	VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous	10	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	62	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics

	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	9.3	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	80	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Epc7002 eGaN® FETs are supplied only in passivated die form with solder bars
Die Size:1.7 x 1.1 mm

Applications

- Space applications: DC-DC power, motor drives, lidar, ion thrusters
- Commercial satellite EPS & avionics
- Deep space probes
- High frequency rad hard DC-DC conversion
- Rad hard motor drives

Features

- Ultra high efficiency
- Ultra low $R_{DS(on)}$, Q_G, Q_{GD}, Q_{OSS}, and 0 Q_{RR}
- Ultra small footprint
- Light weight
- Total dose
  - Rated > 1 Mrad
- Single event
  - SEE immunity for LET of 85 MeV/(mg/cm^2) with V_{DS} up to 100% of rated breakdown
- Neutron
  - Maintains pre-rad specification for up to 3 x 10^{15} neutrons/cm^2

Benefits

- Superior radiation and electrical performance vs. rad hard MOSFETs: smaller, lighter, and greater radiation hardness

Static Characteristics (T_J = 25°C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.125 mA	40			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 40 V		1	125	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.005	0.3	mA
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.06	3.0	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.001	0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 10 A		8.5	14.5	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.8		V

All measurements were done with substrate shorted to source.
Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V		349		pF
C_{RSS}	Reverse Transfer Capacitance			3.8		
C_{OSS}	Output Capacitance			201		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 20 V, V_{GS} = 0 V		270		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			328		
Q_G	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 10 A		2.9		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 20 V, I_D = 10 A		1		
Q_{GD}	Gate-to-Drain Charge			0.4		
$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		6.6		
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

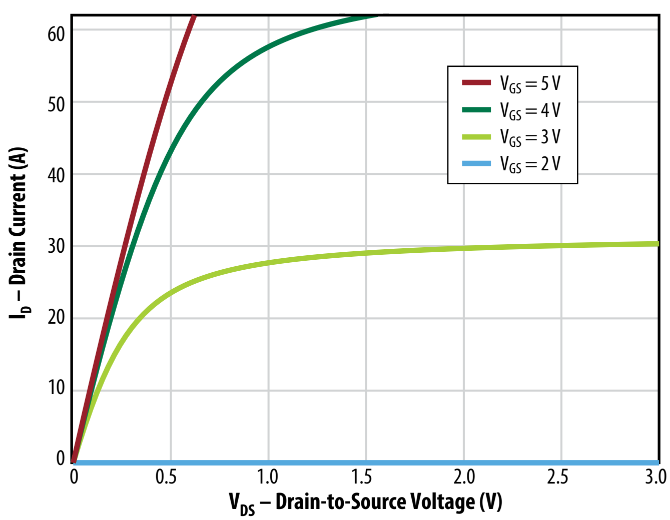


Figure 2: Typical Transfer Characteristics

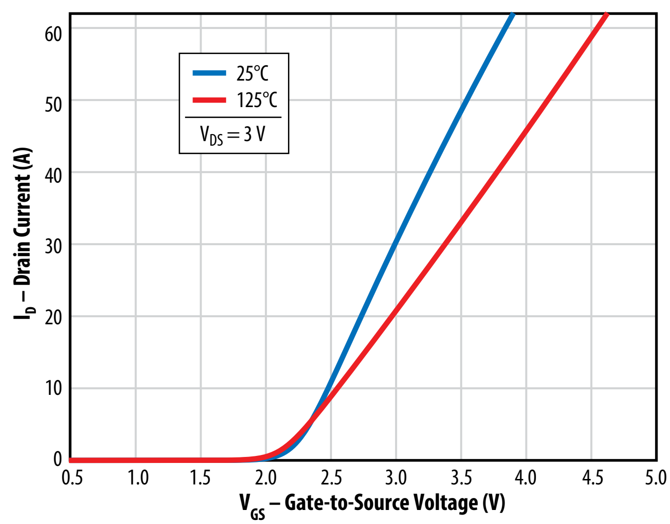


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

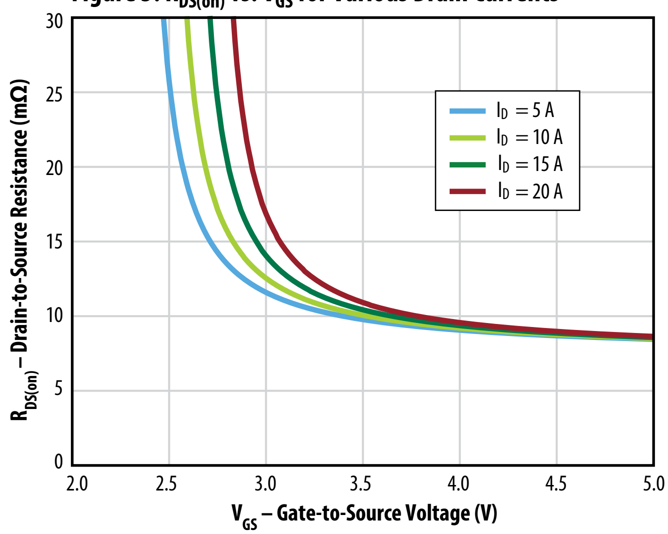


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

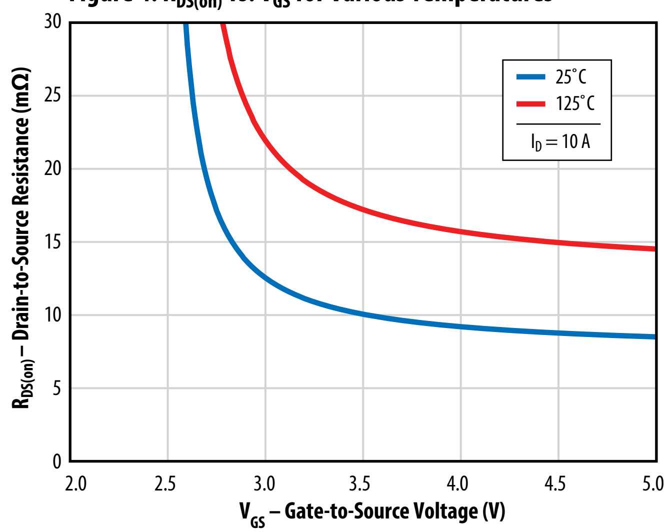


Figure 5a: Typical Capacitance (Linear Scale)

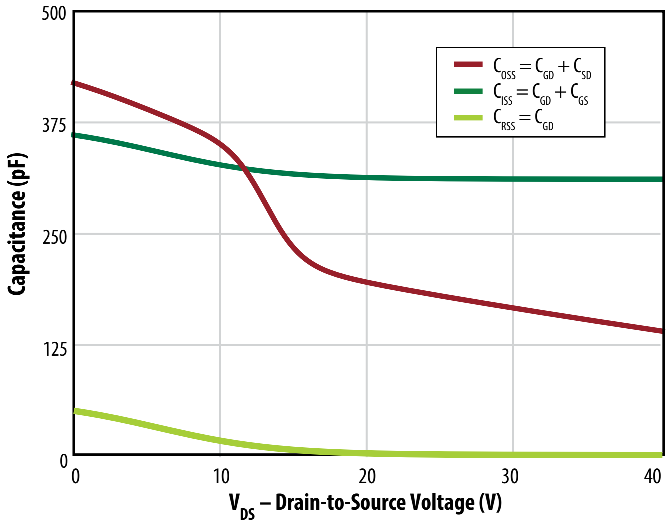


Figure 5b: Typical Capacitance (Log Scale)

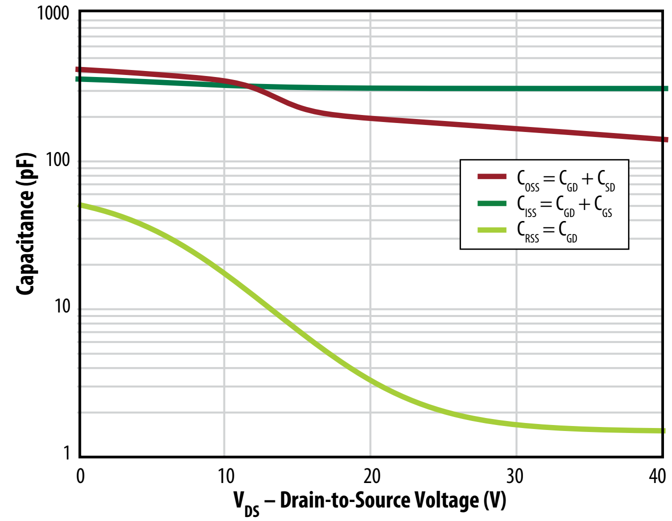


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

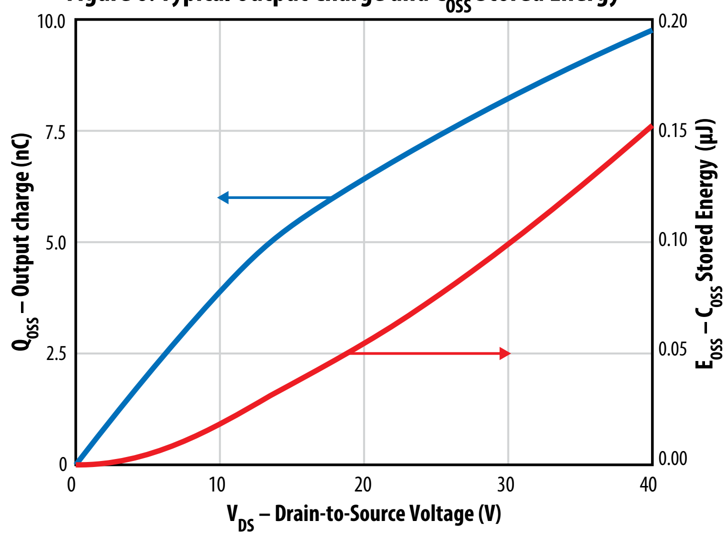


Figure 7: Typical Gate Charge

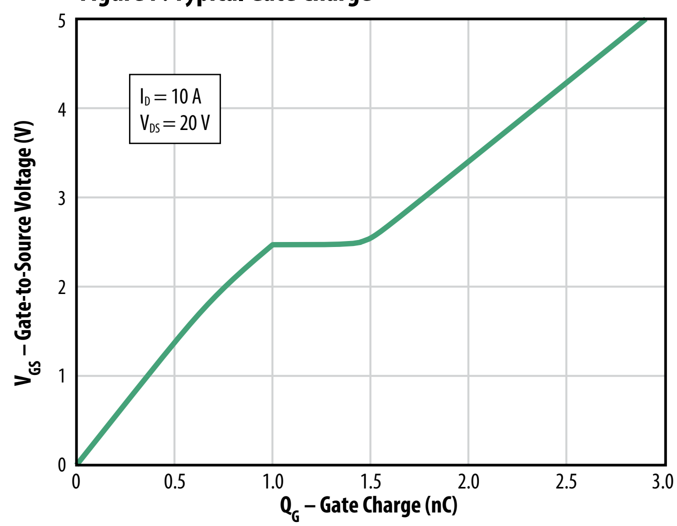
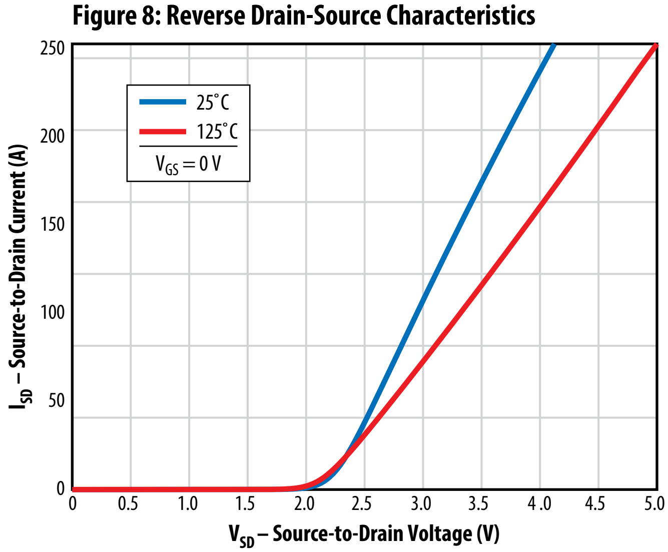


Figure 8: Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Normalized On-State Resistance vs. Temperature

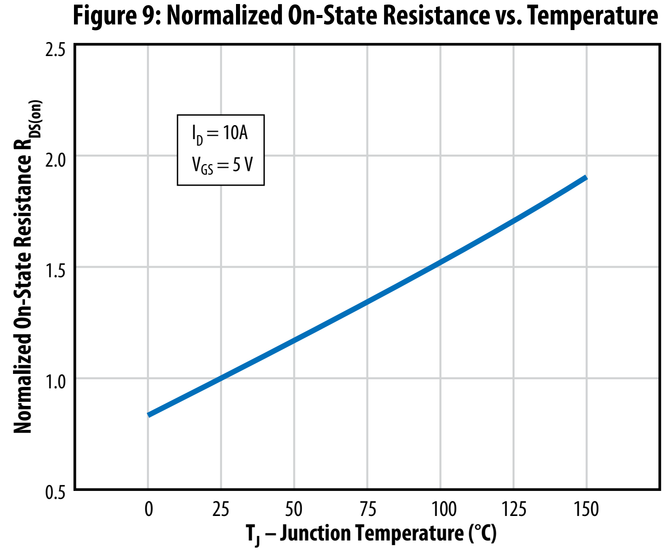


Figure 10: Normalized Threshold Voltage vs. Temperature

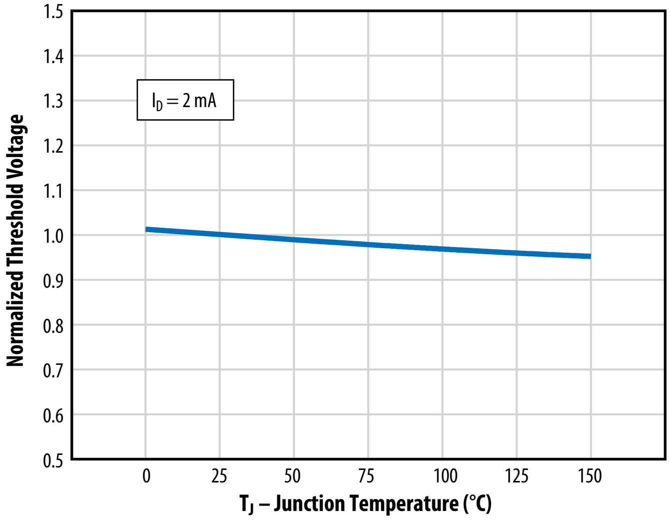
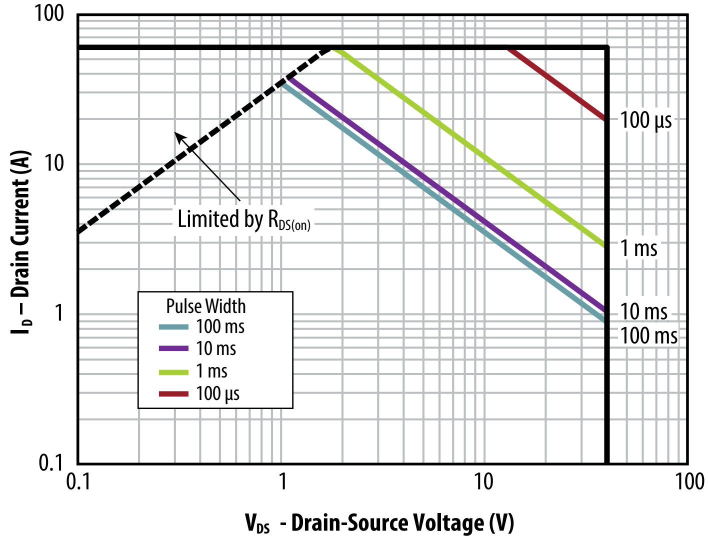
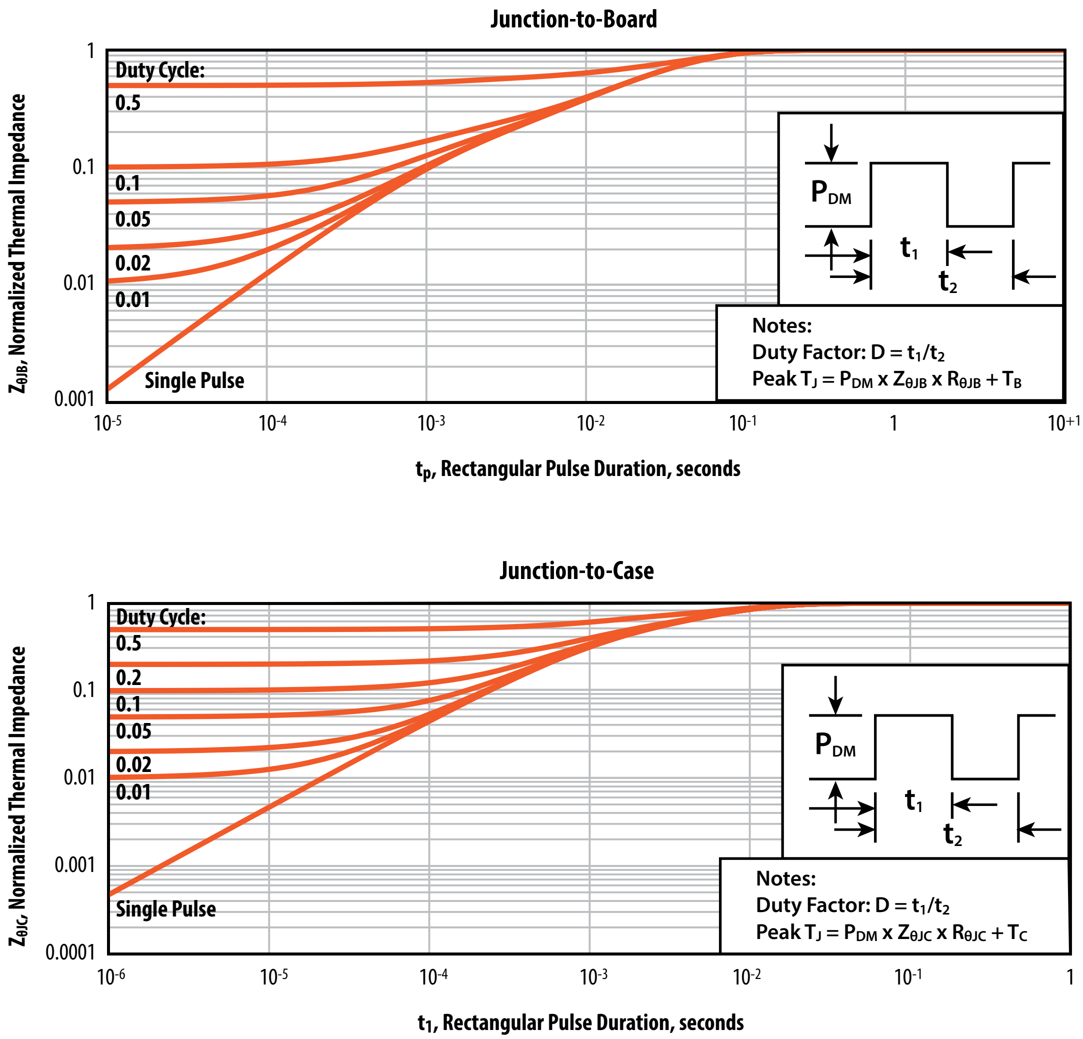


Figure 11: Safe Operating Area



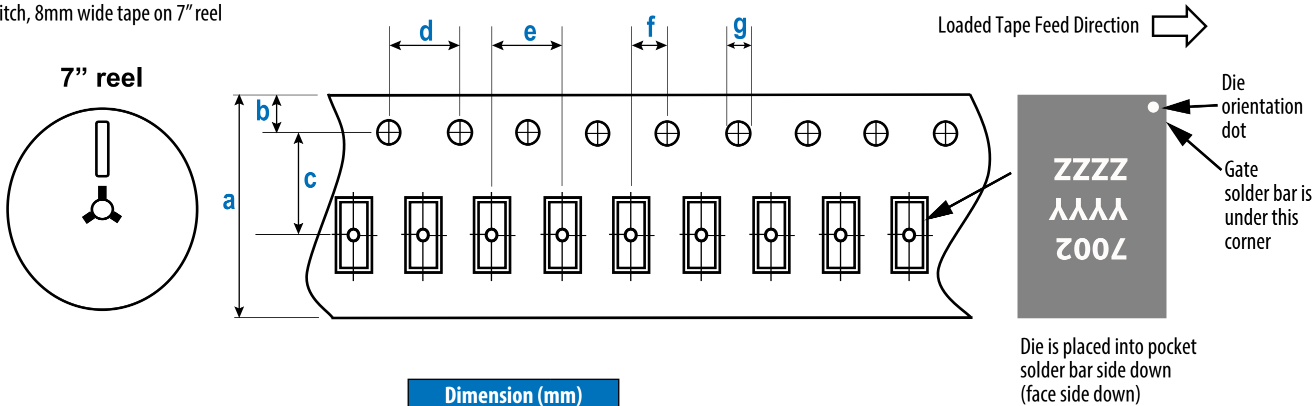
T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

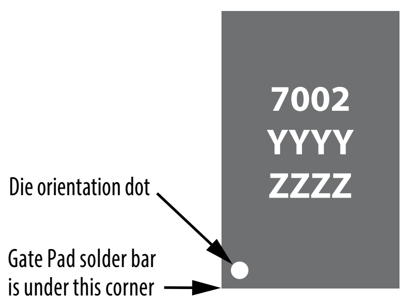


EPC7002 (Note 1)	Dimension (mm) Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

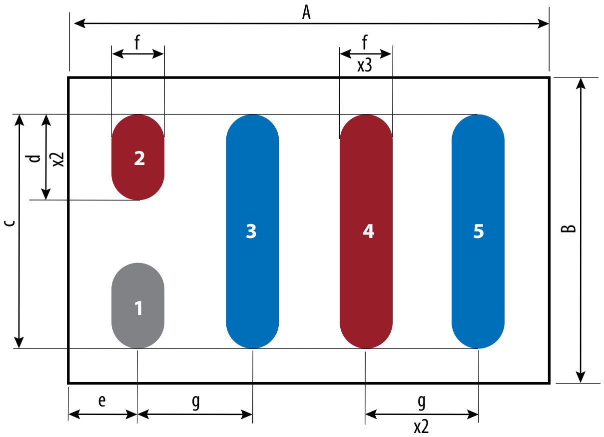
DIE MARKINGS



Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC7002	7002	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



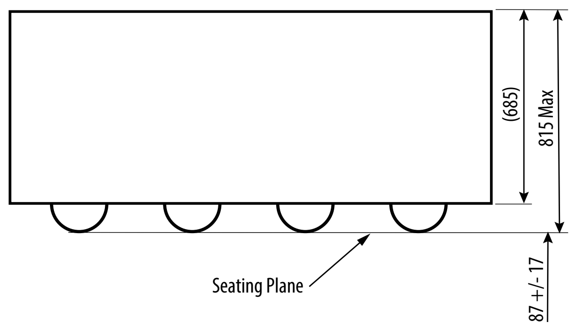
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1672	1702	1732
B	1057	1087	1117
c	829	834	839
d	311	316	321
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;

Pads no. 2 and 4 are Source;

Pads no. 3 and 5 are Drain

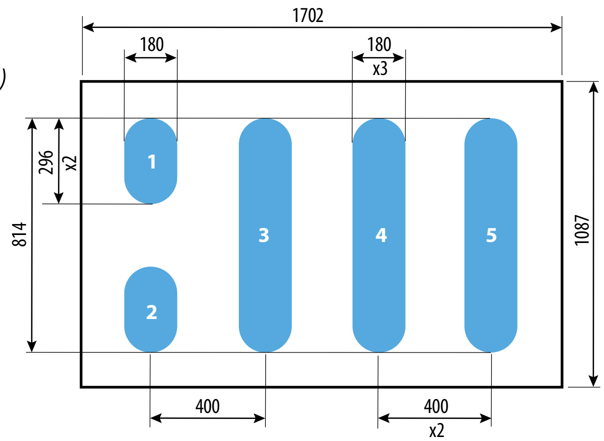
Side View



Substrate (top side) connected to Source

RECOMMENDED LAND PATTERN

(measurements in µm)



The land pattern is solder mask defined

Pad no. 1 is Gate;

Pads no. 2 and 4 are Source;

Pads no. 3 and 5 are Drain