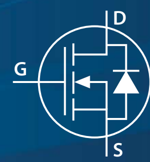
EPC7019 – Rad Hard Power Transistor

V_{DS} , 40 V
$R_{DS(on)}$, 1.5 mΩ max
I_D , 530 A
95% Pb / 5% Sn solder

Preliminary



EFFICIENT POWER CONVERSION

Halogen-Free

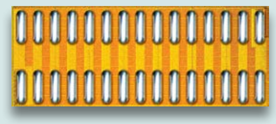
Rad Hard eGaN® transistors have been specifically designed for critical applications in the high reliability or commercial satellite space environments. GaN transistors offer superior reliability performance in a space environment because there are no minority carriers for single event, and as a wide band semiconductor there is less displacement for protons and neutrons, and additionally there is no oxide to breakdown.

These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact designs.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous (T_A = 25°C)	95	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	530	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	0.4	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



EPC7019 eGaN® FETs are supplied only in passivated die form with solder bars.

Die size: 6.05 x 2.3 mm

Applications
- Commercial satellite EPS & avionics
- Deep space probes
- High frequency Rad Hard DC-DC conversion
- Rad Hard motor drives

Features
- Ultra high efficiency
- Ultra low Q_G
- Ultra small footprint
- Light weight
- Total dose
  - Rated > 1 Mrad
- Single event
  - SEE immunity for LET of 85 MeV/(mg/cm²) with V_{DS} up to 100% of rated breakdown
- Neutron
  - Maintains Pre-Rad specification for up to 3 x 10^{15} Neutrons/cm²

Benefits
- Superior radiation and electrical performance vs. rad hard MOSFETs: smaller, lighter, and greater radiation hardness

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 1 mA	40			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 40 V		0.001	0.4	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.05	1.0	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125˚C		0.2	4.0	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.05	1.0	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 18 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D =36 A		1.2	1.5	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		2.0		V

Defined by design. Not subject to production test.

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V		2830		pF
C_{RSS}	Reverse Transfer Capacitance			35		
C_{OSS}	Output Capacitance			1660		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 20 V, V_{GS} = 0 V		2130		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			2540		
Q_G	Total Gate Charge	V_{DS} = 20 V, V_{GS} = 5 V, I_D = 36 A		22		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 20 V, I_D = 36 A		7.6		
Q_{GD}	Gate-to-Drain Charge			3.4		
$Q_{G(TH)}$	Gate Charge to Threshold			5.8		
Q_{OSS}	Output Charge	V_{DS} = 20 V, V_{GS} = 0 V		51		
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.
Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

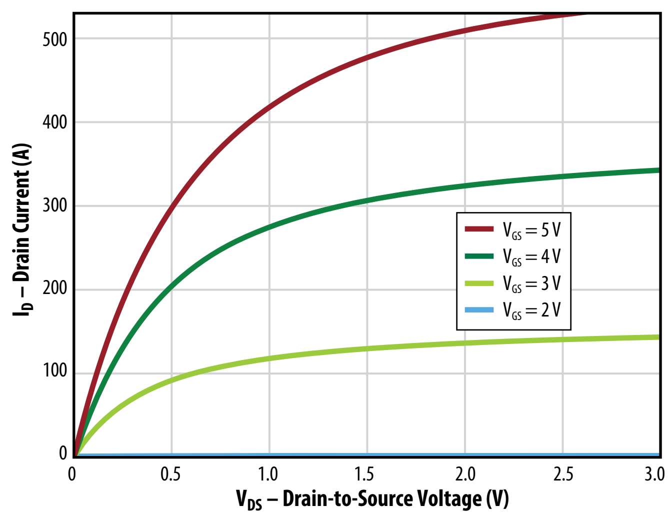


Figure 2: Typical Transfer Characteristics

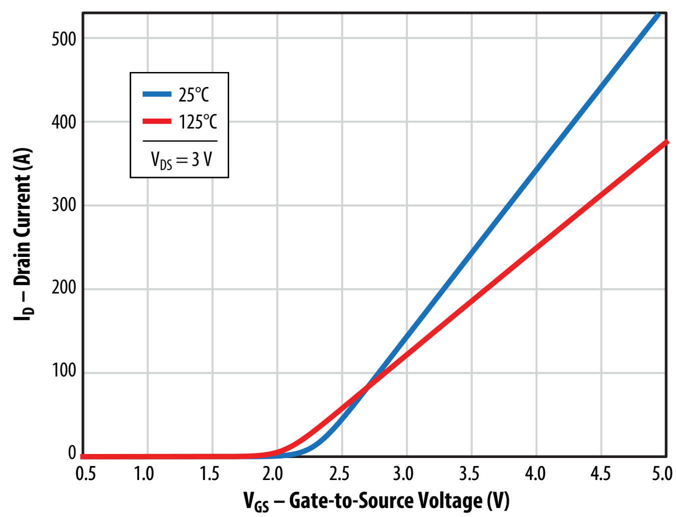


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

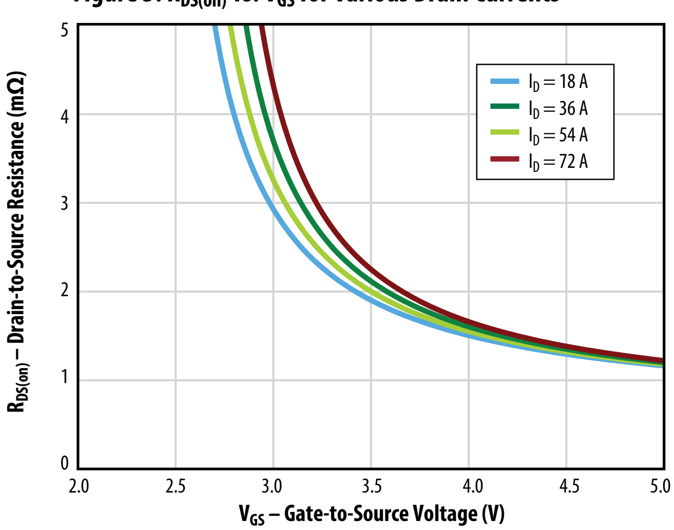


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

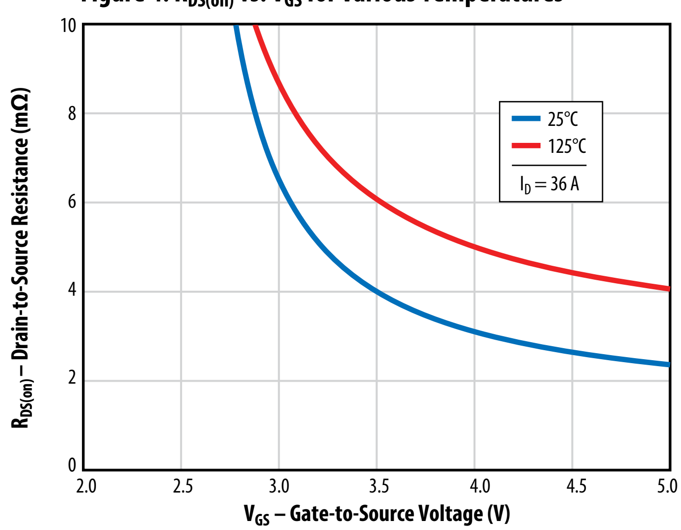


Figure 5a: Typical Capacitance (Linear Scale)

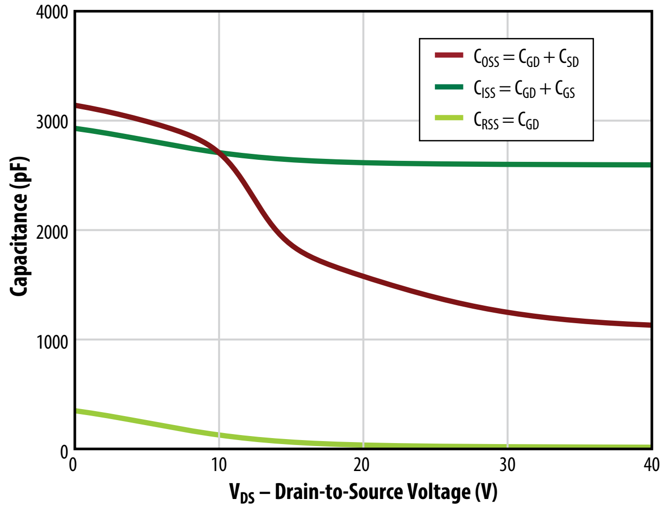


Figure 5b: Typical Capacitance (Log Scale)

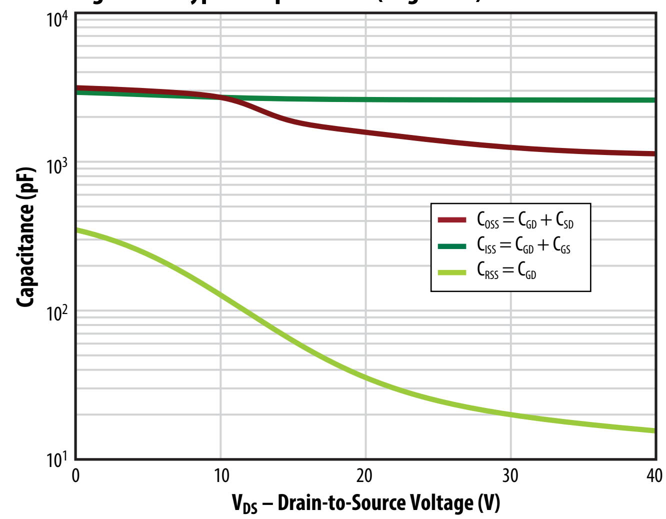


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

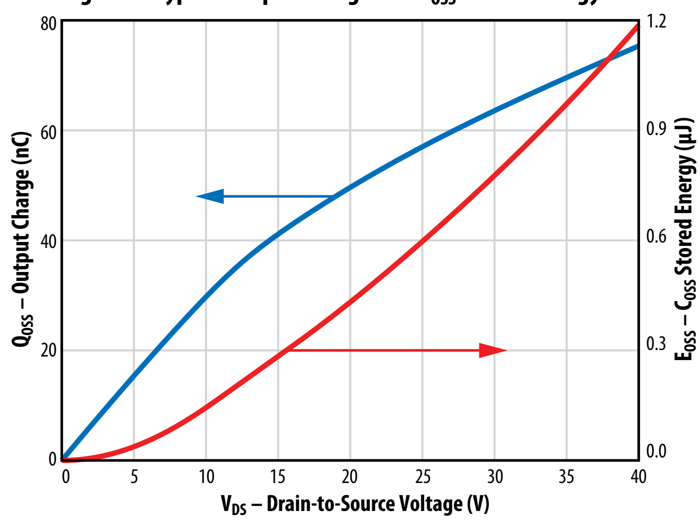


Figure 7: Typical Gate Charge

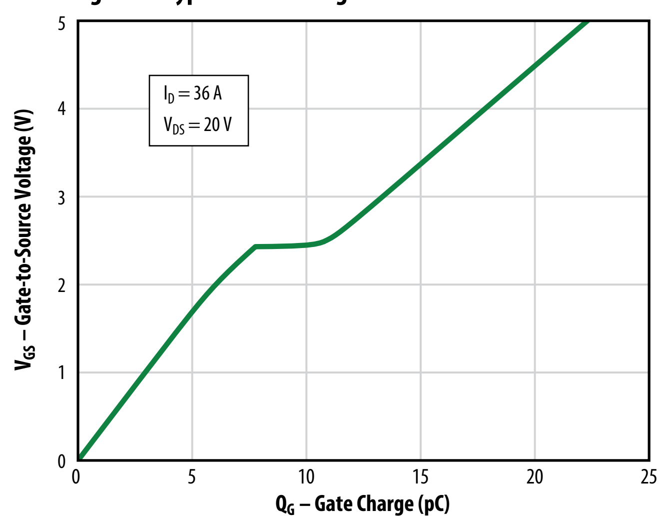
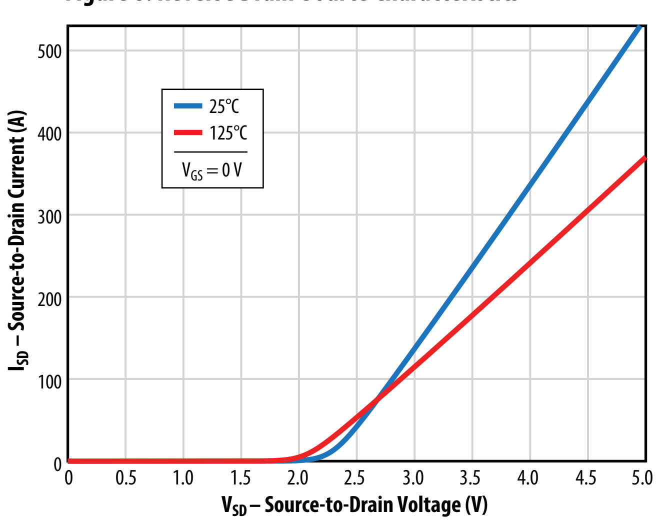


Figure 8: Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 9: Normalized On-State Resistance vs. Temperature

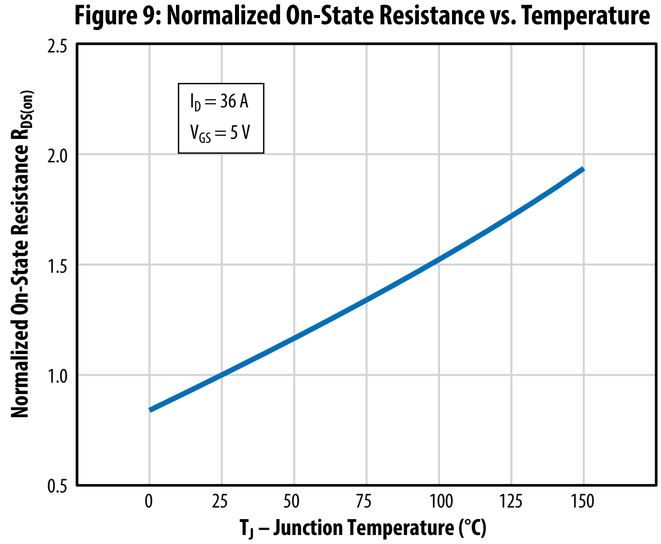


Figure 10: Normalized Threshold Voltage vs. Temperature

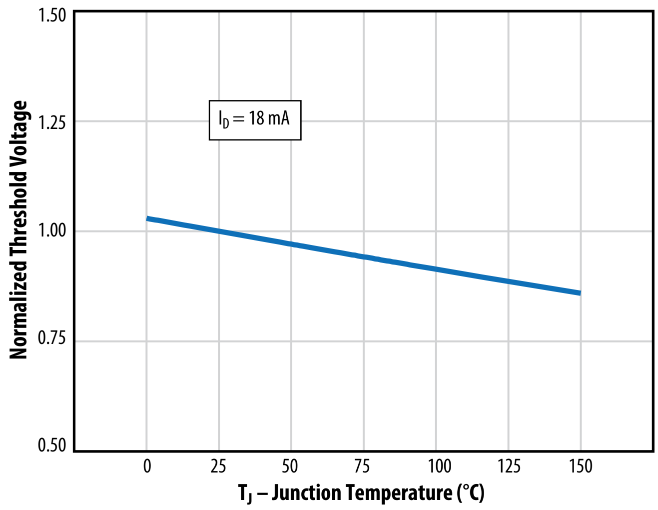
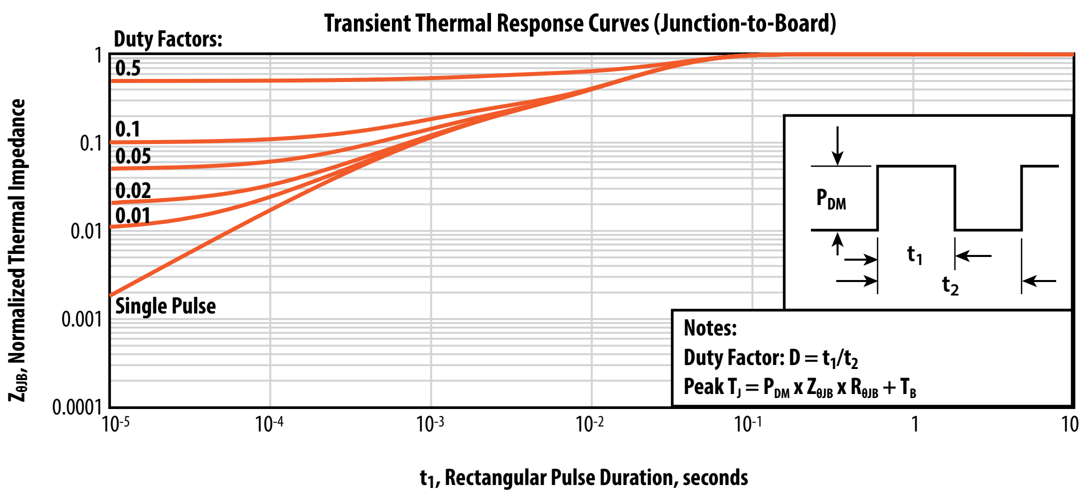


Figure 11: Transient Thermal Response Curves



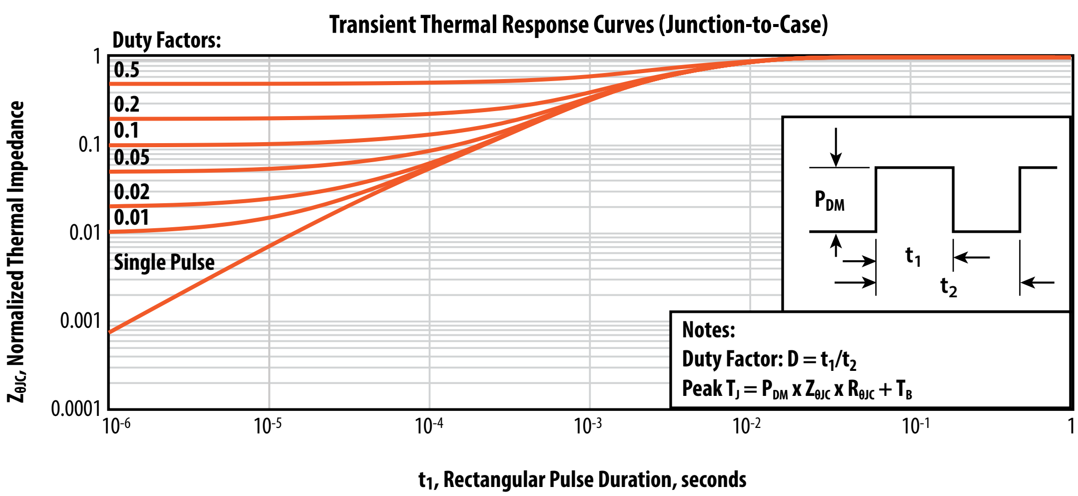
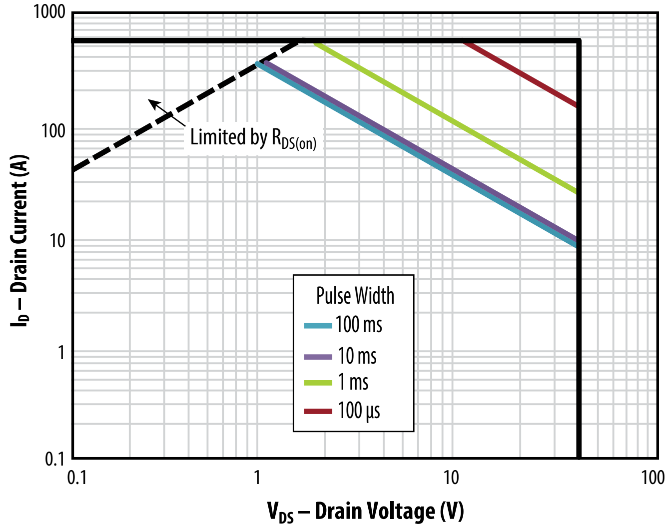
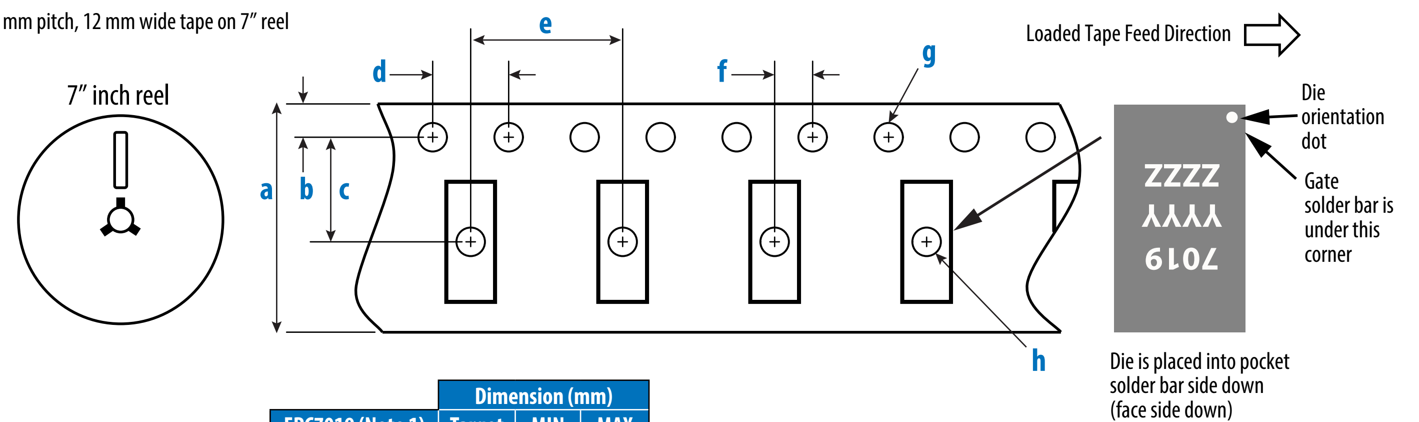


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

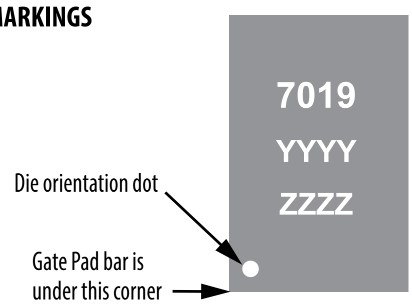


	Dimension (mm)		
EPC7019 (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

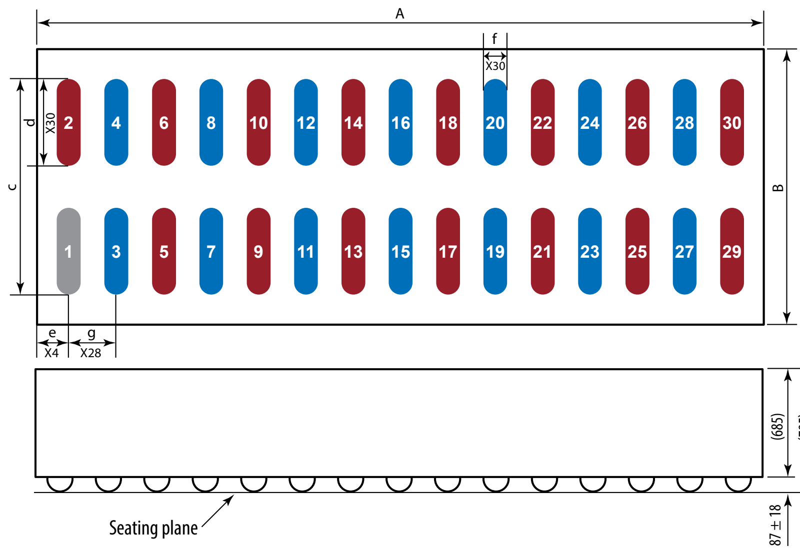
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC7019	7019	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



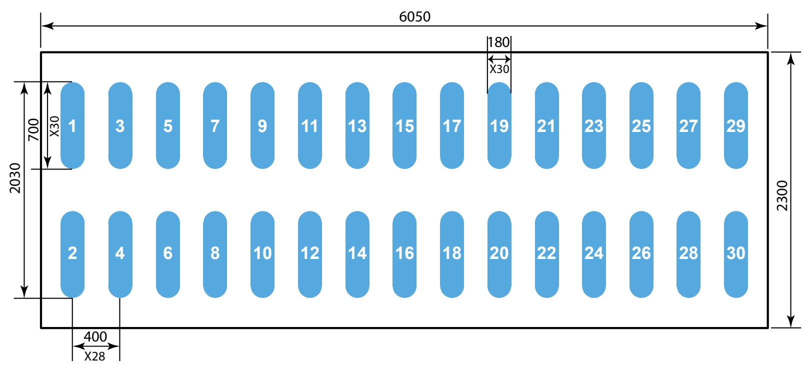
Side View

DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

Pad 1 is Gate;
Pads 2 ,5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30 are Source;
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined.

Pad 1 is Gate;
Pads 2, 5, 6, 9,10,13,14, 17, 18, 21, 22, 25, 26, 29. 30 are Source;
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain

Information subject to change without notice.
Revised June, 2022