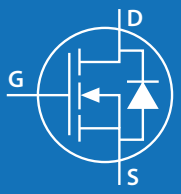
EPC2375 – 100 V GaN Power Transistor

V_{DS} , 100 V
I_D , 204 A
$R_{DS(on)}$, 0.9 mΩ typ

PRELIMINARY



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

July 29, 2026

General Description

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

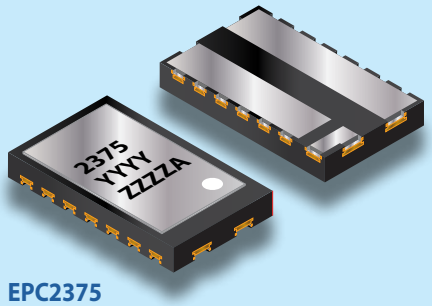
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous (T_J < 125°C)	204	A
	Pulsed (25°C, T_{PULSE} = 10 µs)	630	
	Pulsed (125°C, T_{PULSE} = 10 µs)	505	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = TBD	100			V
I_{DSS}	Drain-to-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.01		mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.045		
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.15		
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.002		
$V_{GS(TH)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 15 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-to-Source Resistance	V_{GS} = 5 V, I_D = 45 A		0.9	1.15	mΩ
V_{SD}	Source-to-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.6		V

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.



EPC2375
Package size: 3 x 5 mm

Features

- Ultra-low Q_G for high frequency
- PQFN package with backside thermal pad
- No reverse recovery

Applications

- High power PSU AC-DC synchronous rectification
- High frequency DC-DC conversion up to 80 V input (buck, boost, buck-boost and LLC)
- Motor drives
- High power density DC-DC modules from 40 V – 60 V to 5 V – 12 V
- Synchronous rectification
- Solar MPPT

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2375

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.5	

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 50 V		3239		pF
C_{RSS}	Reverse Transfer Capacitance			12		
C_{OSS}	Output Capacitance			917		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related	V_{GS} = 0 V, V_{DS} = 0 to 50 V		1277		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related			1616		
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 50 V, I_D = 45 A		25		nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 45 A		7.6		
Q_{GD}	Gate-to-Drain Charge			3.4		
$Q_{G(TH)}$	Gate Charge at Threshold			5.4		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 50 V		81		
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

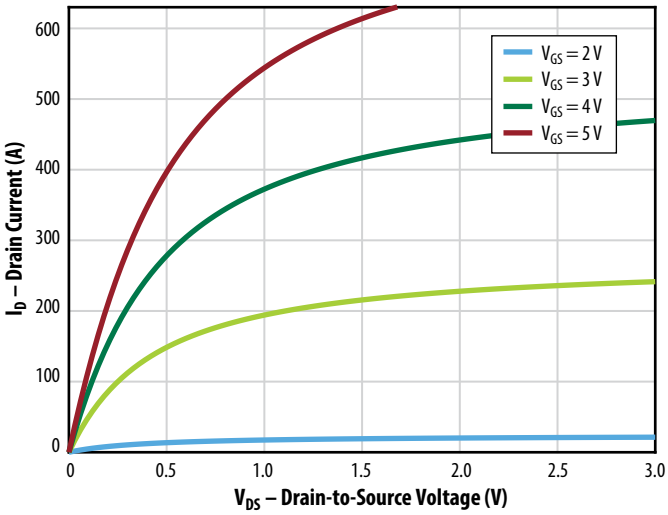


Figure 2: Typical Transfer Characteristics

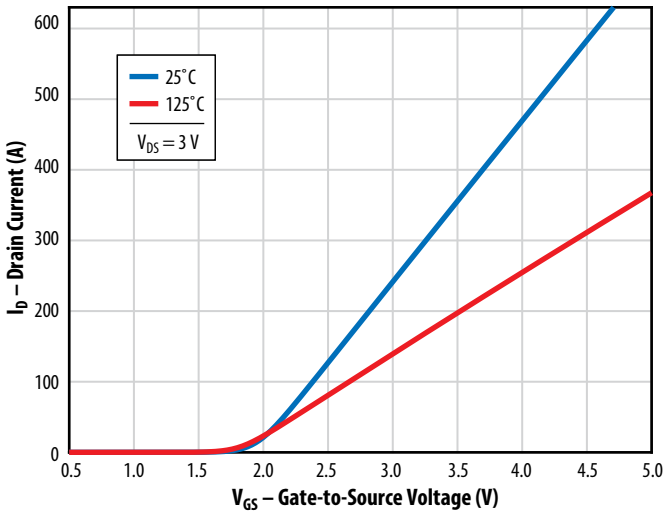


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

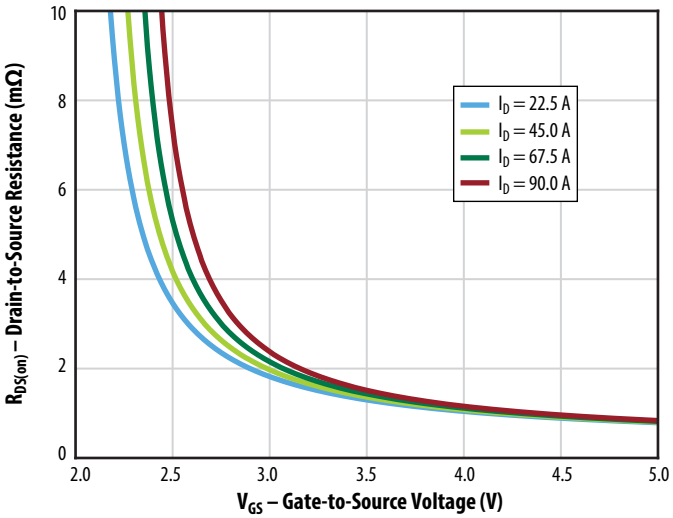


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

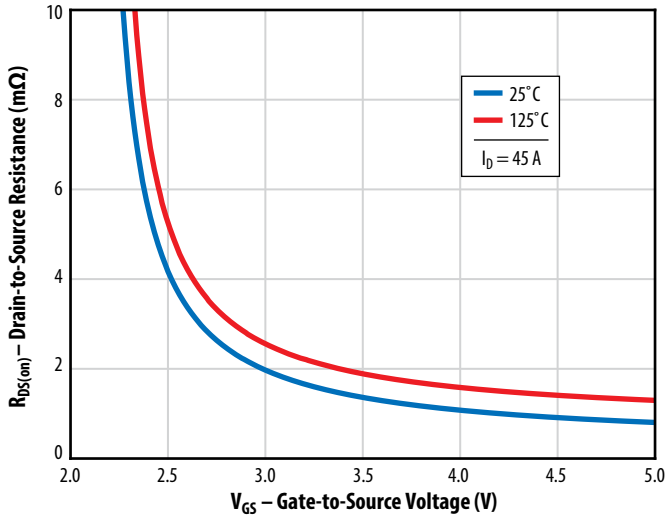


Figure 5a: Typical Capacitance (Linear Scale)

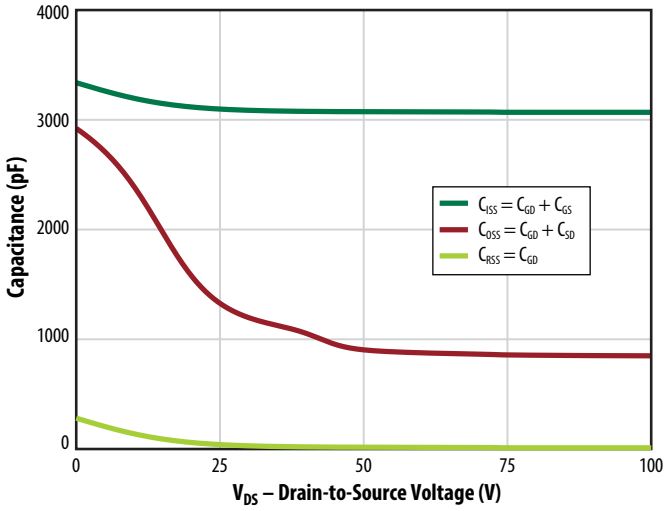


Figure 5b: Typical Capacitance (Log Scale)

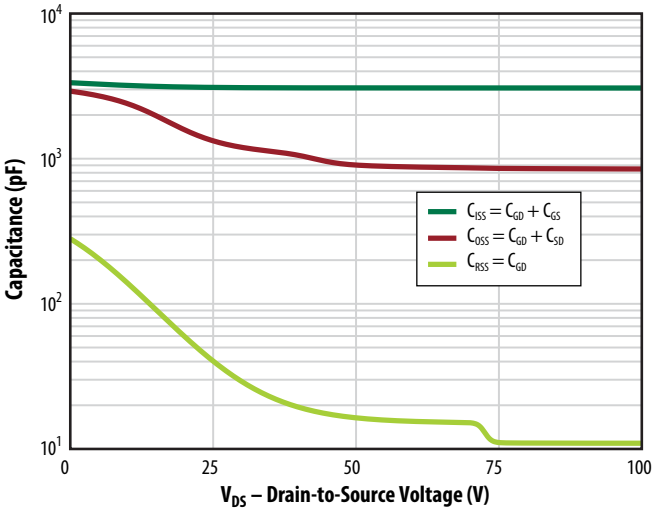


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

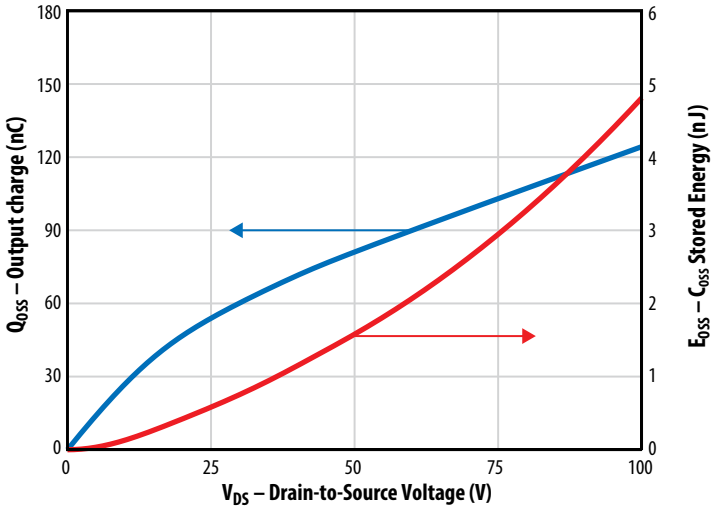


Figure 7: Typical Gate Charge

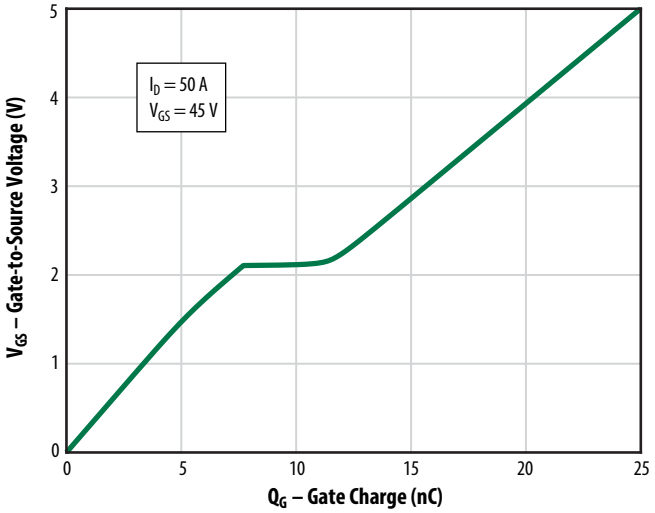
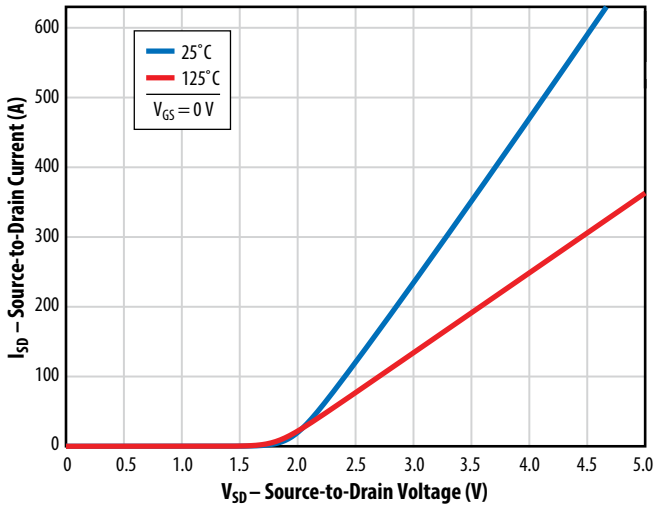


Figure 8: Typical Reverse Drain-Source Characteristics



Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF

Figure 9: Typical Normalized On-State Resistance vs. Temp.

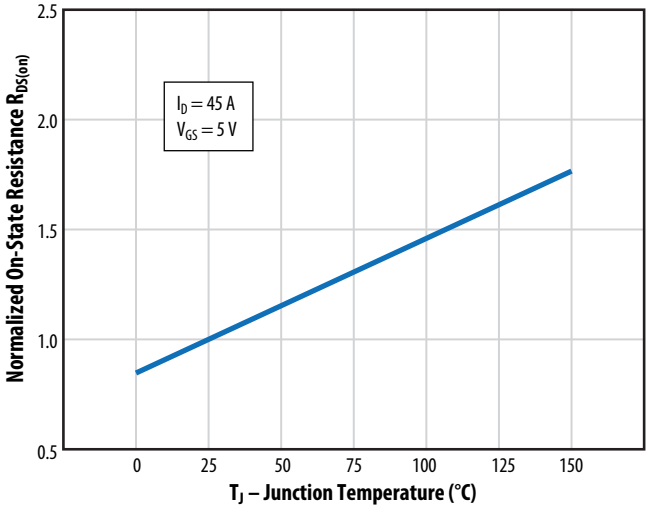


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

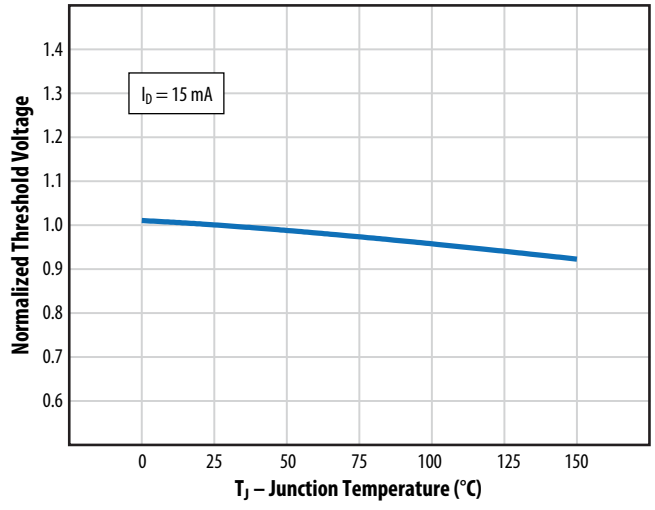
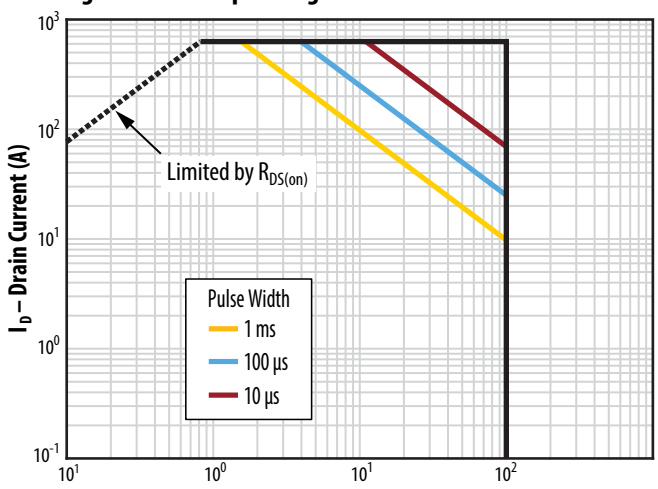
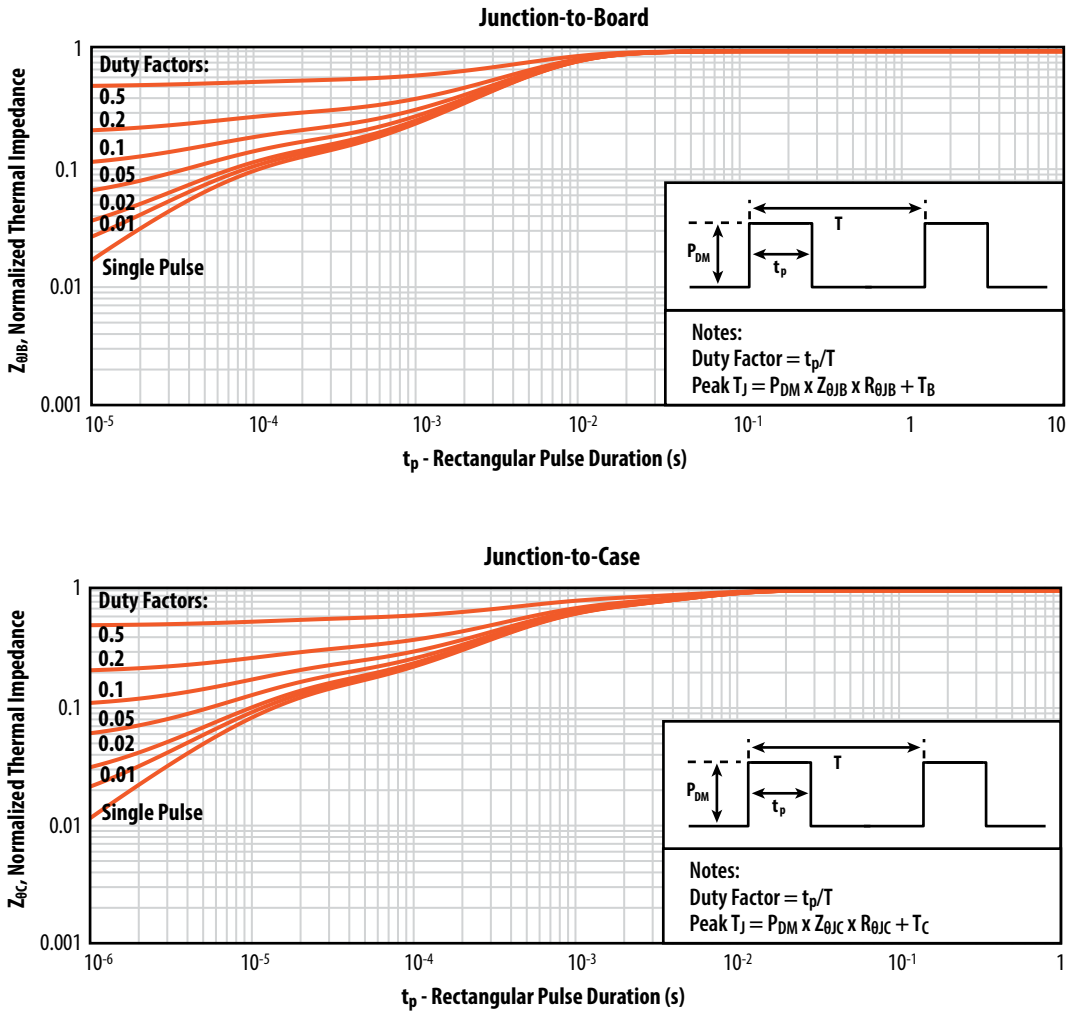


Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Typical Transient Thermal Response Curves



TYPICAL THERMAL CONCEPT

The EPC2375 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

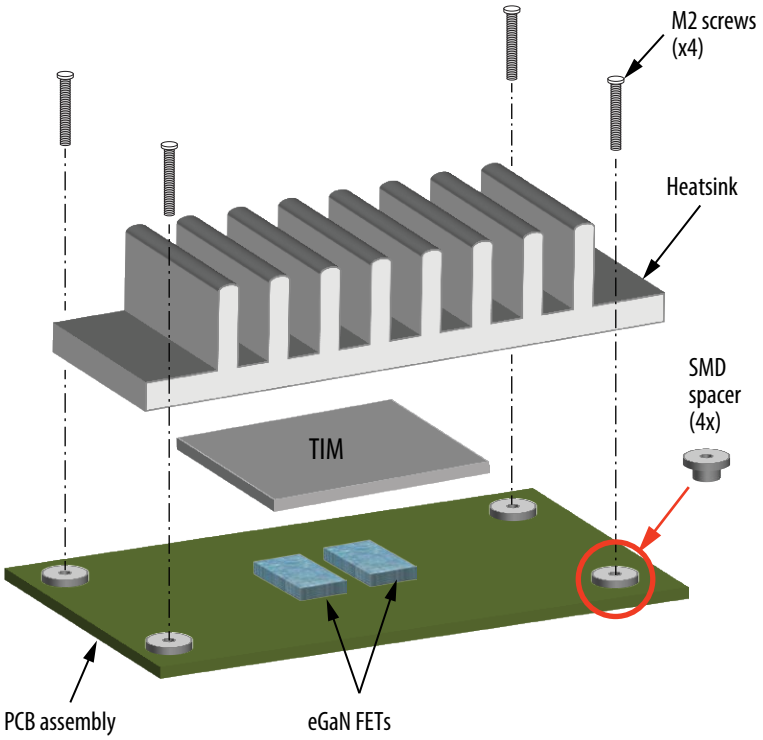


Figure 13: Exploded view of heatsink assembly using screws

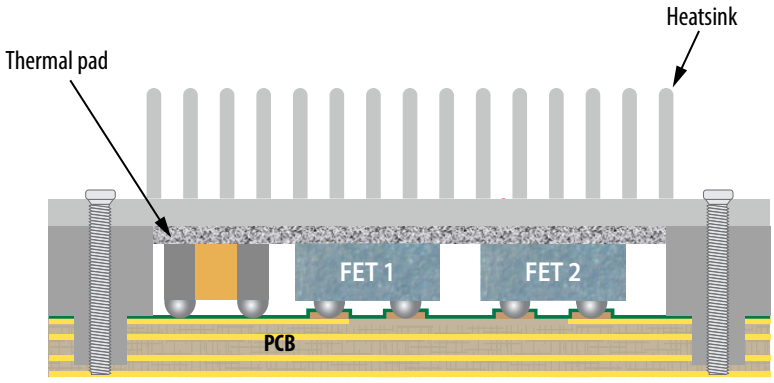


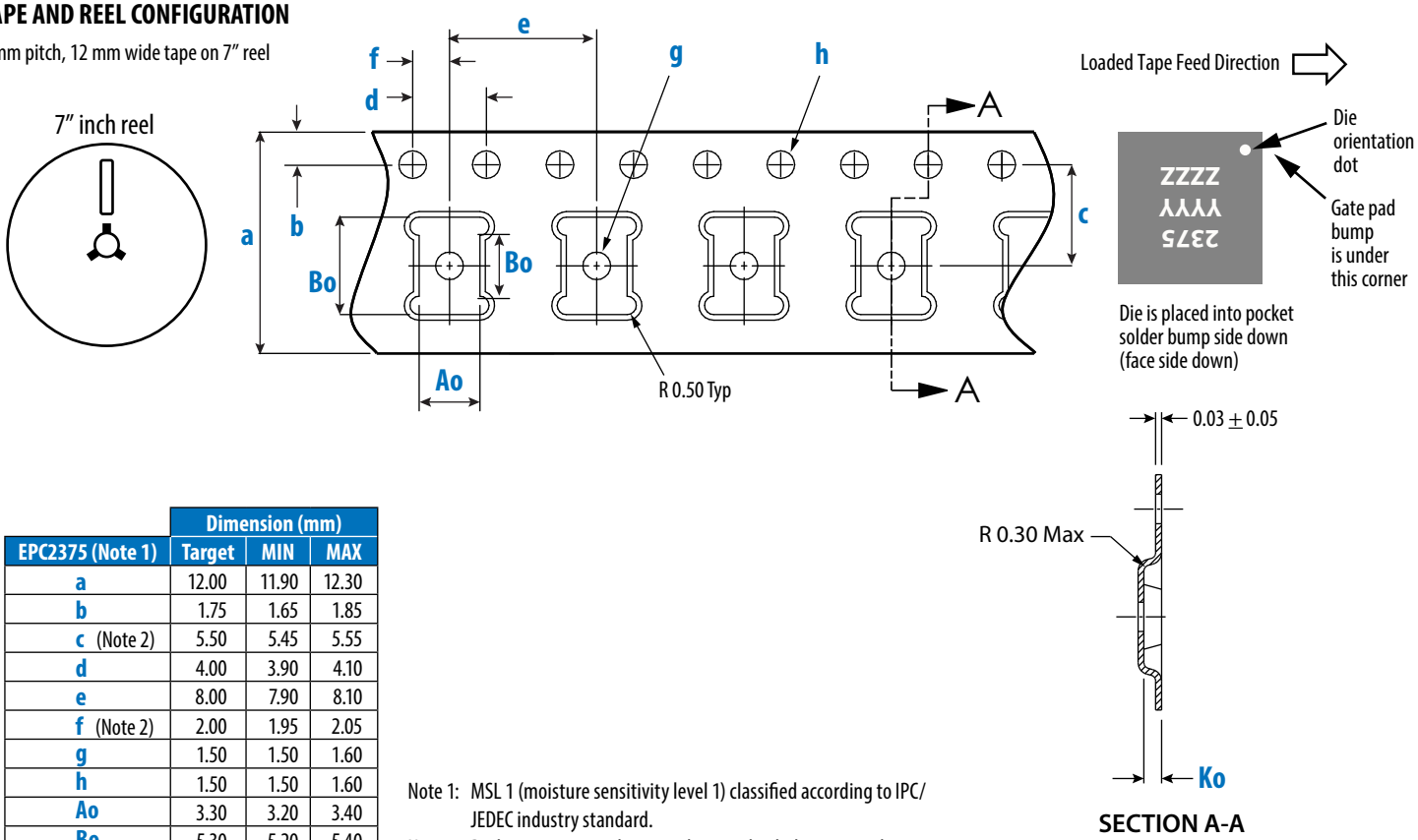
Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

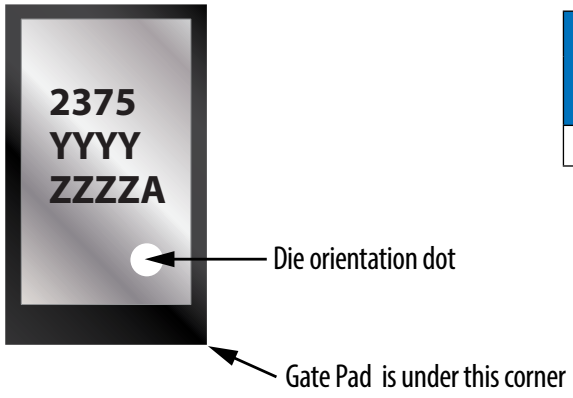


EPC2375 (Note 1)	Dimension (mm) Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.60
Ao	3.30	3.20	3.40
Bo	5.30	5.20	5.40
Ko	0.90	0.80	1.00

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

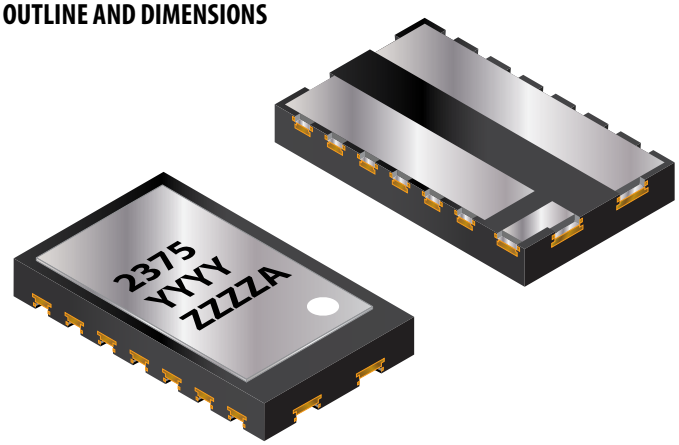
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

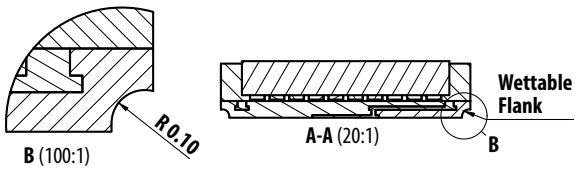
Part Marking

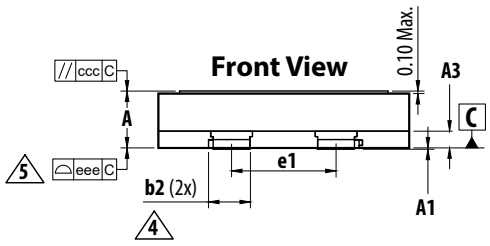


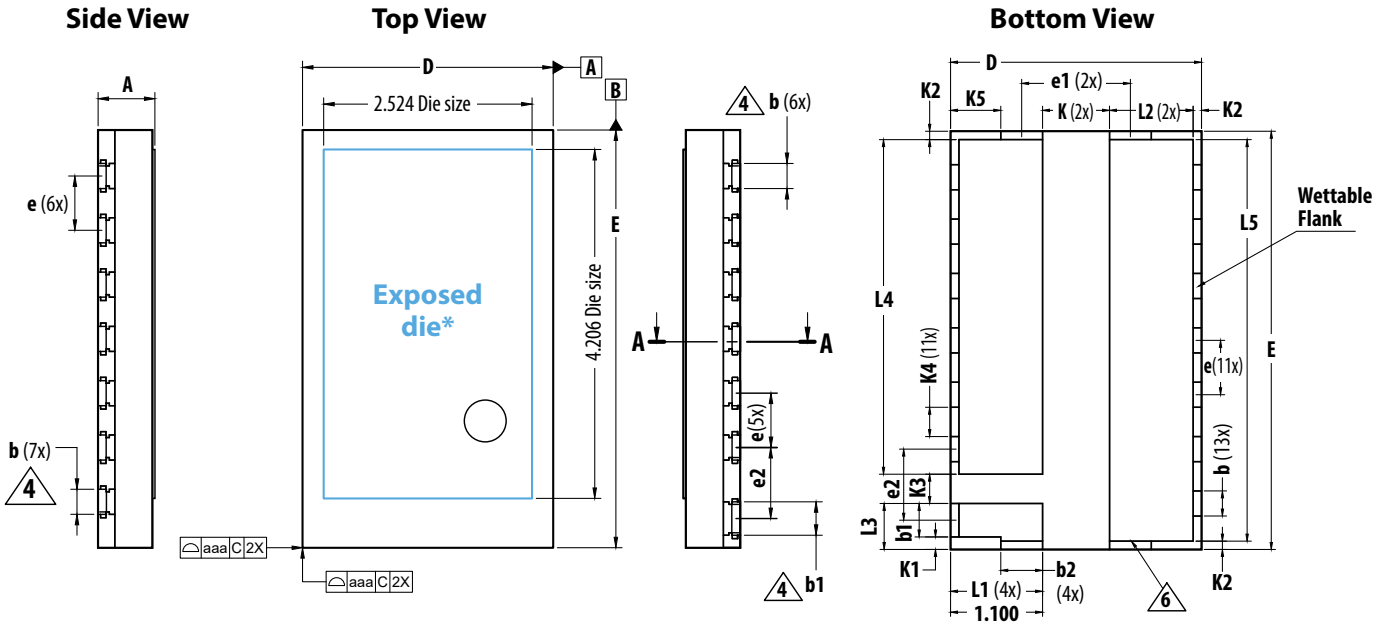
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2375	2375	YYYY	ZZZZA

PACKAGE OUTLINE AND DIMENSIONS









*The exposed die is the silicon substrate that is internally connected to the source.
It is not recommended to use it as an electrical connection

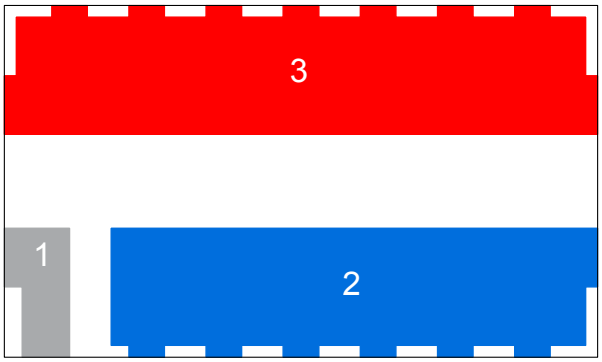
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3			0.25	
b	0.25	0.30	0.35	4
b1	0.35	0.40	0.45	4
b2	0.45	0.50	0.55	4
D	2.90	3.00	3.10	
E	4.90	5.00	5.10	
e		0.65		BSC
e1		1.30		BSC
e2		0.85		BSC
L1	1.00	1.10	1.20	
L2	0.90	1.00	1.10	
L3	0.45	0.55	0.65	
L4	3.90	4.00	4.10	
L5	4.70	4.80	4.90	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K		0.80		REF
K1		0.15		REF
K2		0.10		REF
K3		0.35		REF
K4		0.35		REF
K5		0.60		REF
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		3		3

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.
6. Lead plating is NiPdAu (1.5/0.01/0.005 µm min). Au as the finish.

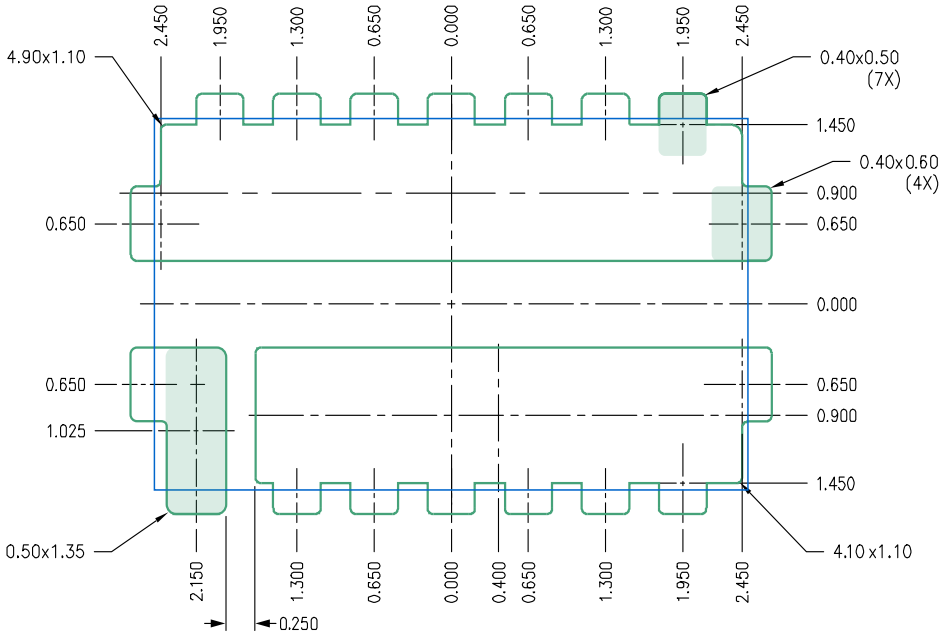
TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Legend:

Part Outline

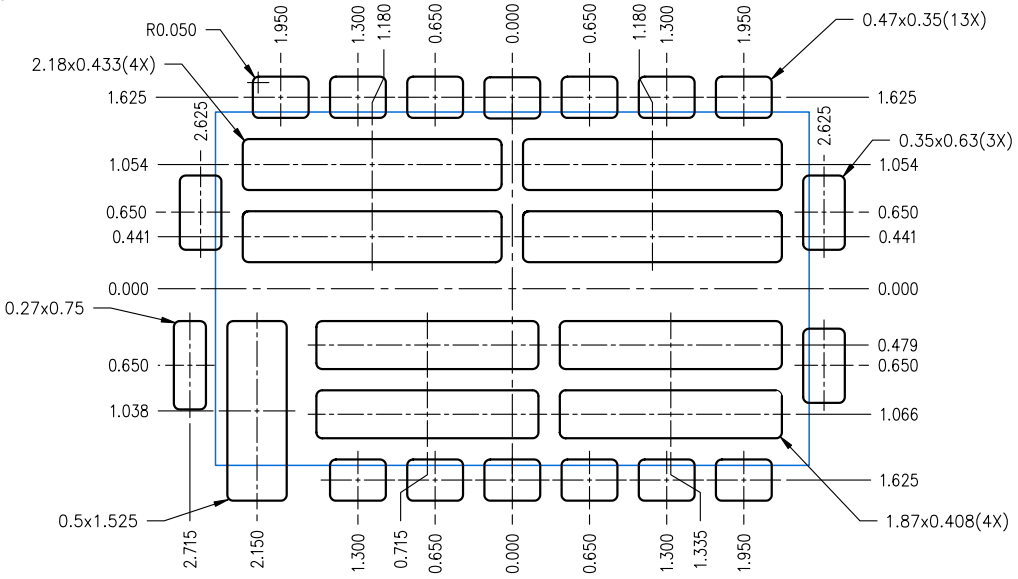
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



Legend:

Part Outline

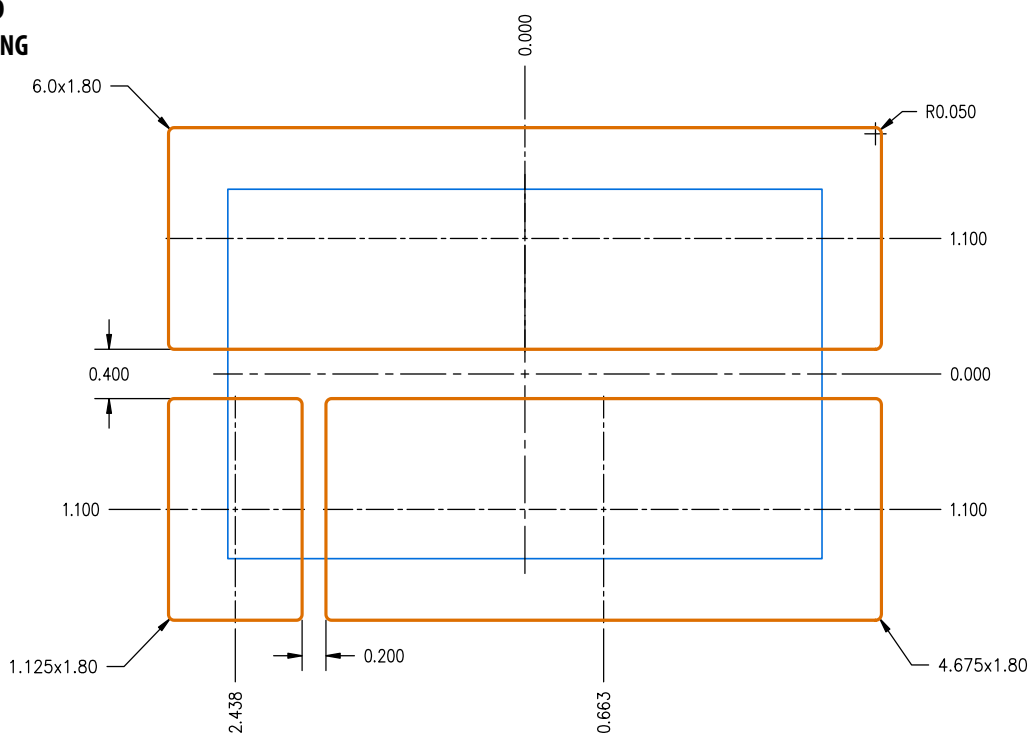
Stencil Opening

The recommended stencil should be 4mils (100 µm) thick, must be laser cut, and have openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.

RECOMMENDED COPPER DRAWING

(units in mm)



ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

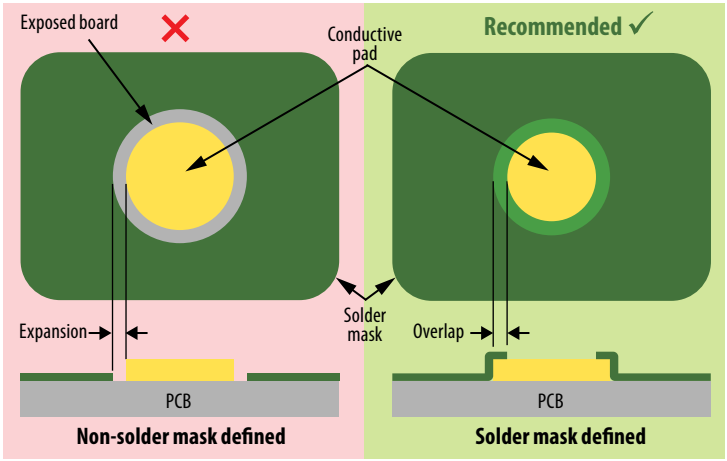


Figure 15: Solder mask defined versus non-solder mask defined pad

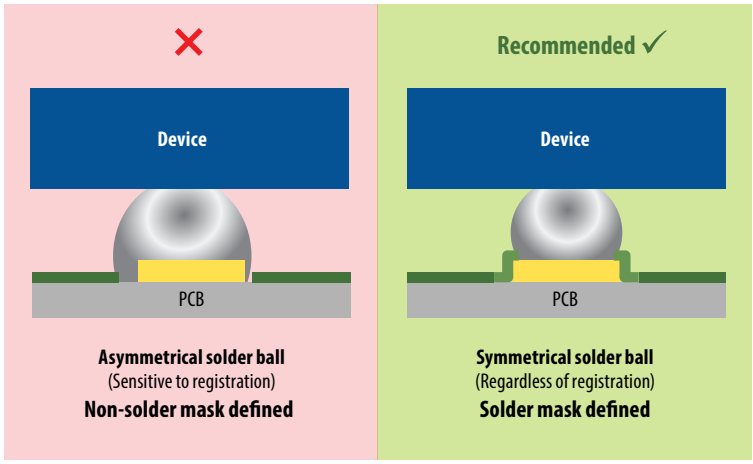


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)

Prior to final qualification and production release, engineering samples might not meet all datasheet specifications.

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