

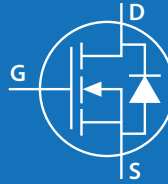
EPC2377 – Enhancement Mode Power Transistor

 V_{DS} , 40 V

 I_D , 101 A

 $R_{DS(on)}$, 0.5 mΩ typ

PRELIMINARY



RoHS

Halogen-Free

July 29, 2026

General Description

EPC's eGaN® power switching HEMTs have been specifically designed for critical applications in dc-dc conversion. These devices have exceptionally high electron mobility and a low temperature coefficient resulting in very low $R_{DS(on)}$ values. The lateral structure of the die provides for very low gate charge (Q_G) and extremely fast switching times. These features enable faster power supply switching frequencies resulting in higher power densities, higher efficiencies and more compact packaging. EPC2377 has been specifically designed for synchronous rectifier applications on the secondary side of a 48 V-12 V LLC converter, where it brings an industry leading low $R_{on} \times Q_g$ figure of merit and enables higher frequency and higher efficiency operation.

Application Notes:

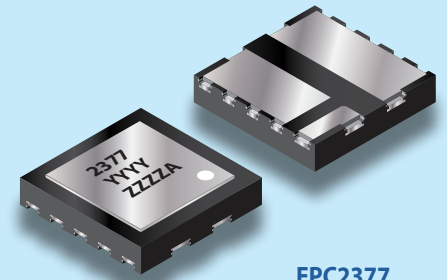
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:
Ask a
GaN Expert



Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous ($T_J \leq 125^\circ\text{C}$)	101	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	553	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.6	
$R_{\theta JA_JEDEC}$	Thermal resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	56	



EPC2377

Package size: 3.3 x 3.3 mm

Features

- Ultra-low Q_G for high frequency
- PQFN package with backside thermal pad
- No reverse recovery

Applications

- High performance, high power-density DC-DC conversion
- High-frequency DC-DC converters
- Synchronous rectifiers

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2377>

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = \text{TBD}$	40			V
I_{DSS}	Drain-to-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$		0.2		mA
		$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}, T_J = 125^\circ\text{C}$		0.9		
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		85		μA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$				
	Gate-to-Source Reverse Leakage	$V_{GS} = -2\text{ V}$		300		
$V_{GS(TH)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 20\text{ mA}$	0.8	1.2	2.5	V
$R_{DS(on)}$	Drain-to-Source Resistance	$V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		0.5	0.7	$\text{m}\Omega$
V_{SD}	Source-to-Drain Forward Voltage [#]	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$		1.7		V

[#] Defined by design. Not subject to production test.

All measurements were done with substrate shorted to source.

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$		4520		pF
C_{RSS}	Reverse Transfer Capacitance			30		
C_{OSS}	Output Capacitance			991		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }20\text{ V}$		1196		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related			1487		
Q_G	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		26		nC
$Q_{G\text{ Sync}}$	Total Gate Charge Synchronous	$V_{GS} = 5\text{ V}, V_{DS} = 0\text{ V}, I_D = 0\text{ A}$		24		
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 20\text{ V}, I_D = 20\text{ A}$		12		
Q_{GD}	Gate-to-Drain Charge			3.6		
$Q_{G(TH)}$	Gate Charge at Threshold			8.6		
Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$		38		
Q_{RR}	Source-Drain Recovery Charge			0		

[#] Defined by design. Not subject to production test.

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

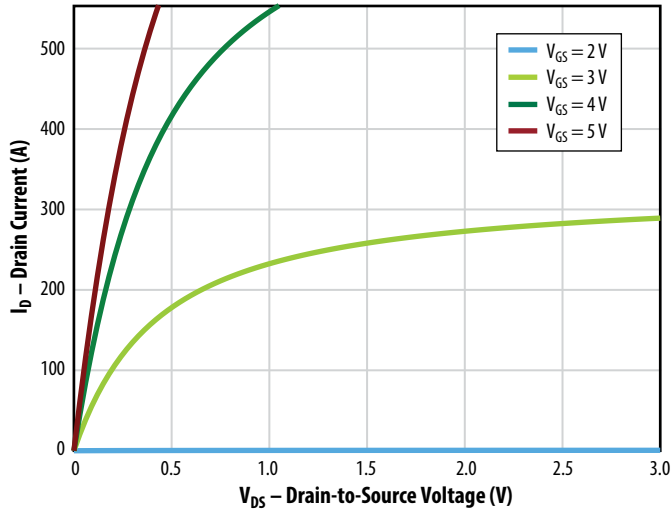


Figure 2: Typical Transfer Characteristics

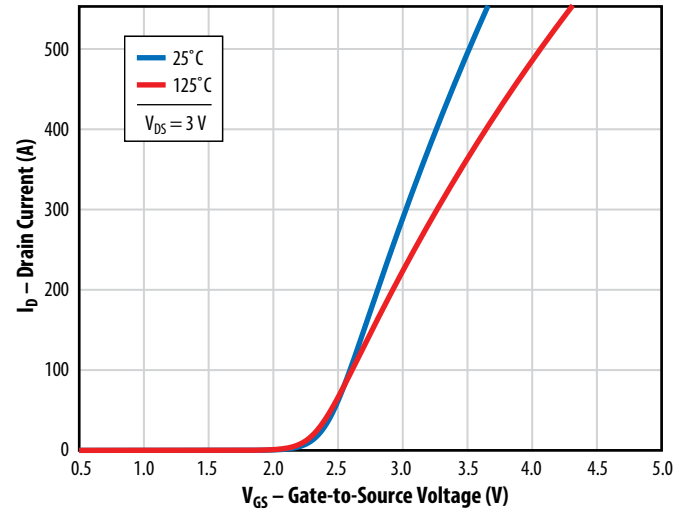
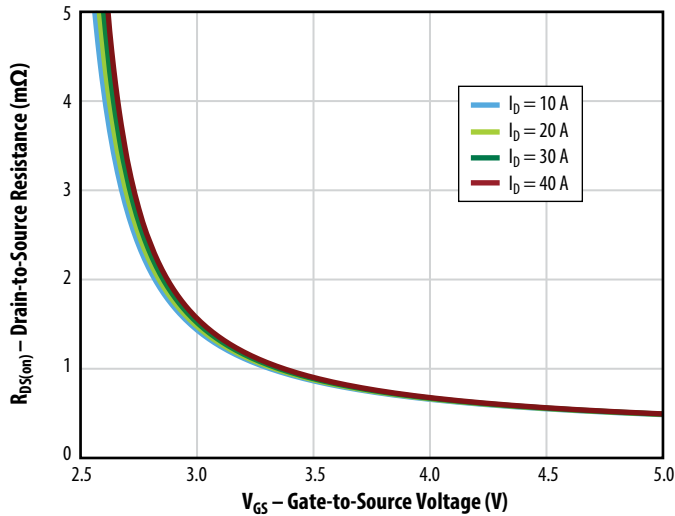
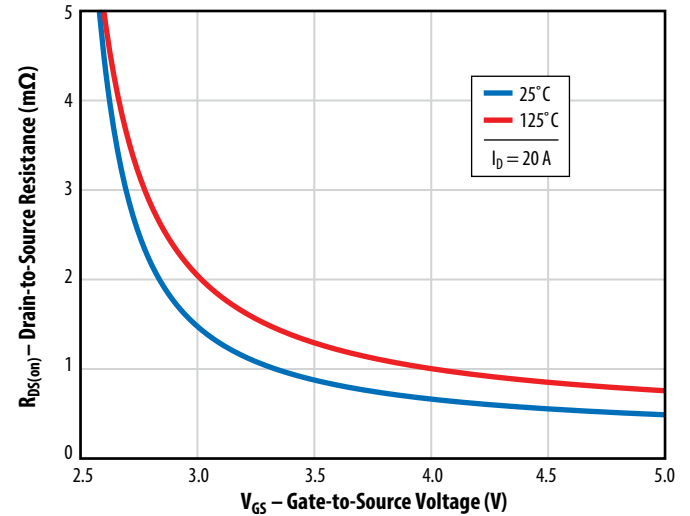
Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

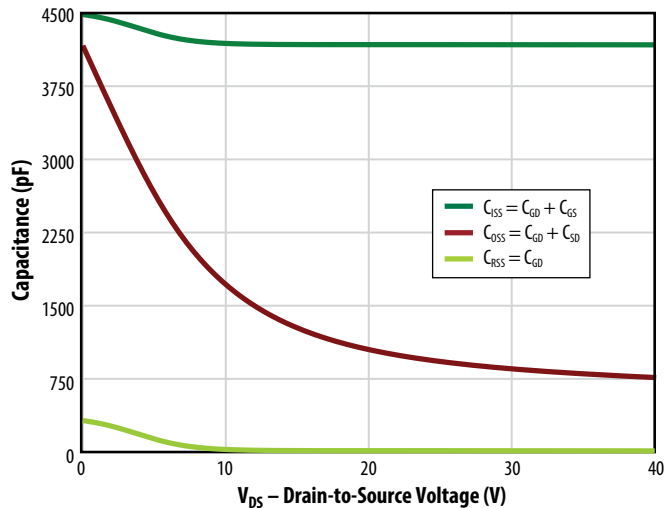


Figure 5b: Typical Capacitance (Log Scale)

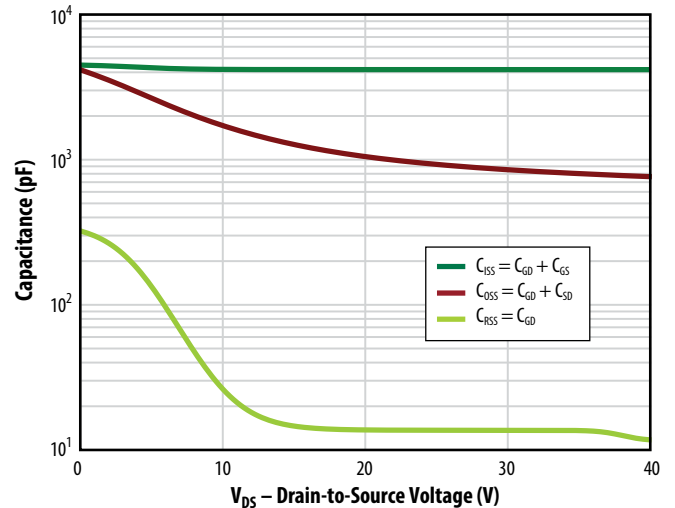


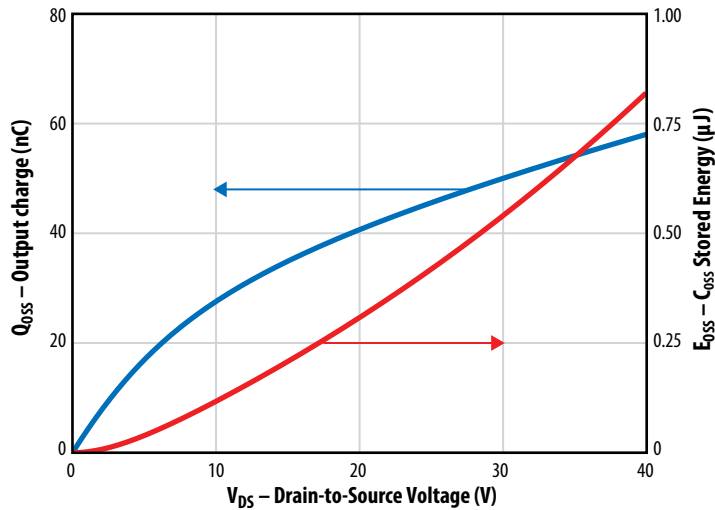
Figure 6: Typical Output Charge and C_{OSS} Stored Energy

Figure 7: Typical Gate Charge

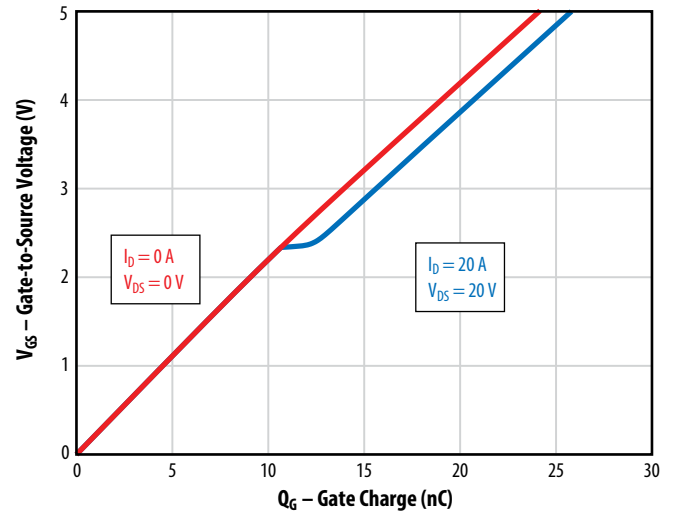
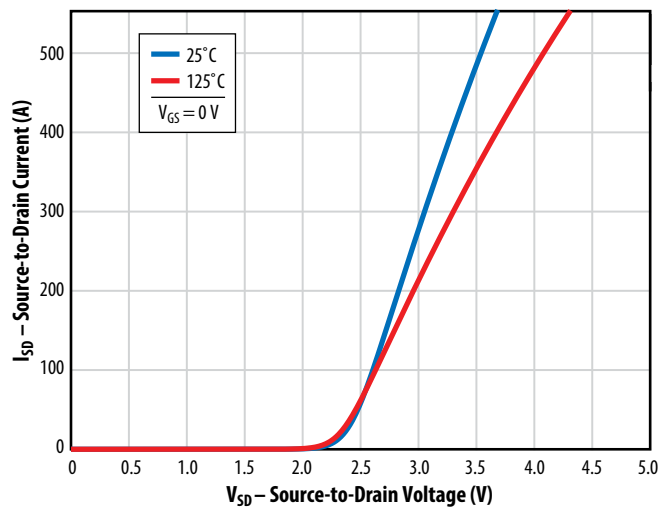


Figure 8: Typical Reverse Drain-Source Characteristics



Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0V for OFF

Figure 9: Typical Normalized On-State Resistance vs. Temp.

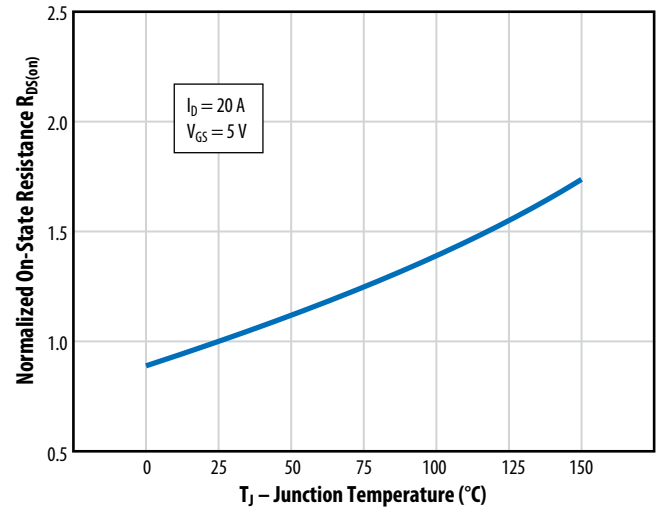


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

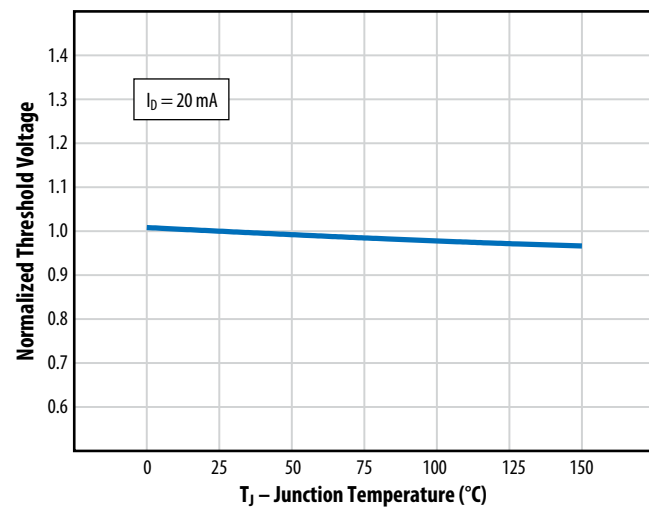


Figure 11: Safe Operating Area

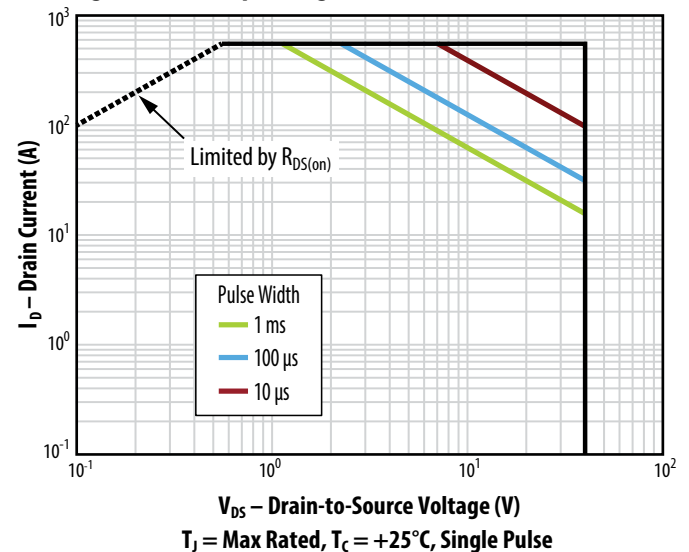
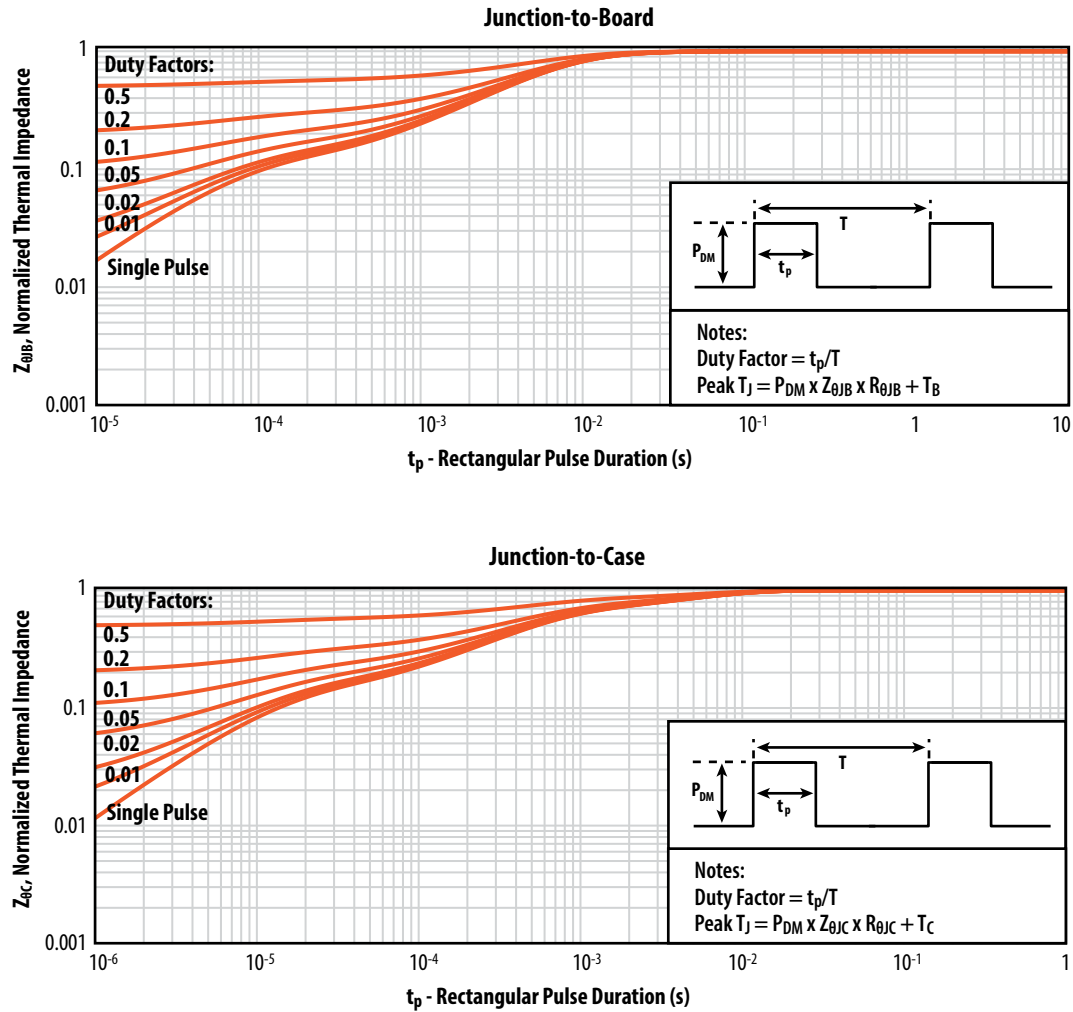


Figure 12: Typical Transient Thermal Response Curves



TYPICAL THERMAL CONCEPT

The EPC2377 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs.

Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

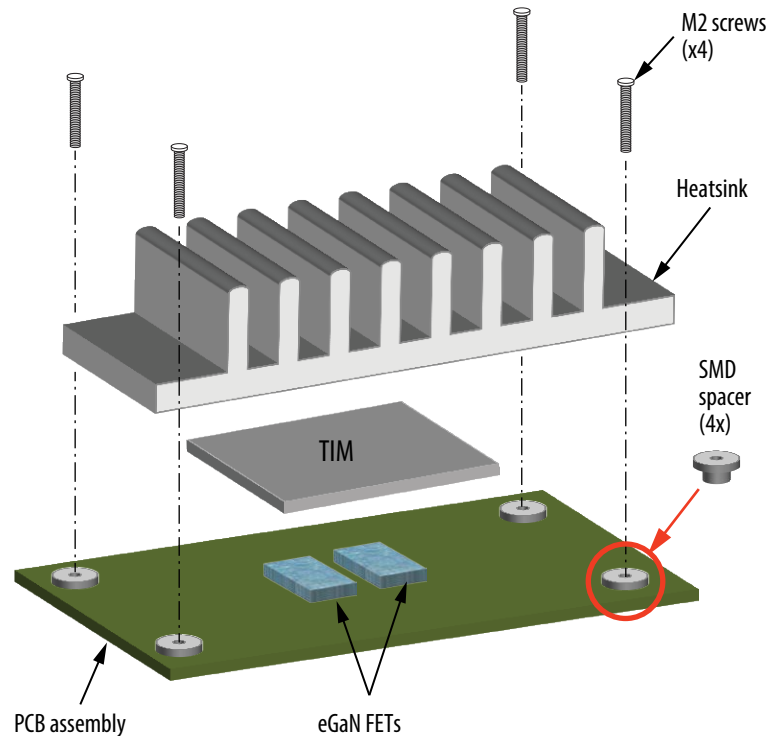


Figure 13: Exploded view of heatsink assembly using screws

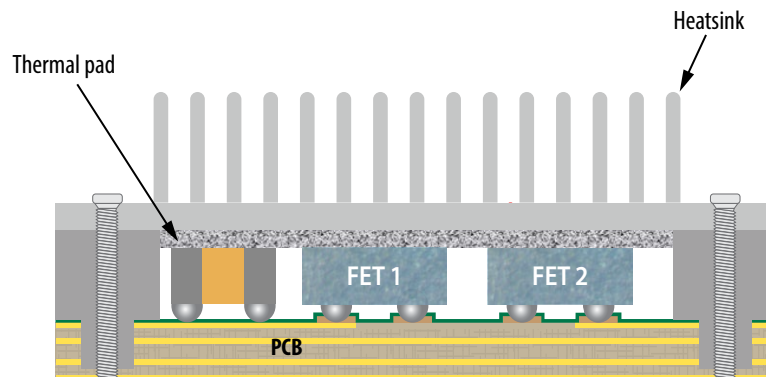


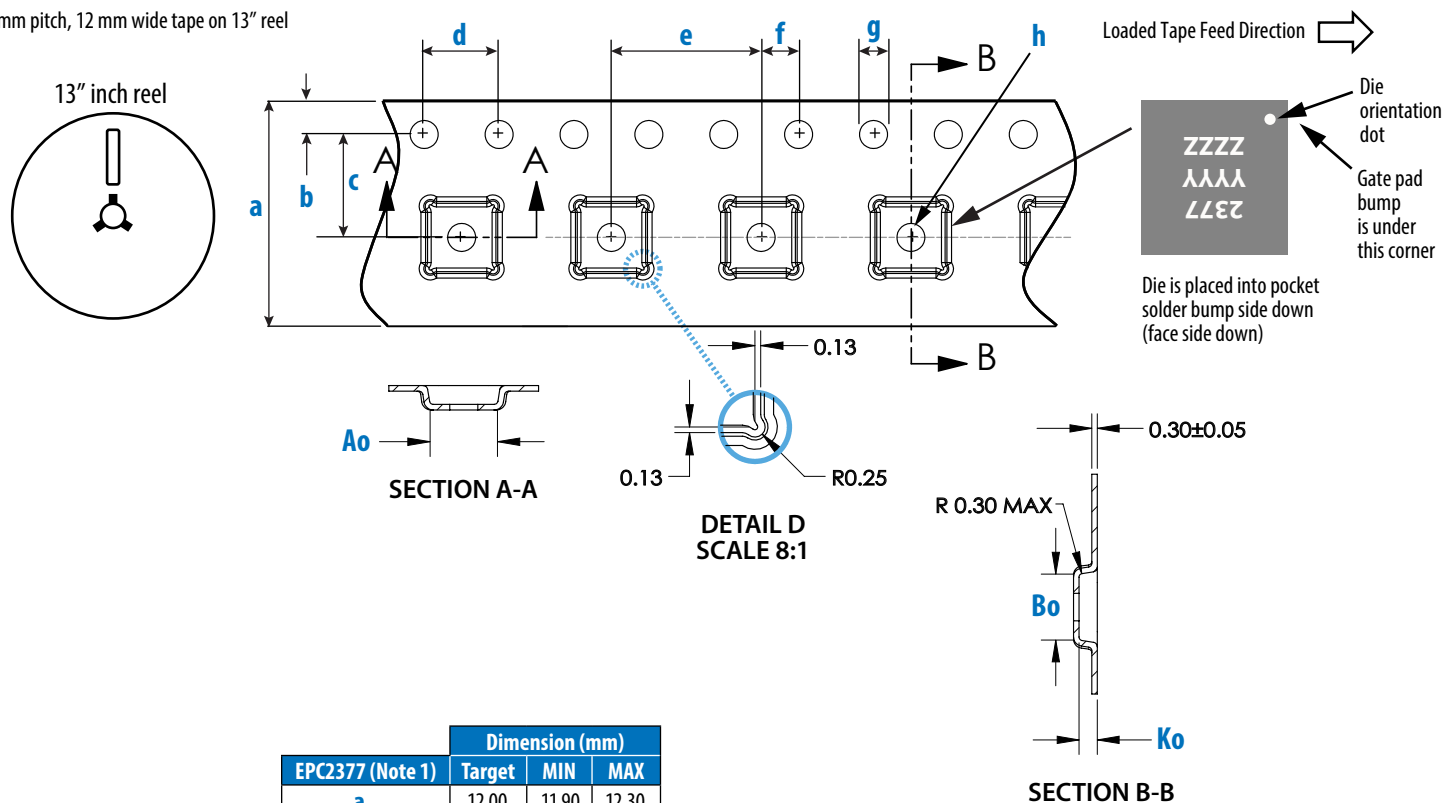
Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

TAPE AND REEL CONFIGURATION

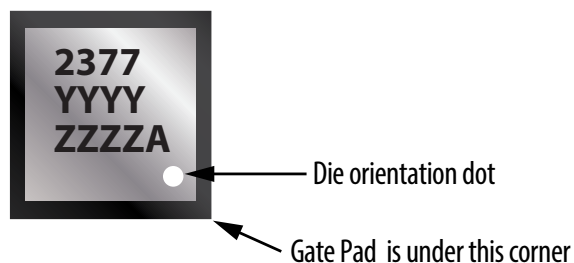
8 mm pitch, 12 mm wide tape on 13" reel



Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

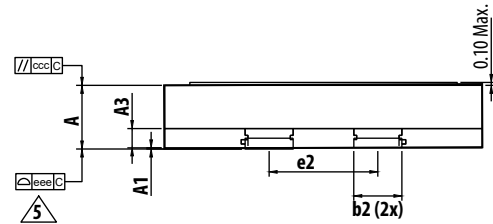
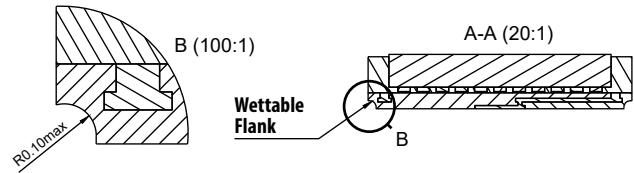
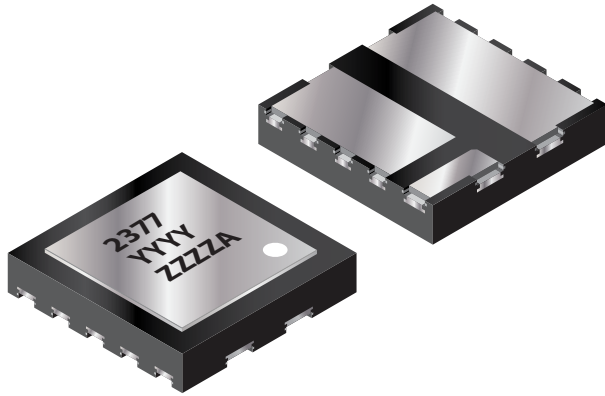
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

Part Marking



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2377	2377	YYYY	ZZZZA

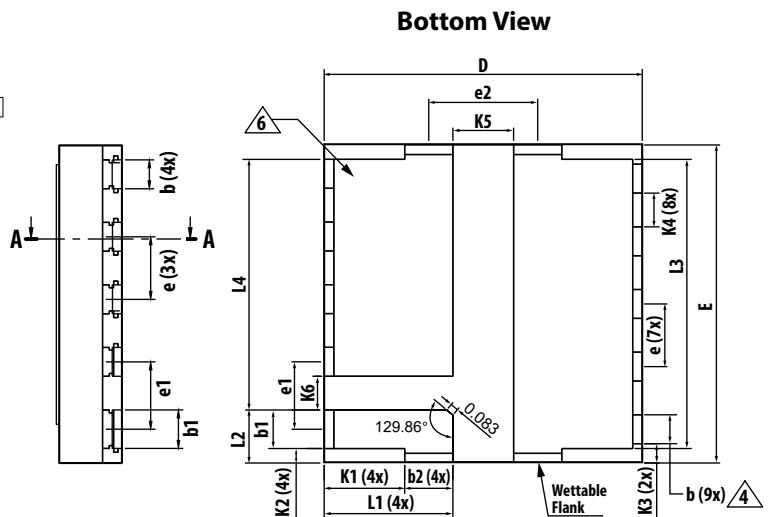
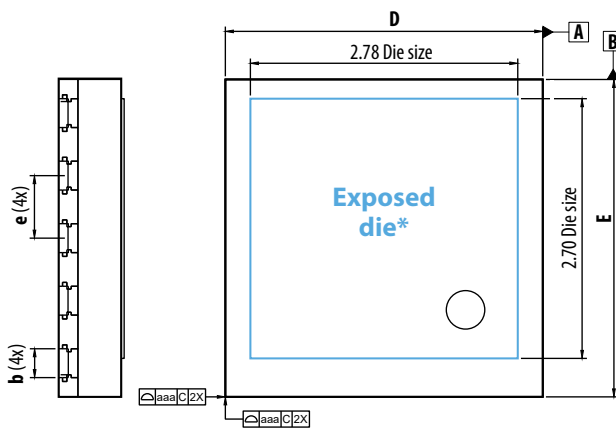
PACKAGE OUTLINE AND DIMENSIONS



Front View

Side View

Top View



Bottom View

*The exposed die is the silicon substrate that is internally connected to the source.
It is not recommended to use it as an electrical connection

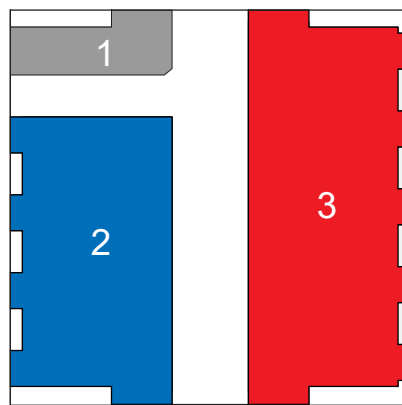
SYMBOL	Dimension (mm)				Note
	MIN	Nominal	MAX		
A	0.60	0.65	0.70		
A1	0.00	0.02	0.05		
A3			0.25		
b	0.25	0.30	0.35	4	
b1	0.35	0.40	0.45	4	
b2	0.45	0.50	0.55	4	
D	3.20	3.30	3.40		
E	3.20	3.30	3.40		
e		0.65			BSC
e1		0.70			BSC
e2		1.13			BSC
L1	1.235	1.335	1.435		
L2	0.45	0.55	0.65		
L3	2.90	3.00	3.10		
L4	2.15	2.25	2.35		

SYMBOL	Dimension (mm)				Note
	MIN	Nominal	MAX		
K1		0.835			REF
K2		0.15			REF
K3		0.20			REF
K4		0.35			REF
K5		0.63			REF
K6		0.35			REF
aaa		0.05			
bbb		0.10			
ccc		0.10			
eee		0.08			
N		3			3

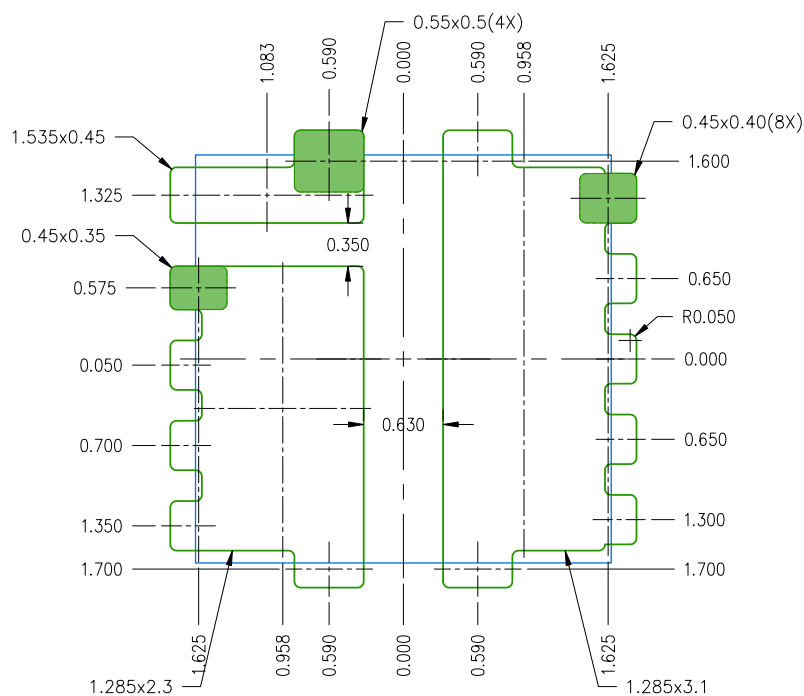
Notes:

- Dimensioning and tolerancing conform to ASME Y14.5-2009
- All dimensions are in millimeters
- N is the total number of terminals
- △4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
- △5. Coplanarity applies to the terminals and all the other bottom surface metallization.
- △6. Lead plating is NiPdAu (1.5/0.01/0.005 μm min). Au as the finish.

TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain

**RECOMMENDED
LAND PATTERN**
(units in mm)


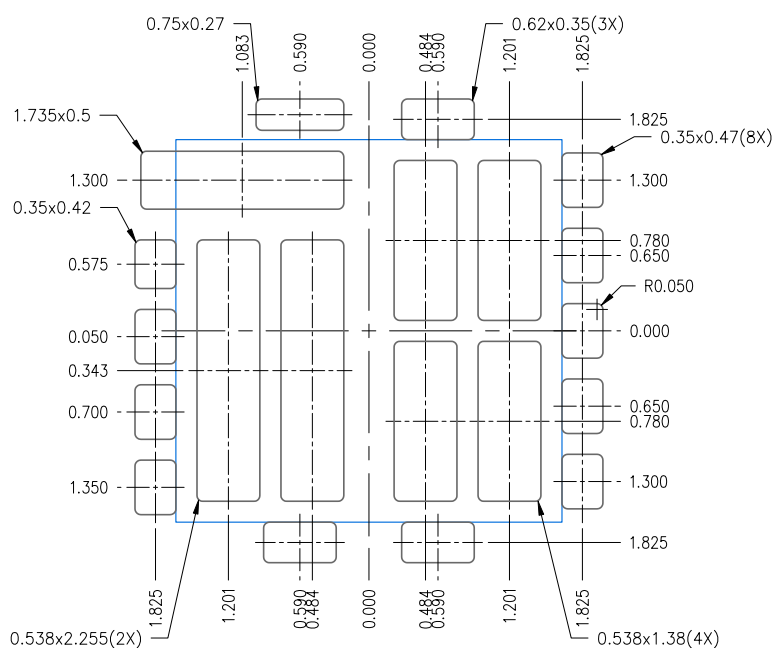
Legend:

Part Outline

Mask Opening

Radius = 0.05

Land pattern is solder mask defined

**RECOMMENDED
STENCIL DRAWING**
(units in mm)


Legend:

Part Outline

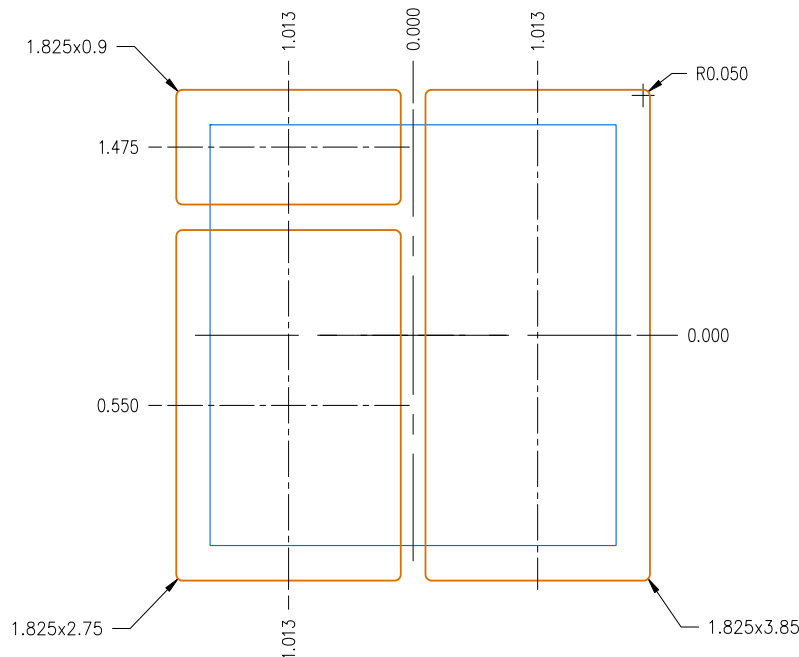
Stencil Opening

The recommended stencil should be 4mils (100 μ m) thick, must be laser cut, and have openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metal content.

RECOMMENDED COPPER DRAWING

(units in mm)



Legend:

Part Outline

Copper

Radius = 0.05

ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

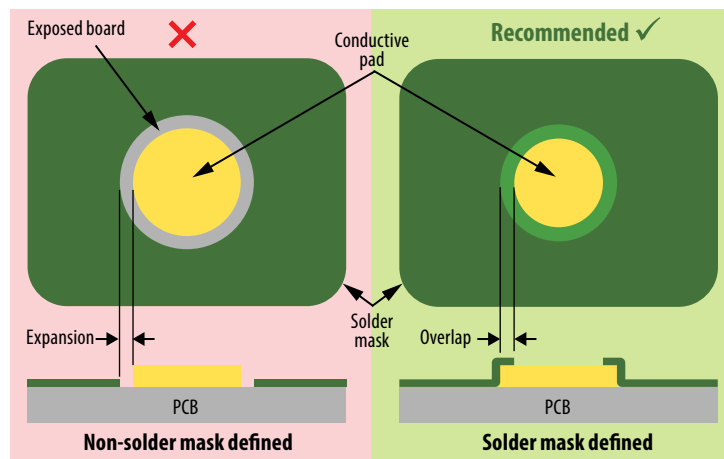


Figure 15: Solder mask defined versus non-solder mask defined pad

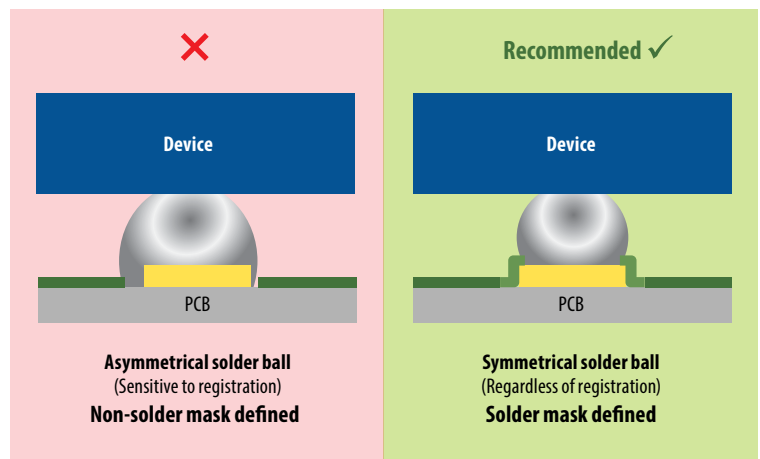


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

Prior to final qualification and production release, engineering samples might not meet all datasheet specifications.

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EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

Information subject to change without notice.

Change Log

STATUS	VERSION	DATE	REMARK
2.0	Preliminary	29 July 2026	Preliminary release