Evaluation Board EPC90175 Quick Start Guide

25 V Half-bridge with Gate Drive using EPC2371

May 1, 2026

Revision 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC90175 is a half bridge evaluation board for the 25 V-rated EPC2371 eGaN® field effect transistor (FET). The purpose of this evaluation board is to simplify the evaluation process of EPC2371 by including all the critical components on a single board that can be easily integrated into most existing converter topologies.

The EPC90175 evaluation board measures 2.5" x 2" and contains two EPC2371 eGaN FETs in a half-bridge configuration paired with the Analog Devices LT8418 half-bridge gate driver. The board also contains all other critical components such as a deadtime generation circuit and input bus capacitors. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on EPC2371 please refer to their datasheets available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (T_A = 25°C) EPC90175

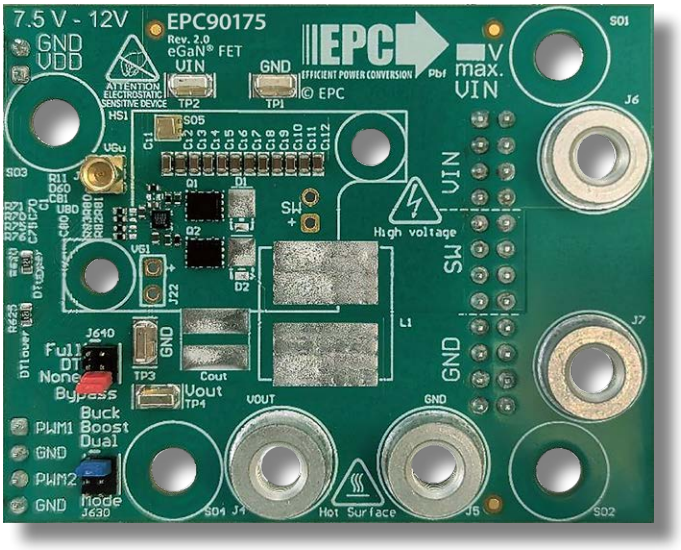
Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{DD}	Gate Drive Regulator Supply Range		7.5	8.5	12	V
V_{IN}	Bus Input Voltage Range(1)				20 (1)	
I_{OUT}	Switch Node Output Current (2)				65(2)	A
V_{PWM}	PWM Logic Input Voltage Threshold (3)	Input 'High'	3.5 (3)		5.5 (3)	V
		Input 'Low'	0		1.5 (3)	
	PWM 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10 ns	50			ns
	PWM 'Low' State Input Pulse Width (4)	V_{PWM} rise and fall time < 10 ns	200 (4)			

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 25 V for EPC2371.

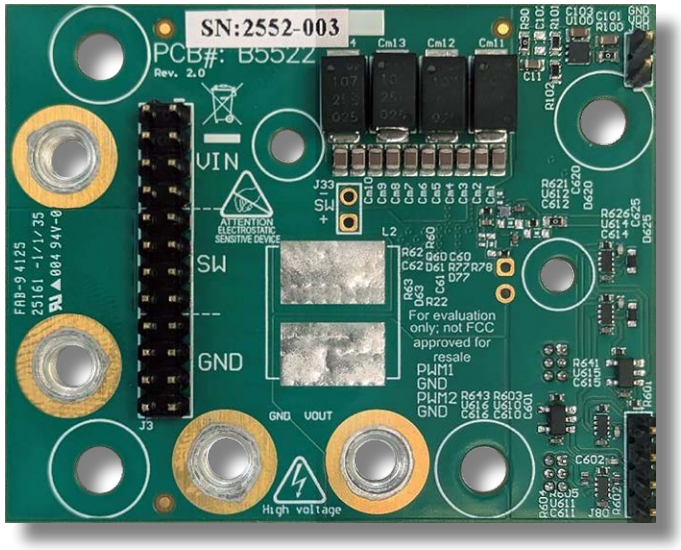
(2) Maximum current depends on die temperature and input bus capacitor temperature – actual maximum current is affected by switching frequency, bus voltage, inductor current ripple and thermal cooling.

(3) Refer to the LT8418 datasheet when bypassing the on-board logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view



Back view

EPC90175 evaluation board

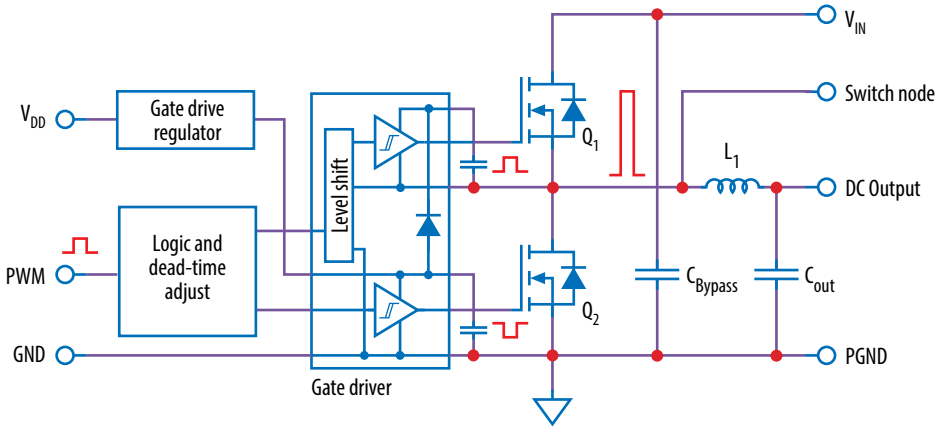


Figure 1: Block diagram of EPC90175 evaluation board default configuration

QUICK START PROCEDURE

The EPC90175 evaluation board is easy to set up as a buck or boost converter to evaluate the performance of the two EPC2371 eGaN FETs. This board includes a dead-time generating circuit that adds a delay from when the gate signal of one FET is commanded to turn off, to when the gate signal of the other FET is commanded to turn on. In the default configuration, this dead time circuit ensures that both the high and low side FETs will not be turned on at the same time thus preventing a shoot-through condition. The dead-time and/or polarity changing circuits can be utilized or bypassed for added versatility.

Single/dual PWM signal input settings

There are two PWM signal input ports on the board, PWM1 and PWM2. Both input ports are used as inputs in dual-input mode where PWM1 connects to the upper FET and PWM2 connects to the lower FET. The PWM1 input port is used as the input in single-input mode where the circuit will generate the required complementary PWM for the FETs. The input mode is set by choosing the appropriate jumper positions for J630 (mode selection) as shown in figure 2(a) for a single-input buck converter (**blue** jumper across pins 1 & 2 of J630), (b) for a single-input boost converter (**blue** jumpers across pins 3 & 4 of J630), and (c) for a dual-input operation (**blue** jumpers across pins 5 & 6 of J630).

Note: In dual mode there is no shoot-through protection as both gate signals can be set high at the same time.

Dead-time settings

Dead-time is defined as the time between when one FET turns off and the other FET turns on, and for this board is referenced to the input of the gate driver. The dead-time can be set to a specific value where resistor R620 delays the turn on of the upper FET and resistor R625 delays the turn on of the lower FET as illustrated in figure 3.

The required resistance for the desired dead-time setting can be read off the graph in figure 4. An example for 10 ns dead-time setting shows that a 120 Ω resistor is needed.

Note: This is the default deadtime and resistor value installed. A minimum dead-time of 5 ns and maximum of 15 ns is recommended.

Bypass settings

Both the polarity changer and the deadtime circuits can be bypassed using the jumper settings on J640 (Bypass), for direct access to the gate driver input. There are three bypass options: 1) No bypass, 2) Dead-time bypass, 3) Full bypass. The jumper positions for J640 for all three bypass options are shown in figure 5.

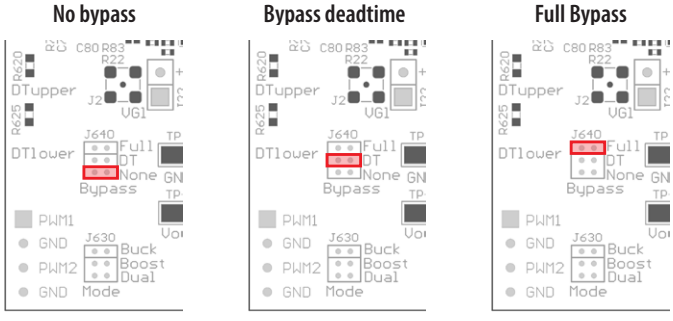


Figure 5: Bypass mode Jumper settings for J640

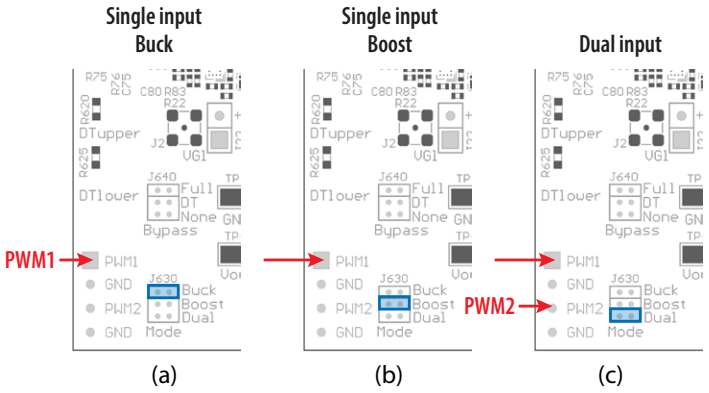


Figure 2: Input mode selection on J630

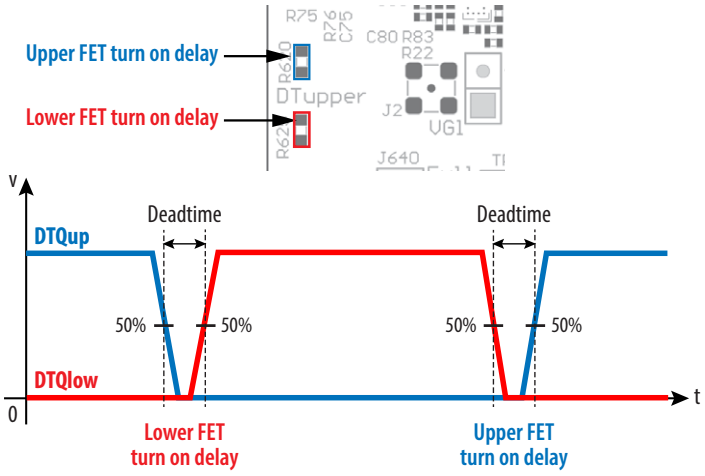


Figure 3: Definition of dead-time between the upper-FET gate signal (DTQup) and the lower-FET gate signal (DTQlow)

Figure 4: The required resistance values for R620 or R625 as a function of desired dead-time

In ***no-bypass mode***, figure 5(a) (**red** jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In ***dead-time bypass mode***, figure 5(b) (**red** jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In ***full bypass mode***, Figure 5(c) (**red** jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Bypass mode warnings

- ***In bypass mode the PWM signals must include the deadtimes and desired polarity for either buck or boost operation.***
- When operating in ***full bypass mode***, the input signal specifications revert to that of the LT8418 gate driver IC. Refer to its datasheet for details.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Buck Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the ***buck mode*** J630 ***must*** be selected as shown in figure 6(a).

To select ***Dual Input Buck Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the dual-input mode J630 ***must*** be selected as shown in figure 6(b).

Note: In bypass mode the PWM signals must include the deadtimes and desired polarity for either buck or boost operation.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

EPC recommends following theses steps:

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 6.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

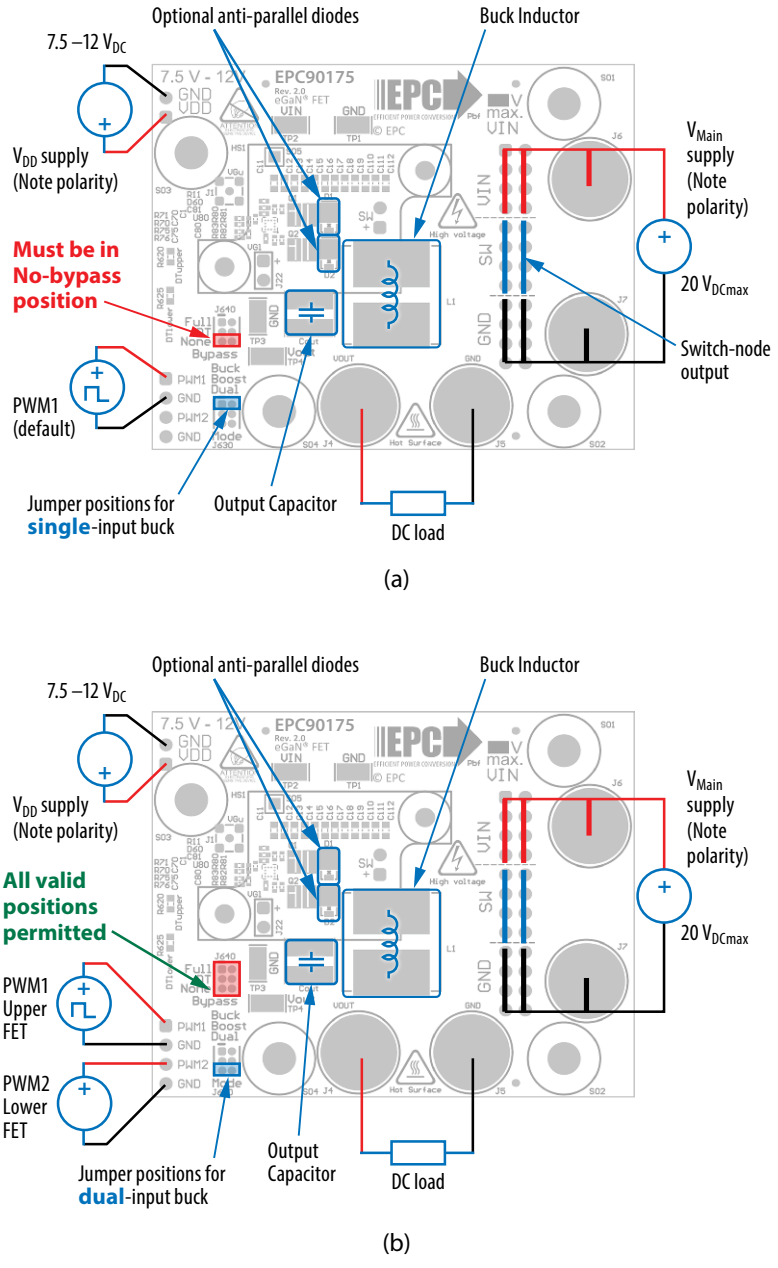


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select ***Single Input Boost Mode***, the bypass jumper J640 ***must*** be set to the ***no-bypass mode***, the boost mode J630 ***must*** be selected as shown in figure.7(a).

To select ***Dual Input Boost Mode***, the bypass jumper J640 ***may*** be configured to any of the valid settings, the ***dual-input mode*** J630 ***must*** be selected as shown in figure 7(b).

Note: In bypass mode the PWM signals must include the deadtimes and desired polarity for either buck or boost operation.

Once the input source, dead-time settings and bypass configurations have be chosen and set, then the boards can be operated.

EPC recommends following theses steps:

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC2371 FETs.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (**labeled as VIN**) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to V_{DD} (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to chosen input mode setting and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. **Making sure the output is not open circuit**, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (***do not exceed the absolute maximum voltage***). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

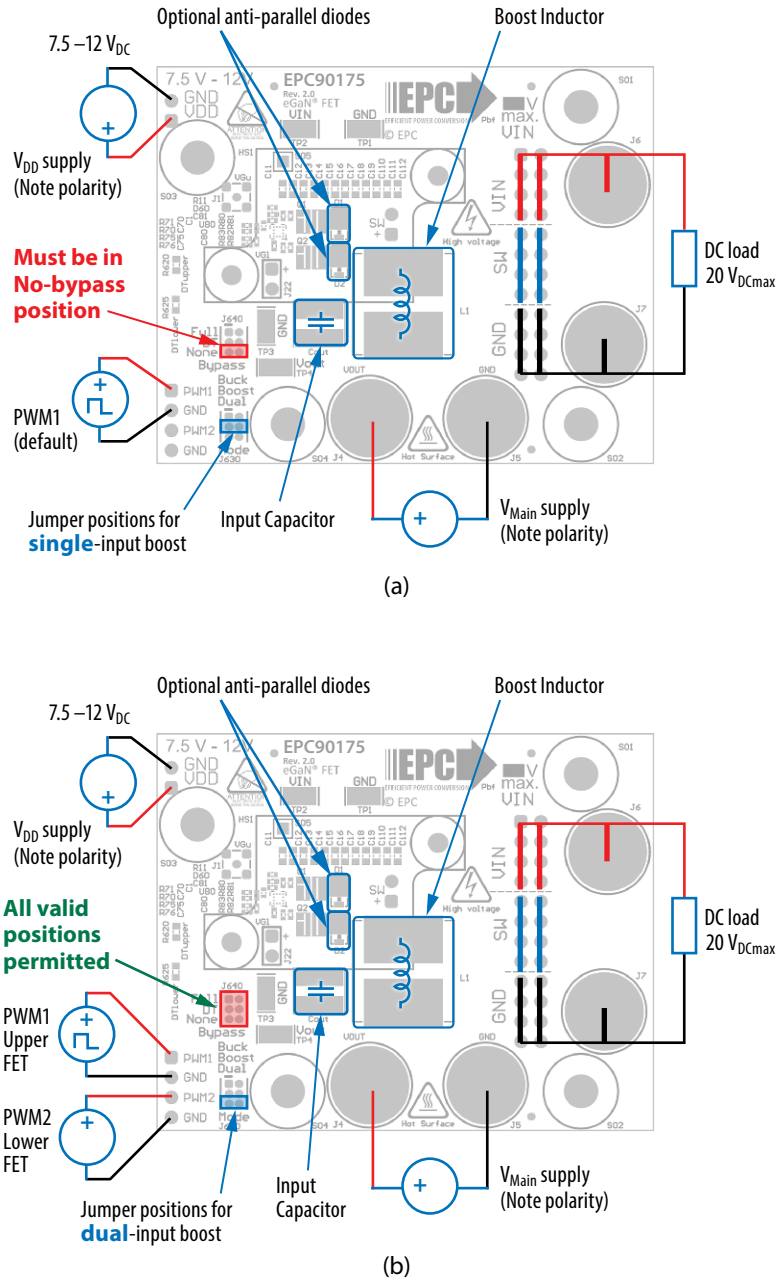


Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

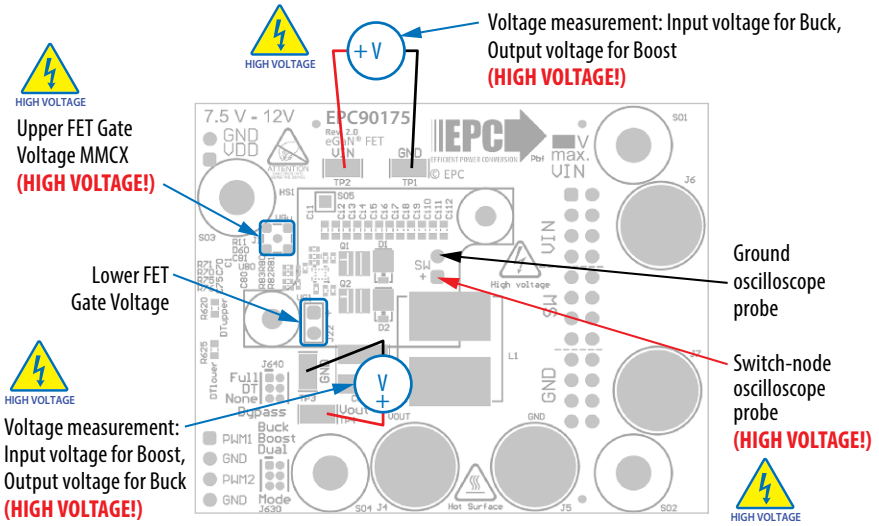
MEASUREMENT CONSIDERATIONS

Measurement connections are shown in figure 8.

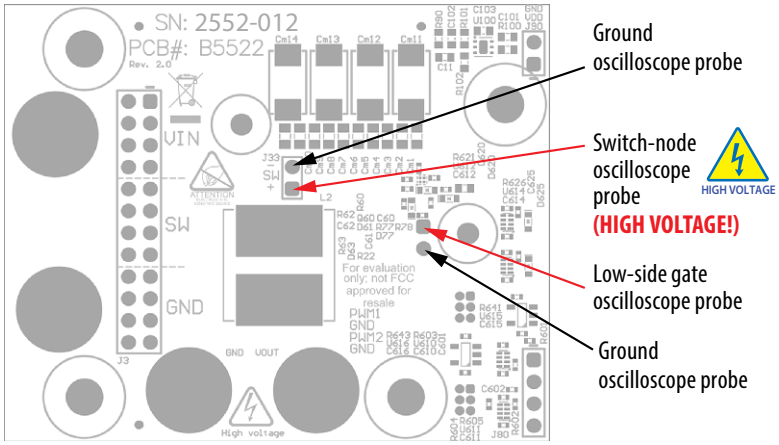
When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. A two-pin header (J33) is provided for switch-node measurement.

A differential probe is recommended for measuring the high-side gate voltage. IsoVu probes from Tektronix have mating MMCX connector.

NOTE. For information about measurement techniques, the EPC website offers: "**AN023 Accurately Measuring High Speed GaN Transistors**" and the How to GaN educational video series, including: **HTG09- Measurement**



(a)



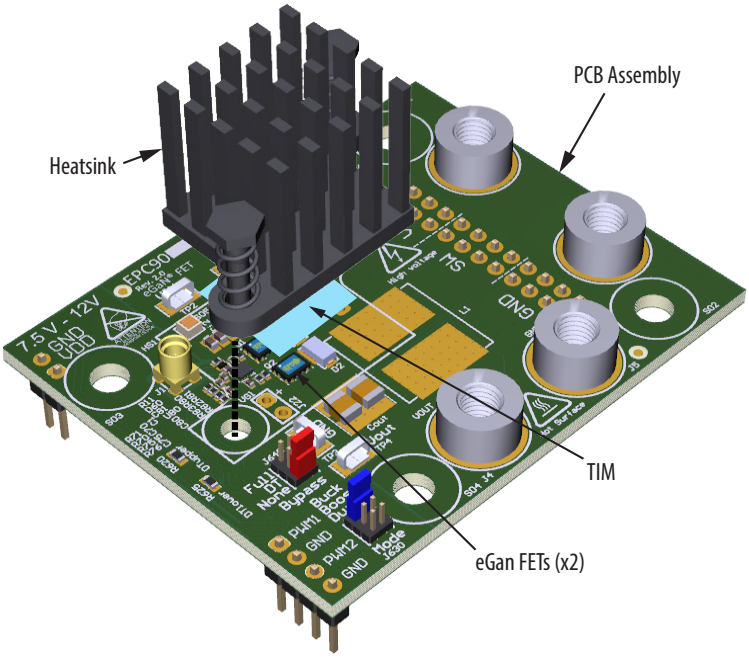
(b)

Figure 8: Measurement points (a) top side, (b) bottom side

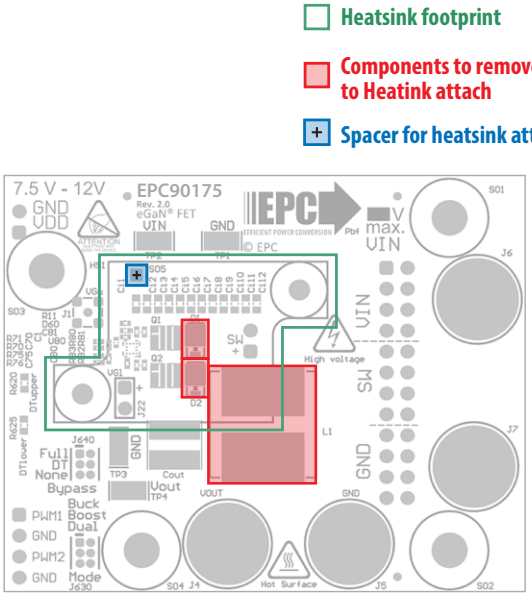
THERMAL CONSIDERATIONS

The EPC90175 board is equipped with a mechanical spacer and 2 heatsink mechanical mounting holes that can be used to easily attach an off-the-shelf heatsink (P/N: 960-19-21-S-AB-0) as shown in figure 9 (a). The setup only requires a thermal interface material (TIM). Prior to attaching a heatsink, any component exceeding 1 mm in thickness under the heatsink area must be removed from the board as shown in figure 9 (b). Note that the board includes pads for the inductor on top and bottom sides, so if the heatsink is installed, the inductor can be moved to the bottom side of the board.

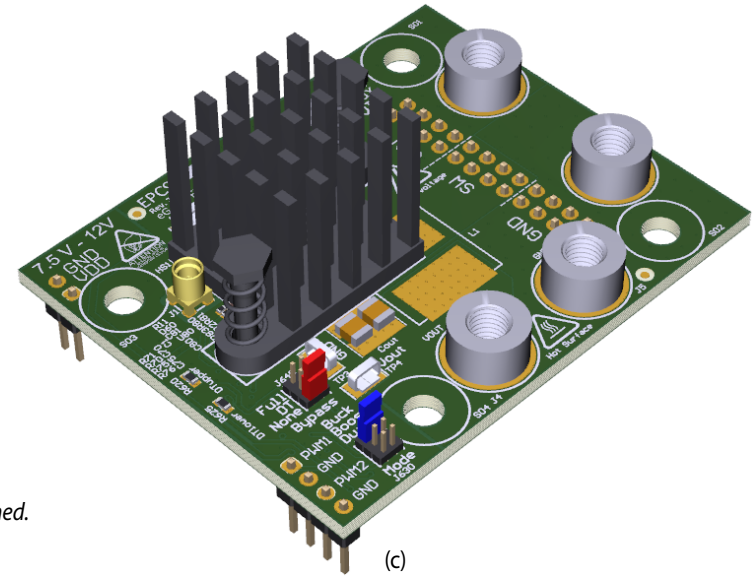
Note that the heatsink is not electrically connected to the board.



(a)



(b)



(c)

Figure 9: Details for attaching a heatsink to the evaluation board.
(a) 3D perspective, (b) top view details, (c) Assembled view with heatsink attached.

EPC recommends using a high thermal conductivity TIM between the board and the heatsink. The size and location of the TIM are shown in Figure 10. Alternatively, a smaller TIM may be used to cover only the area of the FETs. In that case, adding a thin insulator over the capacitors with a cutout around the FETs, as shown in Figure 11, is recommended.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heatsink, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

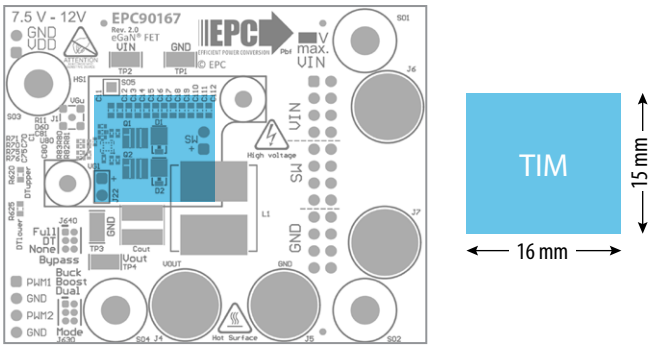


Figure 10: Size and location of the TIM

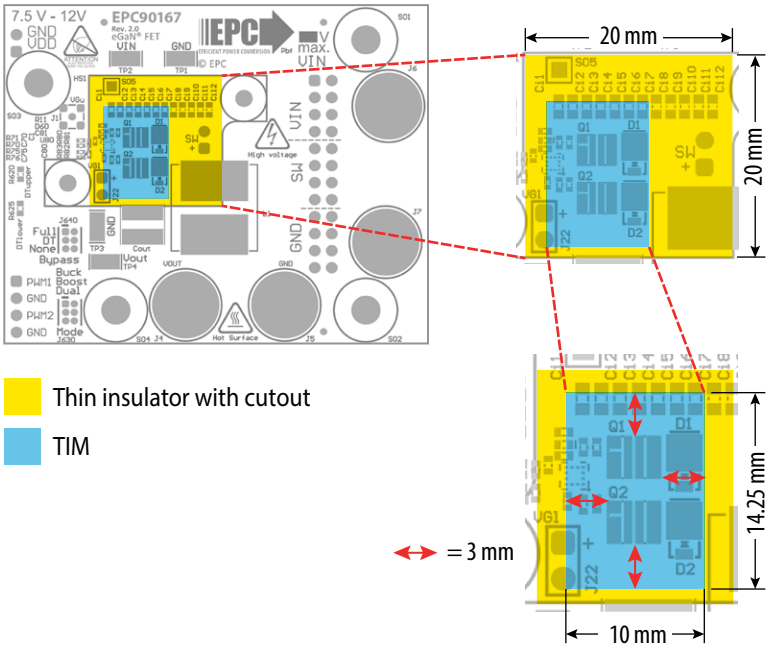


Figure 11: Alternative TIM configuration with insulator sheet with cutout for the TIM

EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m.K)
- **t-Global** P/N: TG-A620 X 0.5 mm (moderate conductivity of 6.2 W/m.K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m.K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m.K)

NOTE. The EPC90175 evaluation board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN FETs, please consult:
D. Reusch and J. Glaser, ***DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion,*** First Edition, Power Conversion Publications, 2015.

EXPERIMENTAL VALIDATION

The performance of EPC90175 configured as a buck converter was tested under various input voltages and switching frequencies. Table 2 lists additional details with the inductor, output capacitance, deadtimes and maximum case temperatures.

A heatsink per figures 9 and 10 (P/N: 960-19-21-S-AB-0) using t-Global TG-A1780 thermal interface material (TIM) was added where specified.

Additional input and output capacitance are added to suppress input and output voltage ripple at high output current as shown in Table 2.

Table 2: Test Conditions for Electrical Performance

Parameter	Value	Units
Output Voltage	1	V
Inductor	0.07	µH (1)
Dead time	5	ns
Gate resistors	0.47	Ω
Output capacitance	110	µF (2)
Ambient temperature	25	°C
Max case temperature	110	°C
Airflow	400	LFM

(1) 0.07 µH inductor from Coilcraft, SLC1175-700MEB

(2) Capacitors used: 22 µF, 25V, x5 (P/N:J GRT21BR61E226ME13L)

ELECTRICAL PERFORMANCE

Measured Waveforms

Figures 12-14 show the measured switchnode voltage.

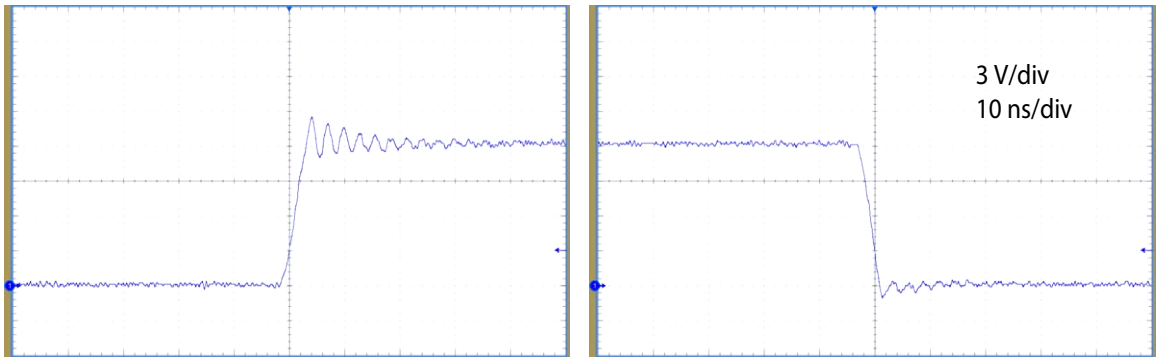


Figure 12: Measured switchnode voltage at 12 V_{IN}, 1 V_{OUT}, 1 MHz, 0 A

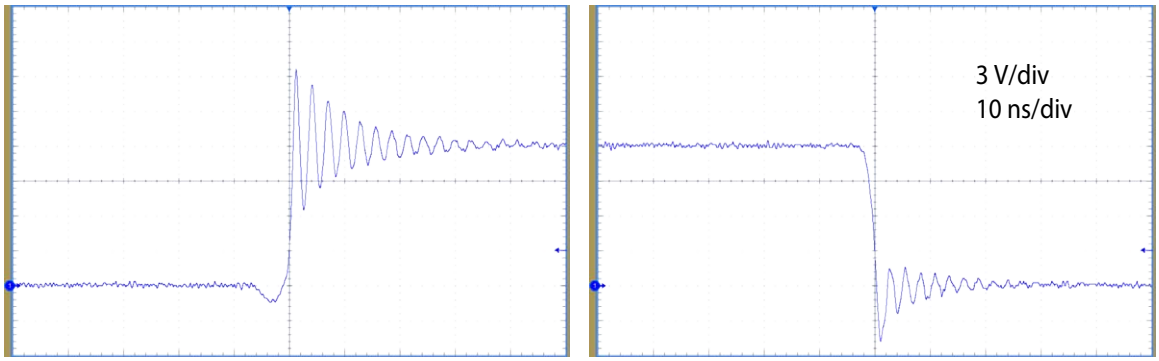


Figure 13: Measured switchnode voltage at 12 V_{IN}, 1 V_{OUT}, 1 MHz, 30 A

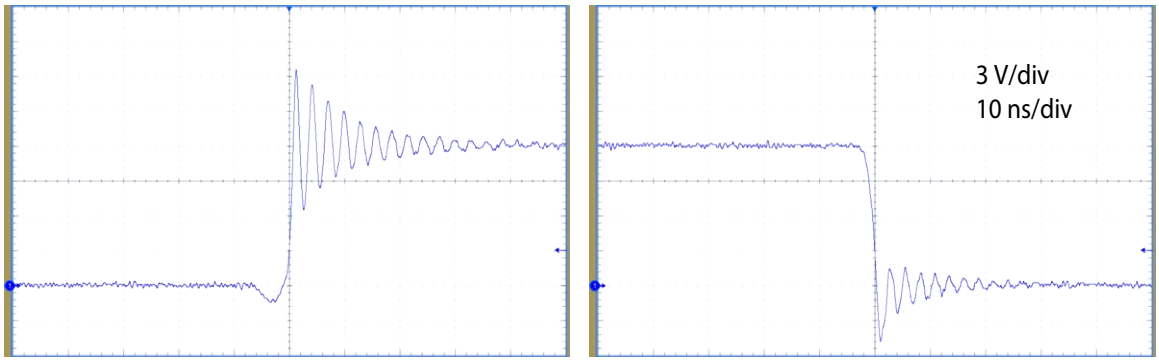


Figure 14: Measured switchnode voltage at 12 V_{IN}, 1 V_{OUT}, 1 MHz, 61 A

EFFICIENCY and POWER LOSSES

Figure 15 shows the efficiency and total power losses at various switching frequencies. The values reported correspond to the thermal steady state with no heatsink installed and 400 LFM of forced airflow.

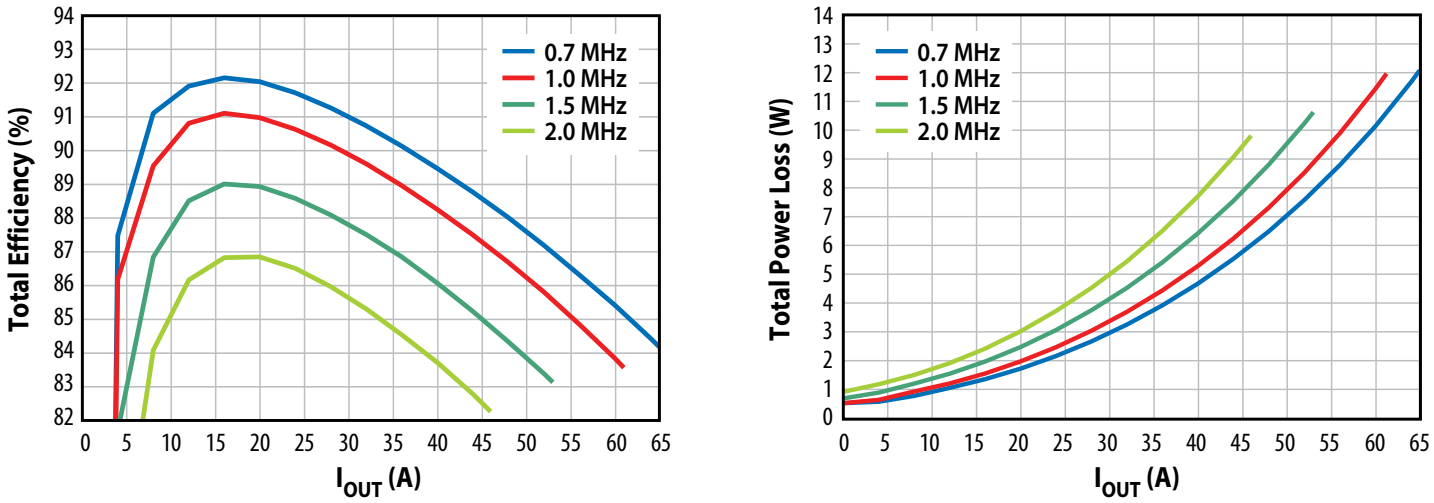


Figure 15: Measured efficiency at 12 V_{IN}, 1 V_{OUT}, across various switching frequencies, up to a maximum output current that results in 100°C of case temperature

Figure 16 shows the efficiency and total power losses at various input voltages. The values reported correspond to the thermal steady state with no heatsink installed and 400 LFM of forced airflow.

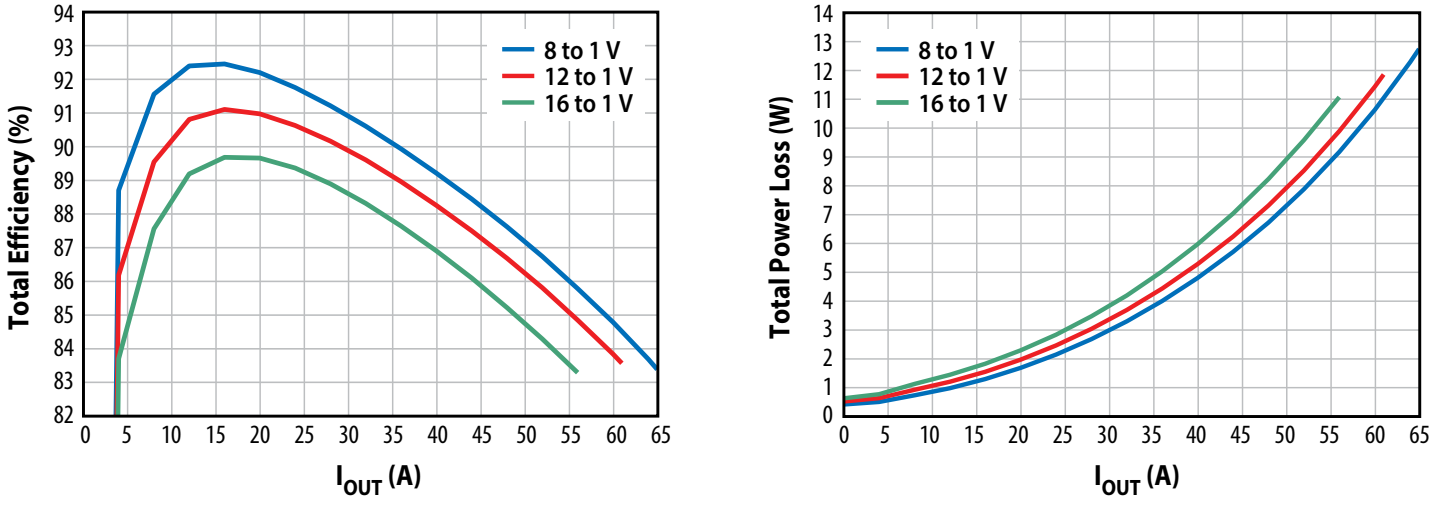
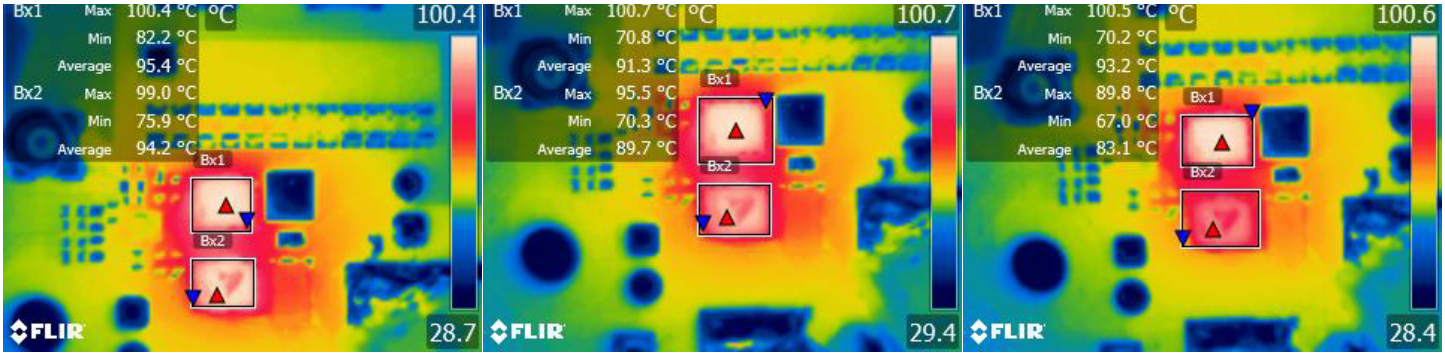


Figure 16: Measured efficiency at 1 MHz, 1 V_{OUT}, across various input voltages, up to a maximum output current that results in 100°C of case temperature

THERMAL PERFORMANCE

Figure 17 shows thermal performance at various input voltages. The values reported correspond to the thermal steady state with no heatsink installed and 400 LFM of forced airflow.



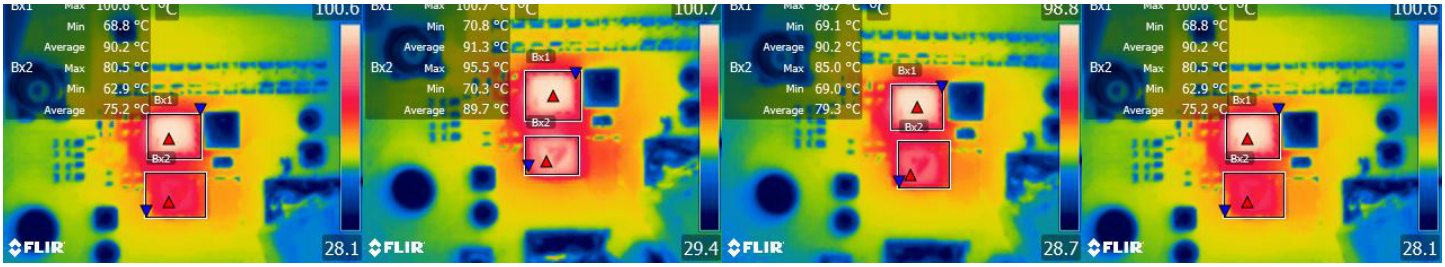
I_{OUT} = 65 A
V_{IN} = 8 V

I_{OUT} = 61 A
V_{IN} = 12 V

I_{OUT} = 56 A
V_{IN} = 16 V

Figure 17: Thermal images of EPC90175 operating at 1 MHz and 1 V_{OUT} with 25°C ambient temperature

Figures 18 shows thermal performance at various switching frequencies. The values reported correspond to the thermal steady state with no heatsink installed and 400 LFM of forced airflow.



I_{OUT} = 65 A
Frequency = 0.7 MHz

I_{OUT} = 61 A
Frequency = 1 MHz

I_{OUT} = 53 A
Frequency = 1.5 MHz

I_{OUT} = 46 A
Frequency = 2 MHz

Figure 18: Thermal images of EPC90175 operating at 12 V_{IN}, 1 V_{OUT}, maximum current required to reach 100°C, across various switching frequencies with 25°C ambient temperature

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC90175 landing page at: https://epc-co.com/epc/products/evaluation-boards/EPC90175

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