Demonstration Board EPC91107KIT Quick Start Guide

5 kW, 240 V_{AC_RMS} to 400 V_{DC} 4-Level Totem-Pole PFC Converter using EPC2304

June 2025

Revision 1.0

DESCRIPTION

The EPC91107KIT is a 5 kW, 4-Level Totem-Pole Power Factor Correction Converter featuring the 200 V rated, 5 mΩ $R_{DS(on)}$, EPC2304. The EPC91107KIT can draw up to 25 A_{AC_RMS} continuous current from the input. The EPC91107KIT was designed for Server Power supplies and is capable of meeting many of the Open Compute Project requirements. The system includes an EMI filter, in-rush current limit startup circuit, housekeeping power supply, and high-performance controller. The EPC91107KIT includes many critical features that allow for detailed performance evaluation, including measurement ports and access to critical circuit nodes. Figure 1 shows an image of the EPC91107KIT highlighting the various boards.

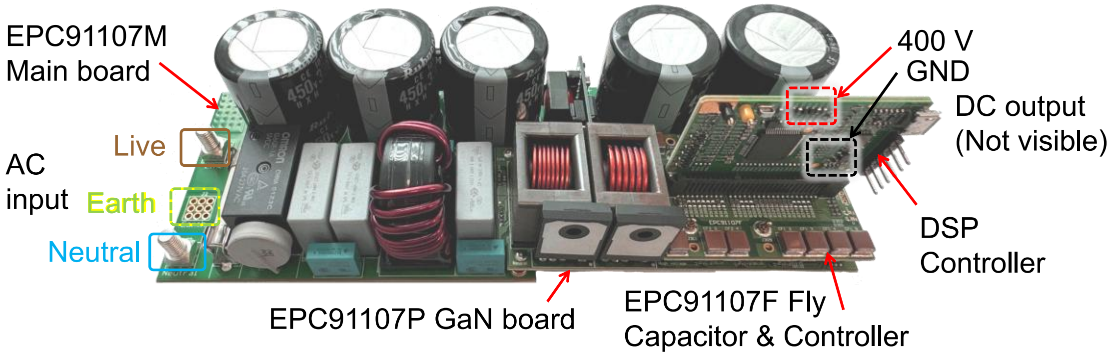

Figure 1: Photo overview of the EPC91107KIT board highlighting the main sections

The power circuit schematic of the EPC91107KIT converter is shown in Figure 2 with the control signal names. The topology is based on a totem-pole PFC where the high frequency leg ($Q_{1\text{-}3X}$) is a four-level flying capacitor configuration. Also shown is the EMI filter and in-rush current limit circuit.

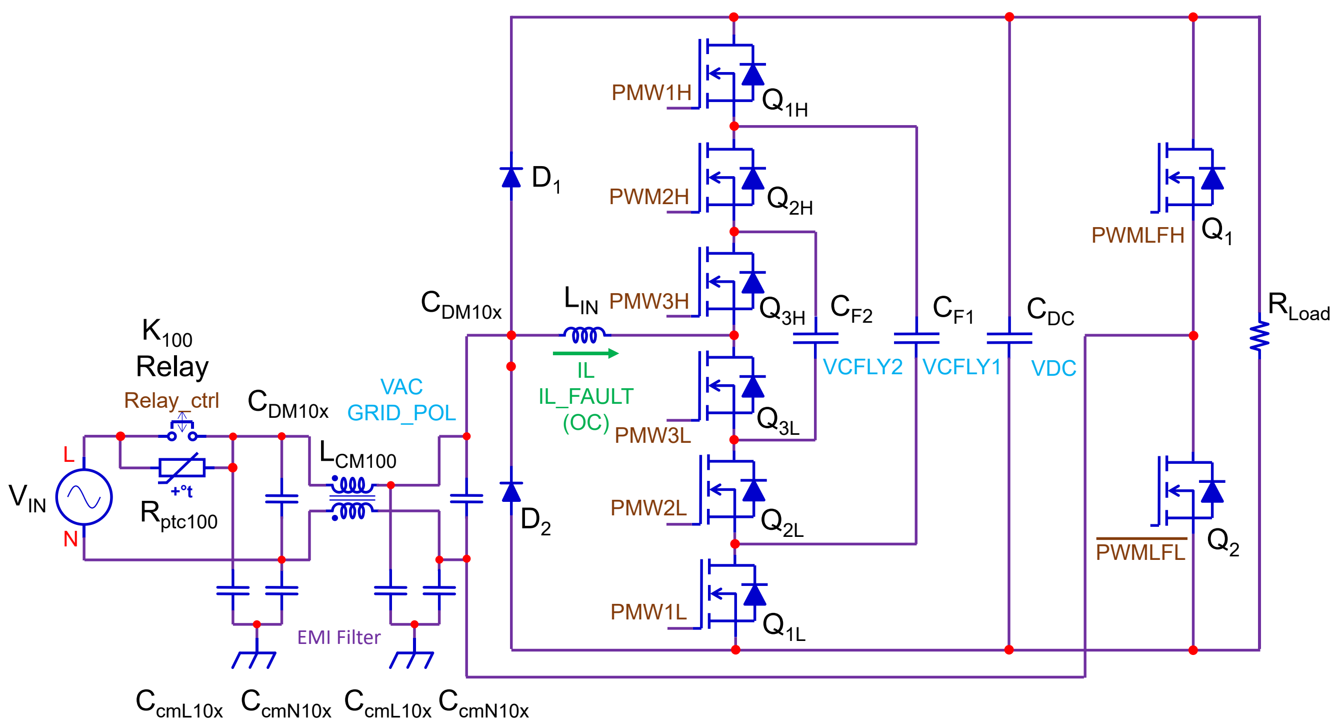

Figure 2. Power schematic of the EPC91107KIT.

MAIN FEATURES

- High efficiency, high power density four-level totem-pole topology
- Housekeeping power supply
- Single common-mode choke EMI Filter
- AC in-rush current limiter
- High power factor (complies with OCP standard)
- Low iTHD (complies with OCP standard)
- High dynamic current response
- Simple assembly
- No special components

RECOMMENDED OPERATING CONDITIONS

Table 1: Electrical Specifications (T_A = 25°C) EPC91107KIT

Symbol	Parameter	Conditions	Min.	Nom.	Max.	Units
V_{IN}	Input Supply Voltage	Full power range (5 kW)	200	240	277	V_{AC_RMS}
V_{IN_abs}	Full Range Input Supply Voltage	Output power derated	85		305(1)	V_{AC_RMS}
I_{IN}	Input Supply Current	Continuous, Fuse = 32 A_{RMS}			25	A_{AC_RMS}
F_{IN}	Grid Frequency		47		63	Hz
V_{OUT}	Output Voltage		384	400	416	V_{DC}
V_{Omax}	Absolute max. output voltage				450	V_{DC}
I_{OUT}	Output Current	Continuous		12.5(2)		A_{DC}
V_{Out_Rip}	Peak-to-peak output Voltage ripple at twice input frequency	At full load current		32		V
f_{sw}	FET switching frequency (PFC Inductor will be 3x)			140		kHz

(1) Can function up to 305 V_{AC_RMS}, EMI filter ceramic common mode capacitors cannot exceed 277 V_{AC_RMS}.

(2) EPC91107KIT has no heatsink installed. **High airflow forced air cooling is required at high load power levels. Device temperature must be observed by thermal camera to ensure device temperature is withing datasheet maximum levels.**

HIGHLIGHTED PARTS

The EPC91107KIT comprises four PCB assemblies, shown in Figure 3 and each performing a specific function. The four PCB assemblies are:

1) EPC91107M – Main motherboard with in-rush current limit circuit, EMI filter, housekeeping power supply, main bus capacitors and connections for the GaN board assembly (EPC91107P) and is shown in Figures 4 and 5,
2) EPC91107P – GaN board assembly that is the complete multi-level totem pole PFC converter and includes connection to the flying capacitor and controller interface board assembly (EPC91107F) as shown in Figures 6 and 7,
3) EPC91107F - Flying capacitor and controller interface board assembly that includes the bulk of the flying capacitors and the connection interface for the controller card as shown in Figures 8 and 9,
4) Controller card - Standard Microchip Plug-In-Module (PIM) controller.

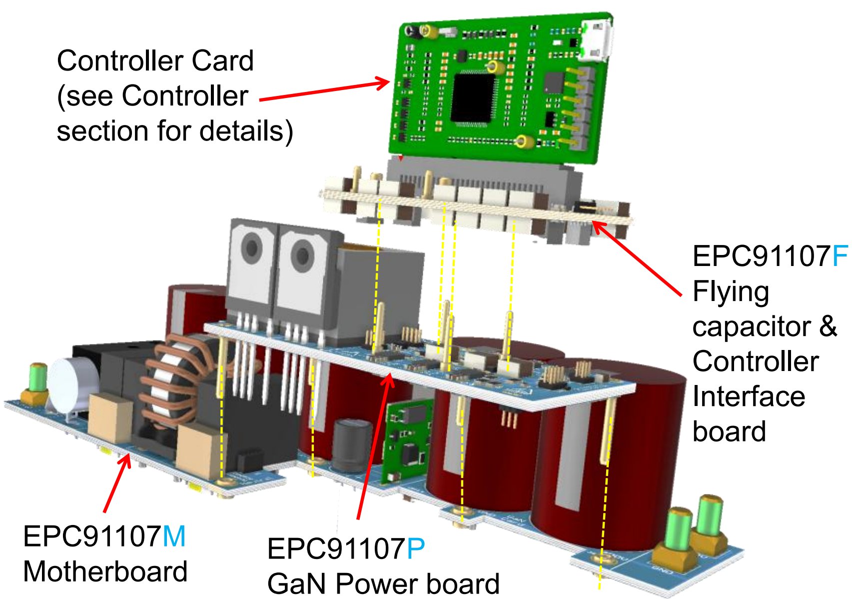

Figure 3: EPC91107KIT exploded view of the assembly.

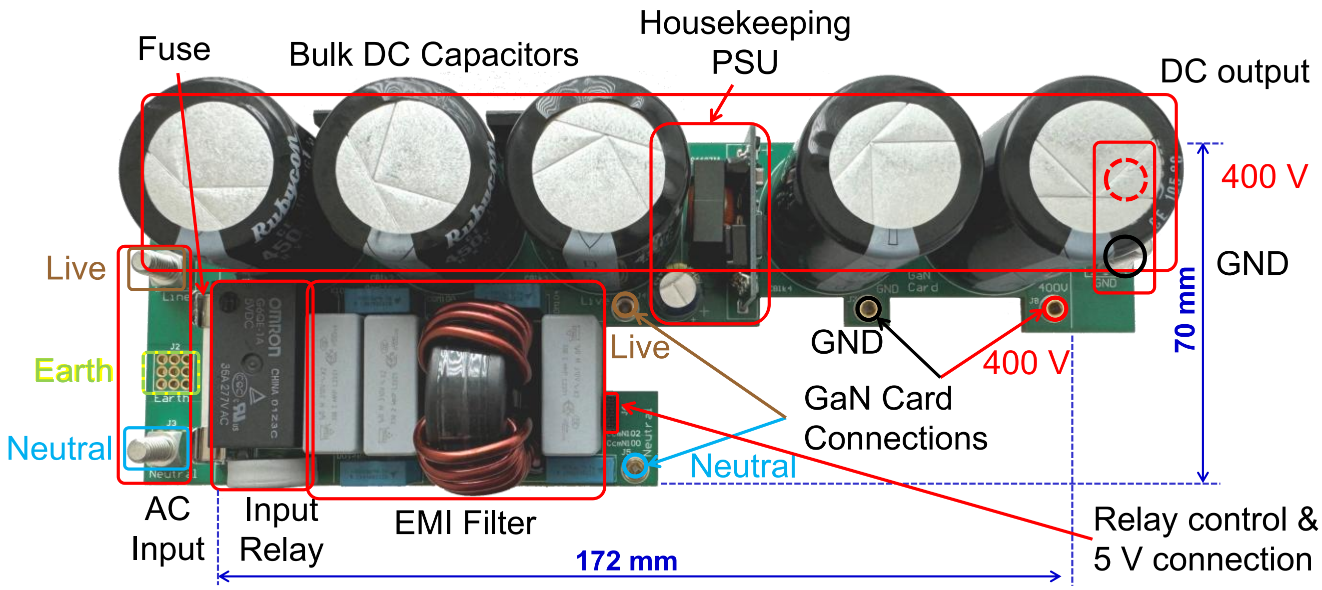

Figure 4: Top view of the EPC91107KIT motherboard EPC91107M showing the main circuit elements.

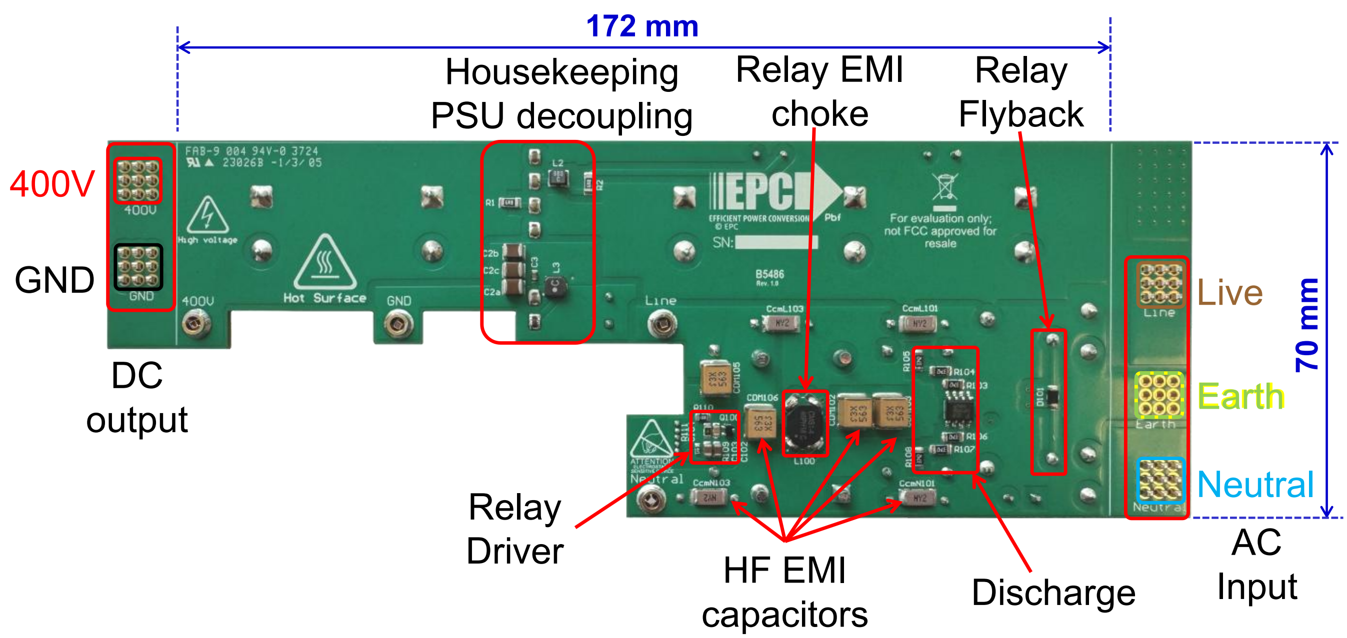

Figure 5: Bottom view of the EPC91107KIT motherboard EPC91107M showing the main circuit elements.

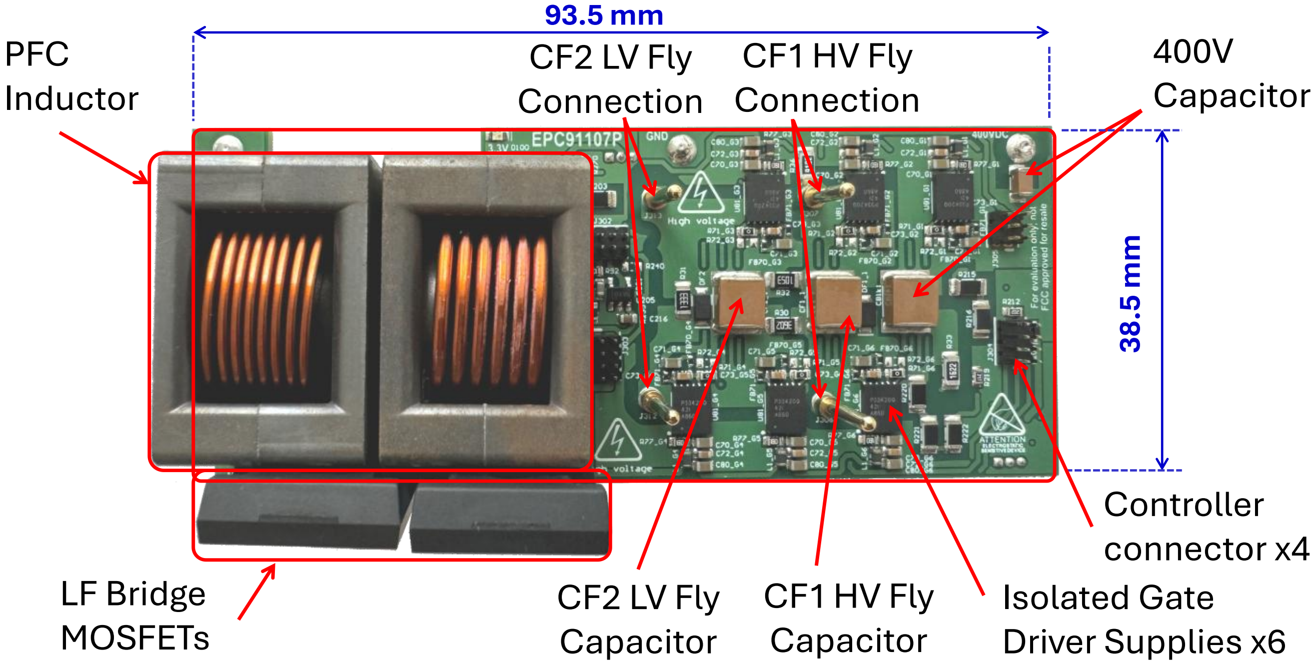

Figure 6: Top view of the EPC91107KIT GaN power board EPC91107P showing the main circuit elements.

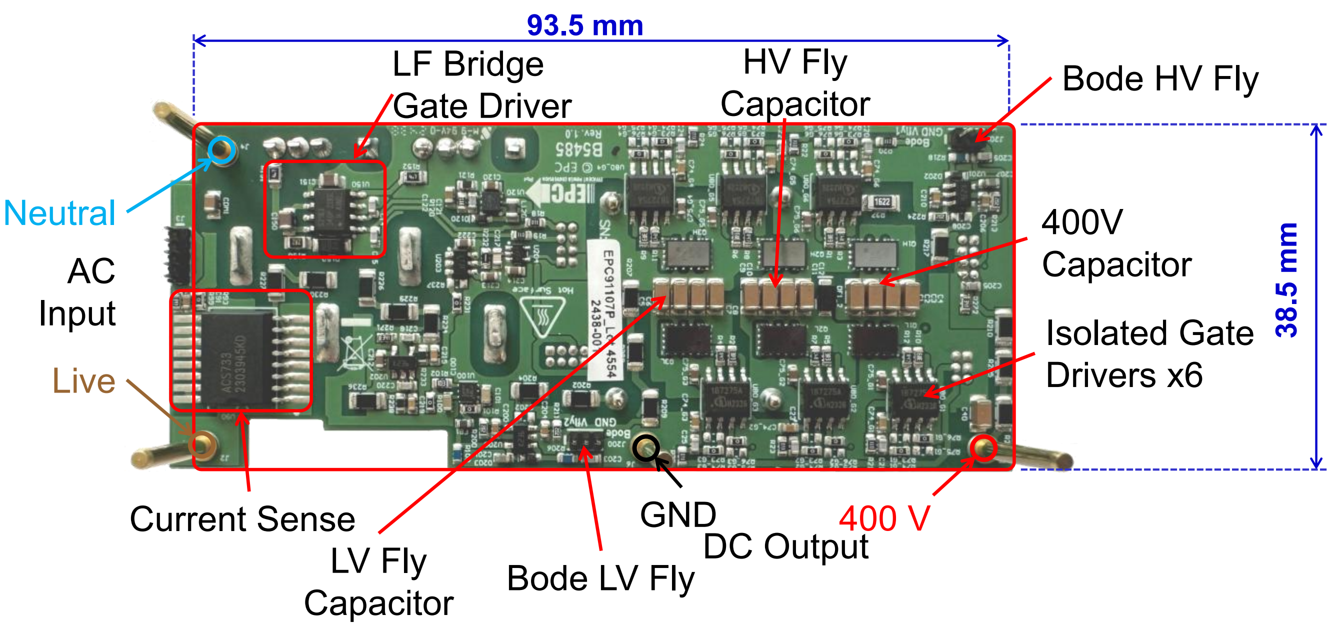

Figure 7: Bottom view of the EPC91107KIT GaN power board EPC91107P showing the main circuit elements.

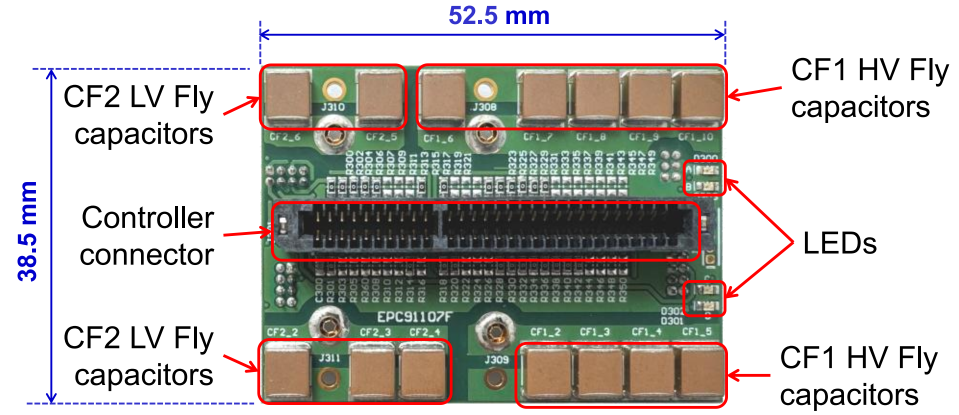

Figure 8: Top view of the EPC91107KIT Flying capacitor and controller interface board EPC9110F showing the main circuit elements.

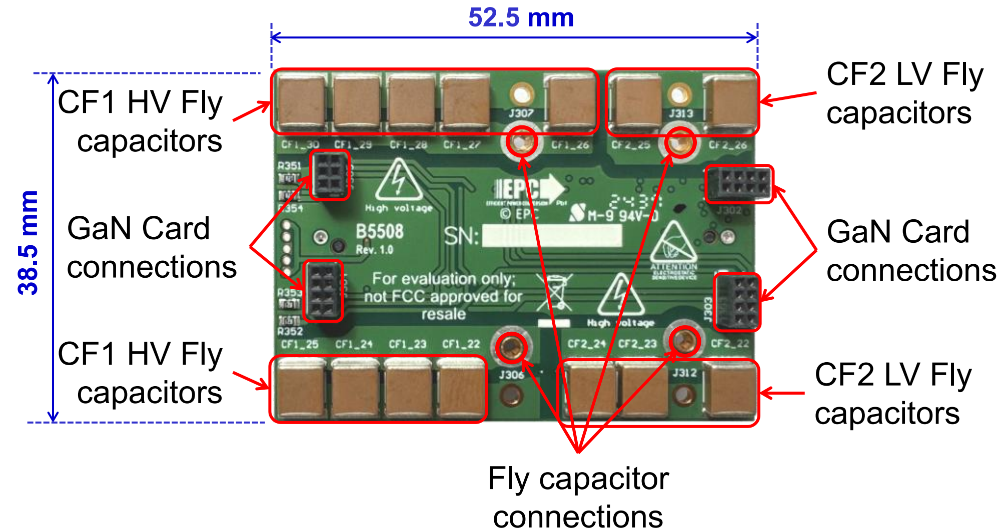

Figure 9: Bottom view of the EPC91107KIT Flying capacitor and controller interface board EPC9110F showing the main circuit elements.

Controller board

The EPC91107KIT comes with a vertical mount edge connector that is compatible with Microchip's PIM controllers as shown in Figure 10. These controllers feature a MCP2221A USB to UART/I^{2}C serial converter, various analog inputs with op amp buffers, and a 250ps PWM resolution.

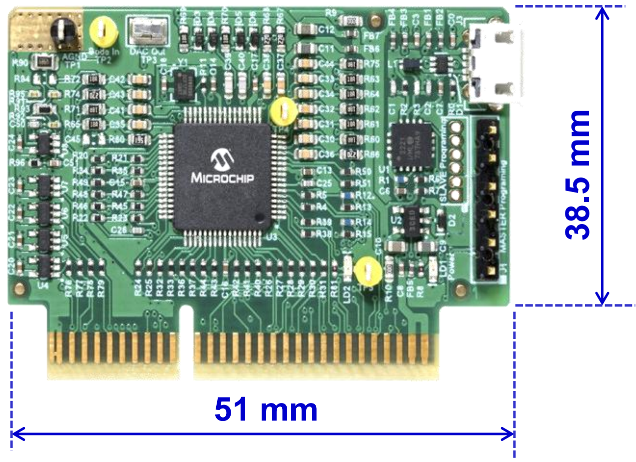

Figure 10: Photo of a typical controller card for the EPC91107KIT.

Compatible controllers are listed as follows:

1) **MA330048** (**Tested**) featuring the dsPIC33CK256MP506 (64 pin) DSP controller,
2) **EV12Y79A** (**In test**) featuring the dsPIC33CK512MP606 (64 pin) DSP controller,
3) **EV42F30A** (under development) featuring the dsPIC33AK512MPS506 next generation dsPIC

The EPC91107KIT **default** controller is the MA330048 and requires the following modifications:

- C41 (size 0603): Add 220 nF > 16 V in parallel (Vref – pin 4)
- C42 (size 0603): Add 220 nF > 16 V in parallel (Vcfly2 – pin 9)
- C35 (size 0603): Add 47 nF > 16 V in parallel (Vac – pin 6)
- C30 (size 0603): Add 47 nF > 16 V in parallel (IL – pin 12)

Where Figure 11 shows the position of the various components.

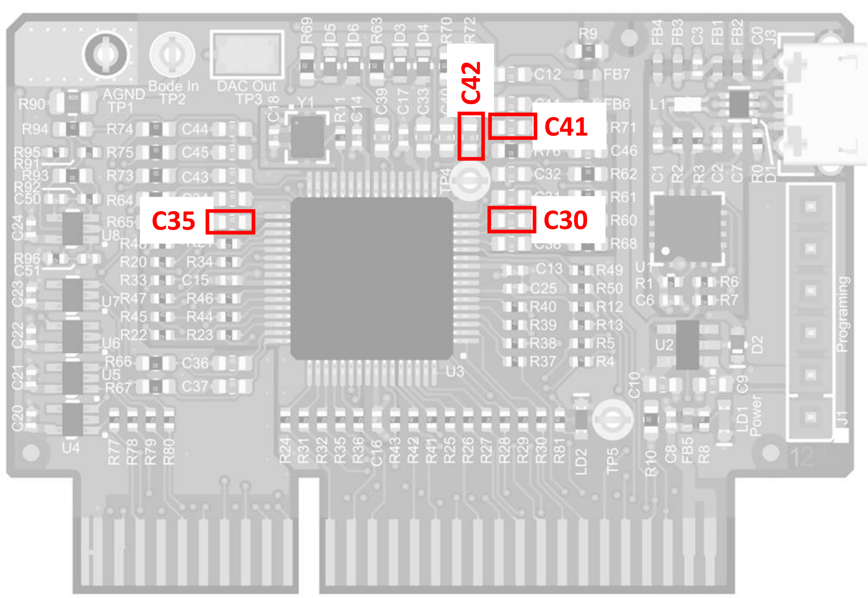

*Figure 11: **MA330048** component modifications locations for compatibility with the EPC91107KIT.*

The EPC91107KIT **alternative** controller is the EV12Y79A and requires the following modifications:

- C42 (size 0603): Add 220 nF > 16 V in parallel (V_{ref} – pin 4)
- C43 (size 0603): Add 220 nF > 16 V in parallel (V_{cfly2} – pin 9)
- C37 (size 0603): Add 47 nF > 16 V in parallel (V_{ac} – pin 6)
- C30 (size 0603): Add 47 nF > 16 V in parallel (I_L – pin 12)

Where Figure 12 shows the position of the various components.

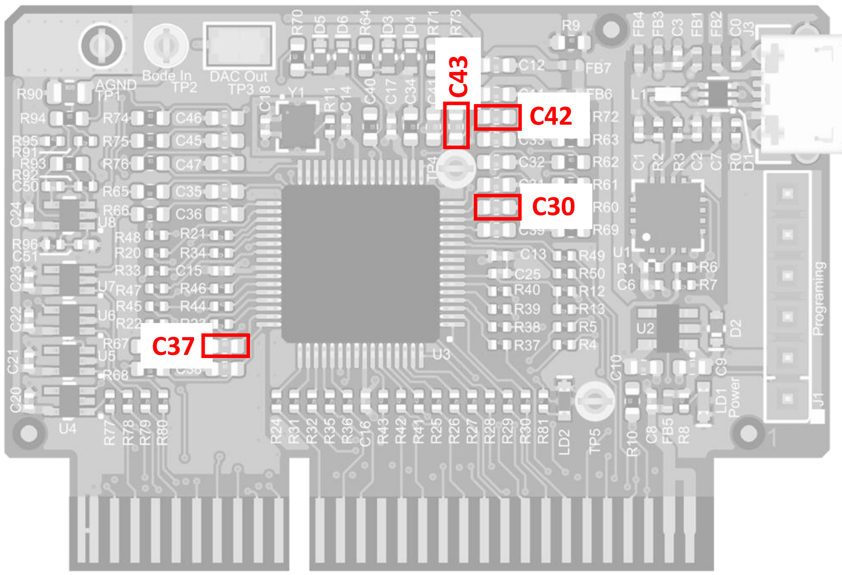

*Figure 12: **EV12Y79A** component modifications locations for compatibility with the EPC91107KIT.*

Relay and control power pin assignment

Table 2: EPC91107M and EPC91107P relay and control power pin map on connectors J6 and J3 respectively.

EPC91107M/P pin number	Function name	Description	Type	Input/ Output	Electrical
1,5	5V	5 V supply for gate drivers and controller card	Power	-	6.3V max, 500 mA max
2,4	Relay_ctrl	Control signal to close in-rush limit relay	Digital	Output	0 V - 3.3 V
3	GND	Power Ground	Power	-	-

Controller Pin Assignment

Table 3: EPC91107F controller pin map on connector J301.

EPC91107F pin number	Function name	Description	Type	Input/ Output	Electrical	PIM - Edge connector pin #
1,2	AGND	Analog Ground	Power	-	-	1,2
3	DAC	Voltage reference Feedback	Analog	Output	0 V - 3.3 V	3
4	VREF	Analog reference voltage feedback	Analog	Input	0 V - 3.3 V offset = 1.65 V	4
6	VAC	AC voltage feedback	Analog	Input	0 V - 3.3 V offset = 1.65 V	6
8	IL	PFC Inductor current feedback	Analog	Input	0 V - 3.3 V offset = 1.65 V	8
9	VCFLY2	LV Flying Capacitor CFLY2 voltage feedback (VDC/3)	Analog	Input	0 V - 3.3 V	9
10	VDC	DC voltage feedback	Analog	Input	0 V - 3.3 V	10
12	IL	PFC Inductor current feedback	Analog	Input	0 V - 3.3 V offset = 1.65 V	12
17	VCFLY1	HV Flying Capacitor CFLY1 voltage feedback (2·VDC/3)	Analog	Input	0 V - 3.3 V	17
21	TX	UART TX	Digital	Output	0 V / 3.3 V	23
22	LED1	Indicator LED 1	Digital	Output	0 V / 3.3 V	24
23	RX	UART RX	Digital	Input	0 V / 3.3 V	25
30	PWMLFL	Low frequency bridge, low side FET PWM	Digital (active low)	Output	0 V / 3.3 V	32
31	LED2	Indicator LED 2	Digital	Output	0 V / 3.3 V	33
32	PWMLFH	Low frequency bridge, high side FET PWM	Digital	Output	0 V / 3.3 V	34
33	GRID_POL	Grid polarity	Digital	Input	0 V / 3.3 V	35
34	LED4	Indicator LED 4	Digital	Output	0 V / 3.3 V	36
35	PWM3H	PWM innermost Upper	Digital	Output	0 V / 3.3 V	37
36	IL_FAULT	PFC inductor over-current current fault	Digital (active low)	Input	0 V / 3.3 V	38
37	LED3	Indicator LED 3	Digital	Output	0 V / 3.3 V	39
38	PWM2L	PWM center pair Lower	Digital	Output	0 V / 3.3 V	40
39	PWM3L	PWM innermost Lower	Digital	Output	0 V / 3.3 V	41
40	PWM2H	PWM center pair Upper	Digital	Output	0 V / 3.3 V	42
41	Relay_ctrl	In-rush relay control	Digital	Output	0 V / 3.3 V	43
43	PWM1H	PWM outermost Upper	Digital	Output	0 V / 3.3 V	45
45	PWM1L	PWM outermost Lower	Digital	Output	0 V / 3.3 V	47
55,57	5V	5V supply	Power	-	6.3V max, 70 mA max	57,59
56,58	GND	Power Ground	Power	-	-	58,60

External 5V connection

An external 5V supply can be connected directly across the 5V output of the housekeeping power supply with minimum voltage of 5.0 V and maximum of 5.5 V as shown in Figure 13. The external power supply needs to be 2 A capable and must be fully isolated from the ground of the EPC91107KIT unit with at least 600 V capability.

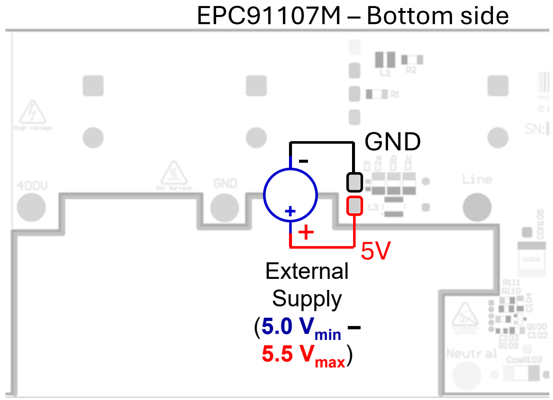

Figure 13: External 5V connection location on EPC91107M.

Switch-node voltage measurement

Figure 14 shows the location to measure the switch-node (SWN) voltage with respect to neutral. It is important to use a high-voltage differential probe for this measurement.

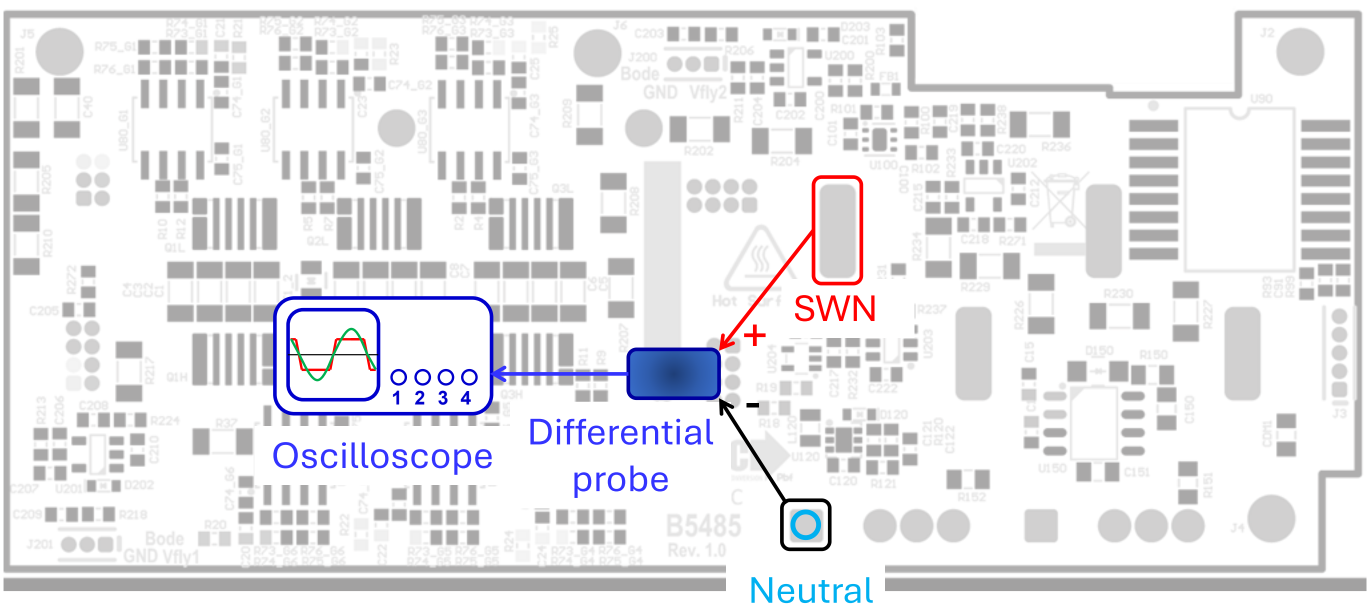

Figure 14: Location for the switch-node (SWN) to neutral measurement.

Controller Summary

The control diagram for the EPC91107KIT is shown in Figure 15 and primarily comprises a traditional totem-pole PFC controller. There is a phase lock loop that locks to the grid frequency and produces a sinusoidal reference used throughout the controller. An outer voltage loop determines the peak current reference that only updates once a cycle using the zero-order hold (ZOH) function which is followed by a multiplier that produces the actual current reference. The current control loop determines the duty-cycle setpoint using the difference between the measured current and current reference that is added with the predictive duty cycle determined from the output voltage measurement and the generated sinusoidal input voltage reference.

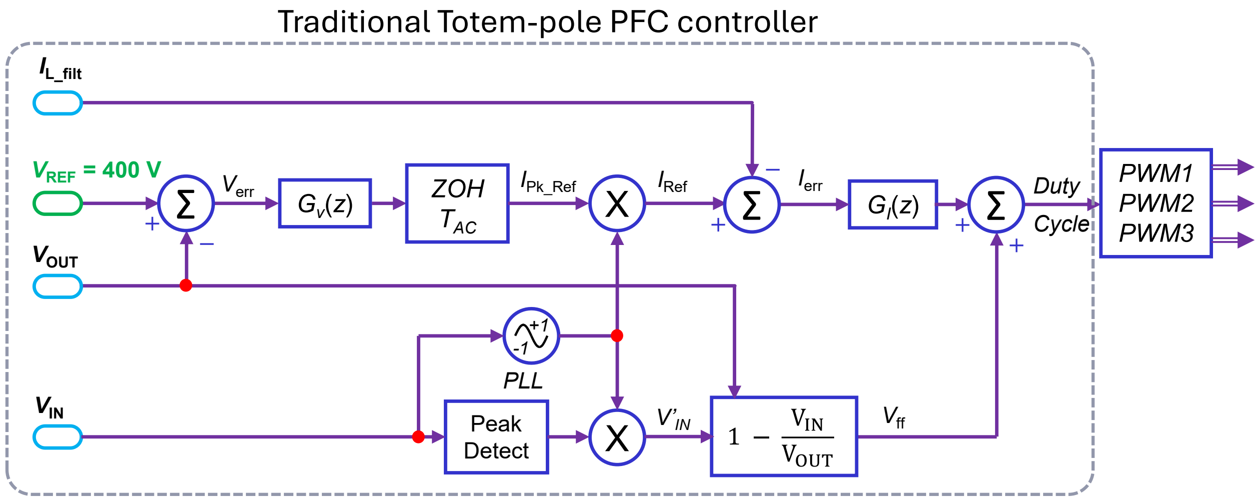

Figure 15: Block diagram of the four-level PFC controller.

The PWM generator uses the duty-cycle setpoint and splits into three independent complementary PWM generators that are 120° phase shifted with respect to each other as shown in Figure 16.

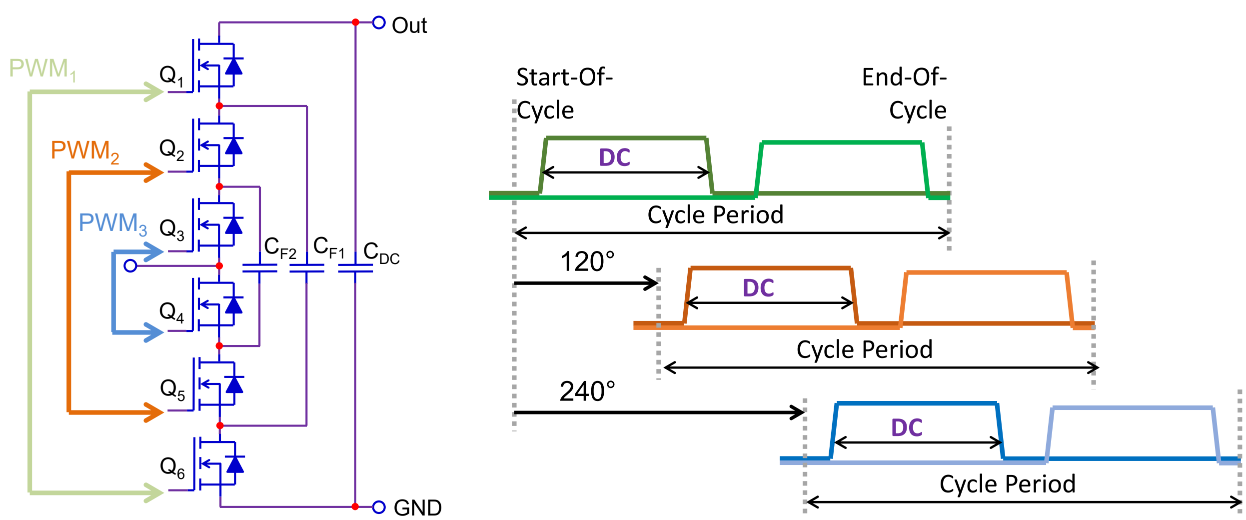

Figure 16: Multi-level bridge PWM signal allocation and pairs.

THERMAL CONSIDERATIONS

The EPC91107KIT is not equipped with a heatsink, so caution must be taken when operating at high power where the devices generate high heat flux to prevent over-temperature of the devices. **It is recommended to use a high rate of forced air cooling over the power FETs located on the bottom side of the EPC91107P board and monitor the temperature using a thermal camera to ensure that the temperatures of the FETs are within datasheet limits**.

The addition of heatsink can significantly improve the heat dissipation from the GaN FETs by adding cooling from the top side of the device and thus reduce the amount of forced air required to maintain the FET temperatures within the datasheet limits and at high power loads. Figure 17 shows cross-sectional view of the cooling system suitable for the EPC91107P board. A SMD spacer is used to set the correct height for the heat-sink or spreader above the FETs and provide the correct compression for the thermal interface material.

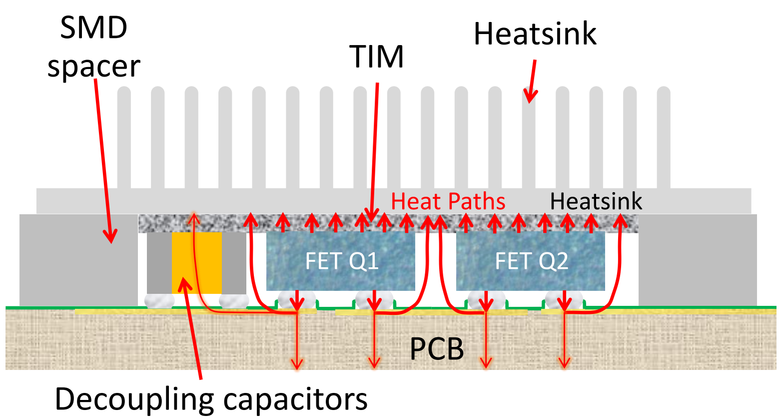

Figure 17: Cross-sectional view of the back-side cooling thermal system.

It is important that the TIM for the eGaN FETs also serves to electrically insulate those connections from the heat-spreader. It may be necessary to first place a heat-spreader above the FETs before interfacing to a larger heatsink. The heat-spreader TIM is then placed over the heat-spreader and the heatsink is then carefully placed on top.

The choice of TIM for the eGaN FETs needs to consider the following characteristics:

Mechanical compliance – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the eGaN FET/IC. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.

Electrical insulation – The backside of the eGaN FET is a silicon substrate that is connected to the Source. Electrical insulation from each GaN FET to the heat-spreader / heatsink is required for the thermal solution.

Thermal performance – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials are preferred to provide higher thermal conductance at the interface.

The thermal requirements for the choice of TIM for the heat-spreader can be relaxed due to the larger areas which allows the use of lower thermal conductivity materials with negligible impact on thermal performance. To help make up for the lower thermal conductivity, a thinner sheet may be used.

EPC recommends the t-Global Part Number: TG-A1780 for the eGaN FETs TIM as it has a high thermal conductivity of 17.8 W/m·K. For the heat-spreader TIM, the t-Global Part Number: TG-A620 with a moderate thermal conductivity of 6.2 W/m·K can be used.

POWER CONNECTION

Connecting power to the EPC91107KIT is very simple and shown in Figure 18. It is important to use a programmable power supply for the AC source until such time EPC releases a version of the controller code tested on “dirty” grids. In addition, the AC source should be selected with sufficient power rating to power the EPC91107KIT.

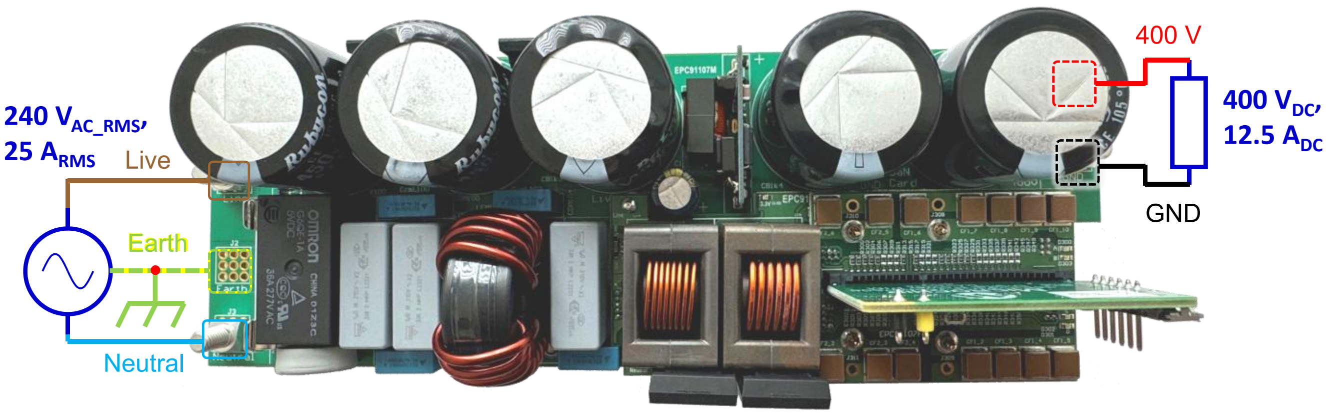

Figure 18: Power connections to the EPC91107KIT.

QUICK START PROCEDURE

Operating restrictions and precautions:

1) ONLY use a programmable AC source set to between 200 V AC and 277 V AC and with 50 or 60 Hz for initial testing. EPC will be providing updates on the controller code to ensure reliable operation on a "dirty" grid.
2) Do not activate the load until the unit is fully operational.
3) Ensure that high voltage safety pre-cautions are in place.
4) Never start the converter with the load activated. The PTC will heat up and open the circuit. Keep the DC programmable load off. Once the converter is operational, then you can change settings on the load. It is best practice at this time to make small load changes. Larger loads steps will be permissible with a future firmware release.
5) Make sure the AC source has sufficient power to operate the board. A minimum power requirement of 1kW is recommended.
6) The operating instructions in this document do not cover how to perform bode measurements. Please refer to the equipment manufacturer for those instructions.

Operating Procedure:

1) Connect the power supply (in the off position) and load as shown in Figure18.
2) Make sure the load is in the off position.
3) To start, simply turn on the AC source, do NOT turn up the power supply.
4) Make sure to cool the board (bottom side where the FETs are) with a fan. There is no heatsink so please use a thermal camera to monitor the temperature of the devices.
5) Exercise caution when taking measurements, particularly gate voltages, switch nodes etc. It is best practice to connect probes in a stable manner prior to operation.
6) Activate the load and increase in small steps. Always observe the temperature of the GaN FETs and do not exceed the maximum power of the system stated in table 1.
7) For shutdown, please follow steps in reverse. For custom tests other than described here, please contact EPC.

EXPERIMENTAL VALIDATION

Waveforms measured using a LeCroy MDA8108HD oscilloscope. Voltage measurement taken using LeCroy HVD3106A High Voltage Differential Probe and current measurement taken using a LeCroy CP031A 30A Current Probe.

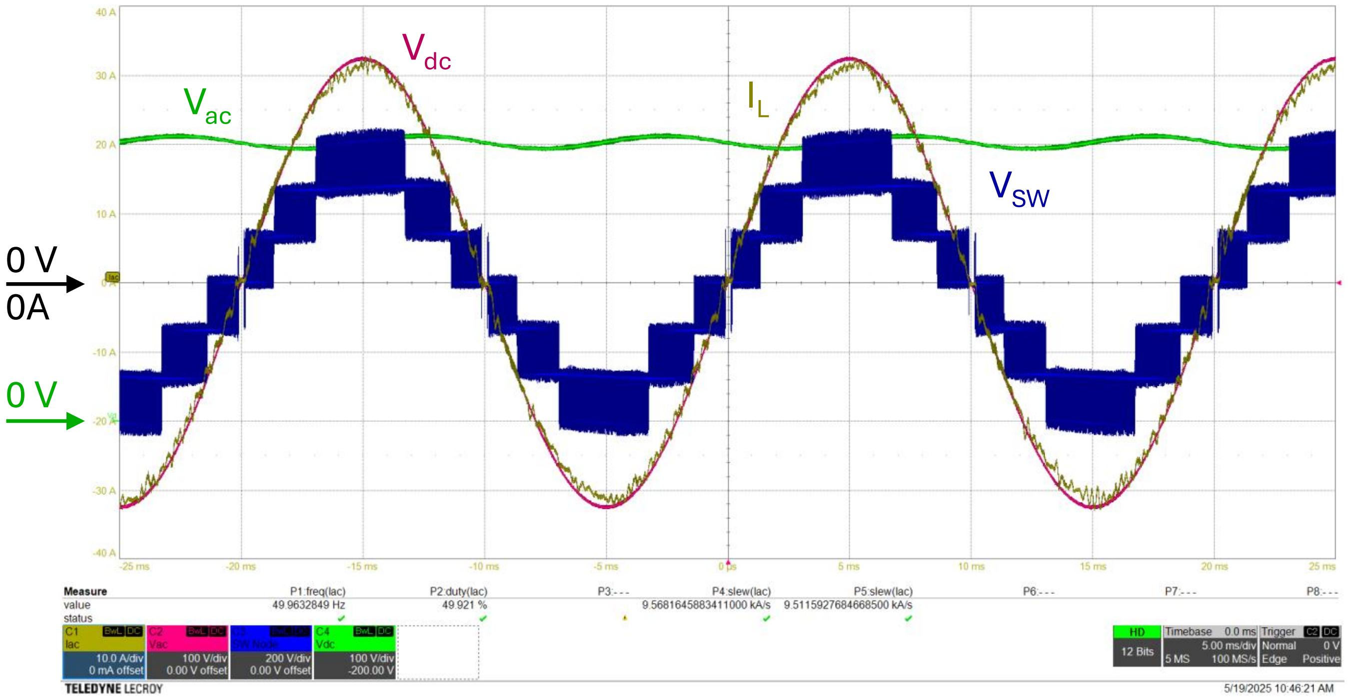

*Figure 19: Measured waveforms of the EPC91107KIT operating with V_{in} = 230 V_{RMS}, **50 Hz**, V_{out} = 400 V_{DC}, P_{out} = 5 kW and showing input voltage, input current, output voltage and switch-node voltage with respect to neutral.*

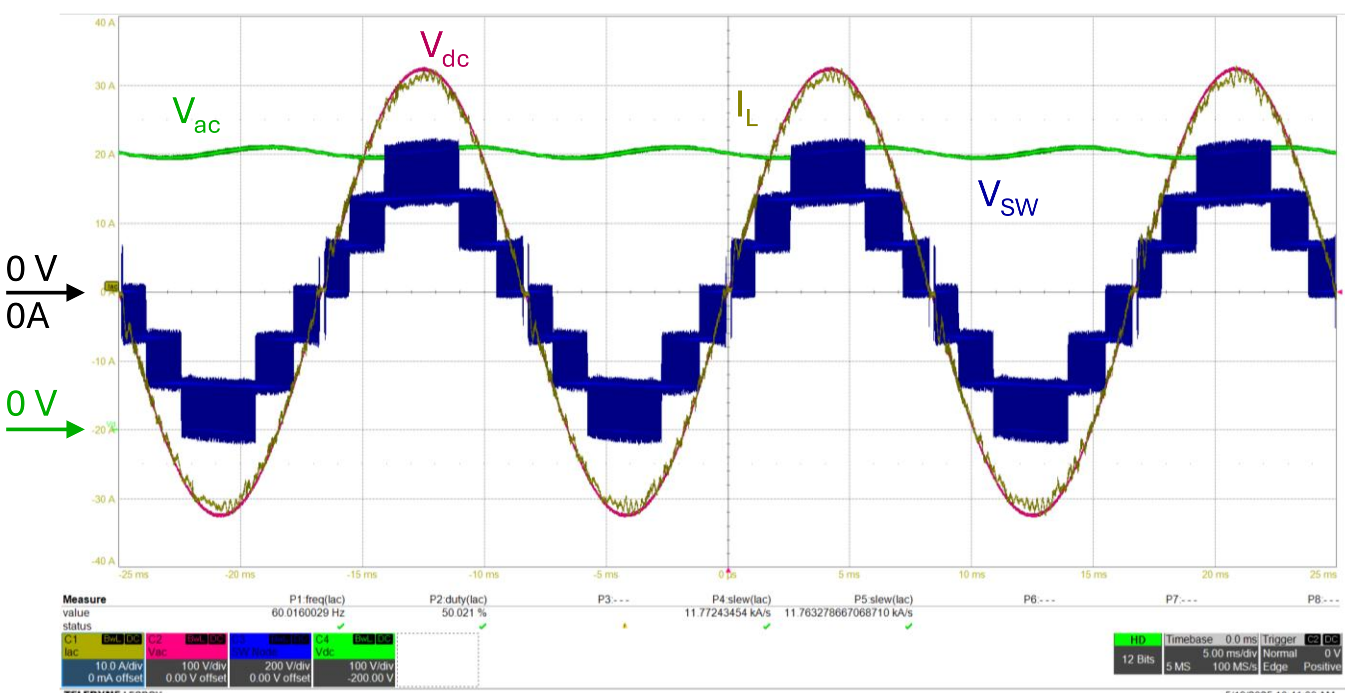

*Figure 20: Measured waveforms of the EPC91107KIT operating with V_{in} = 230 V_{RMS}, **60 Hz**, V_{out} = 400 V_{DC}, P_{out} = 5 kW and showing input voltage, input current, output voltage and switch-node voltage with respect to neutral.*

Efficiency, harmonic and power factor measurements taken using a Yokogawa WT500 power analyzer. Figure 21 shows the measured efficiency against the 80PLUS and OCP standards. The 80PLUS standard has been adjusted to allocate 50% losses to the PFC converter and 50% losses to the isolation stage and the efficiency adjusted upwards accordingly.

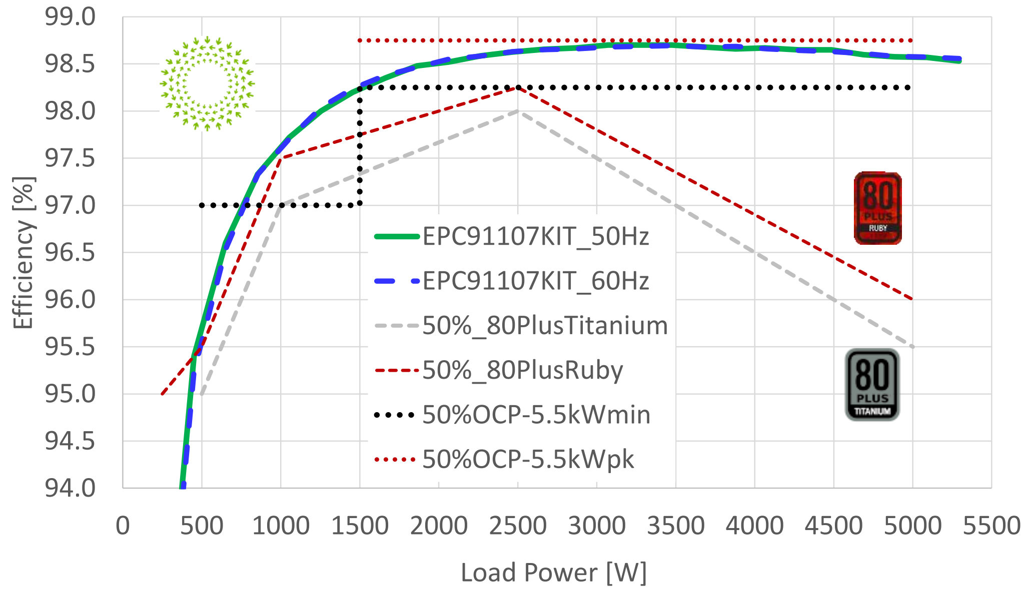

Figure 21: Measured eficiency operating with V_{in} = 230 V_{RMS}, at both 50Hz and 60Hz, V_{out} = 400 V_{DC}, including housekeeping power. Also shown are the 50% adjusted 80PLUS and OCP standards.

Input current total harmonic distortion (iTHD) is shown in Figure 22, for both 50Hz and 60Hz cases, against the M-CRPS and OCP standards. It should be noted that no special techniques have been implemented to achieve these results and require little additional effort to ensure full compliance with the standards.

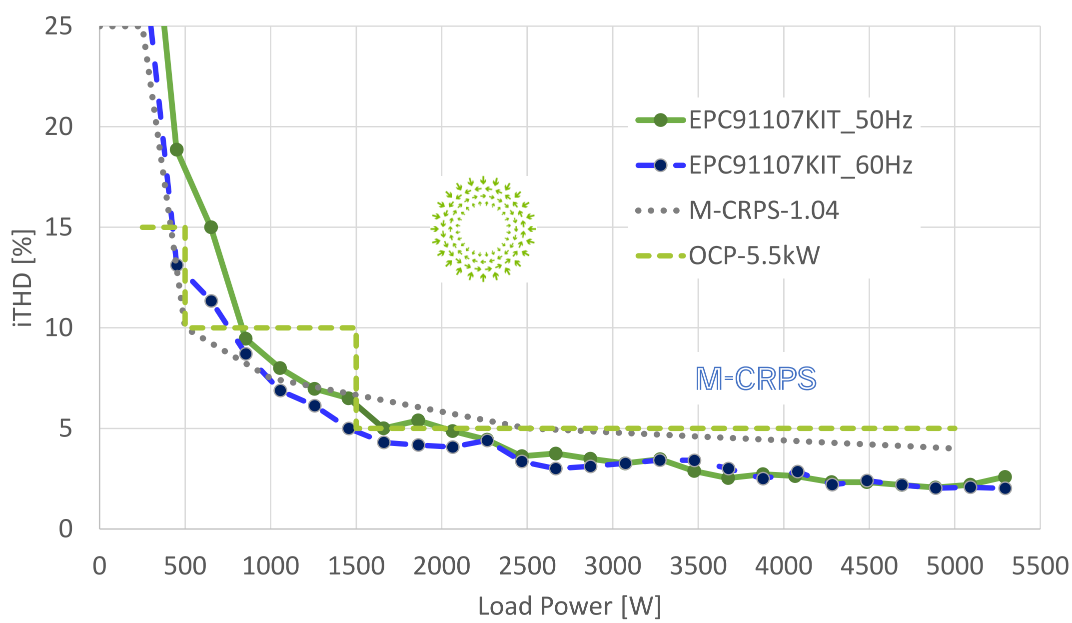

Figure 22: Measured iTHD operating with V_{in} = 230 V_{RMS}, V_{out} = 400 V_{DC} against the M-CRPS and OCP standards.

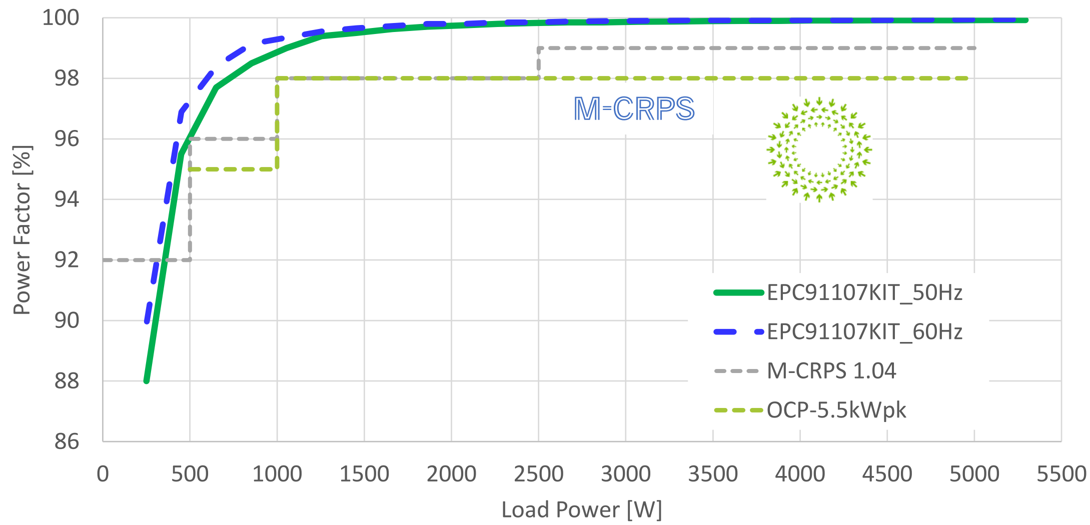

Figure 23: Measured power factor operating with V_{in} = 230 V_{RMS}, V_{out} = 400 V_{DC} against the M-CRPS and OCP standards.

Input power factor is shown in Figure 23, for both 50Hz and 60Hz cases, against the M-CRPS and OCP standards. It should be noted that with techniques to ensure compliance with iTHD will ensure full compliance with power factor standards.

PRECAUTIONS

The EPC91107KIT is a demonstration board configured as a four-level totem-pole PFC converter and is not tested to comply with all OCP or other standards. Please contact EPC for advanced tests to verify if the EPC91107KIT is capable of passing such tests.

Never operate the EPC91107KIT with a Microchip programmer connected to the unit. If communications to the unit is required during testing, EPC recommends using a USB isolator to prevent damage to the computer should a failure occur.

BOARD VERSIONS

Table 4: EPC91107KIT board number versions

Board Number	EPC91107M	EPC91107P	EPC91107F
Schematic Revision	2.0	1.5	1.5
PCB Revision	2.0	1.0	1.0

ACKNOWLEDGEMENTS

EPC would like to acknowledge Microchip Technology Inc. (www.microchip.com) for their support of this project. Microchip Technology Incorporated is a leading provider of smart, connected and secure embedded control solutions. Its easy-to-use development tools and comprehensive product portfolio enable customers to create optimal designs, which reduce risk while lowering total system cost and time to market. The company's solutions serve customers across the industrial, automotive, consumer, aerospace and defense, communications and computing markets. The EPC91107KIT demonstration board features the dsPIC33CK256MP506 16-Bit Digital Signal Controller with High-Speed ADC, Op Amps, Comparators and High-Resolution PWM. Learn more at www.microchip.com.

DOCUMENT HISTORY

Updated: 3 June 2025

Initial release: 21 May 2025

For support files including schematic, Bill of Materials (BOM), and Gerber files please contact an EPC representative.

For More Information:

Please contact info@epc-co.com
or your local sales representative

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EFFICIENT POWER CONVERSION

Evaluation Board Notification

The EPC91107KIT is intended for product evaluation purposes only. They are not intended for commercial use nor are they FCC approved for resale. Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions. This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

As an evaluation tool, this board is not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant.

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