Demonstration Board EPC91110KIT Quick Start Guide

5.5 kW, 400 V_{DC} to 50 V_{DC} Quad Series-Input, Parallel-Output, LLC Converter using EPC2305

June 2025

Revision 1.0

DESCRIPTION

The EPC91110KIT is a fixed-ratio, 5.5 kW, 400 V to 50 V isolated DC/DC converter composed of four modules in an ISOP (Input-Series Output-Parallel) configuration. Each module consists of an LLC converter that can operate as a standalone converter processing up to 1375 W between a 100 V input and a 50 V output. These LLC modules feature the same 150 V-rated 3 mΩ $R_{DS(on)}$ GaN transistors EPC2305, in the primary side and in the rectifier side. The converter has a volume of 80 mm x 70 mm x 27 mm and was designed for Server Power supplies following OCP ORv3 requirements. Figure 1 shows an image of the EPC91110KIT.

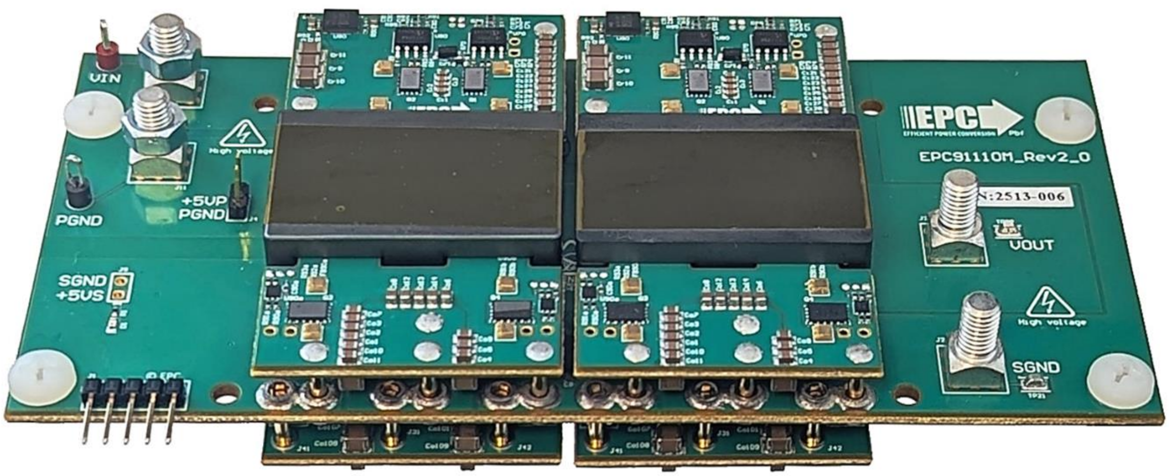

Figure 1: Photo overview of the EPC91110KIT board highlighting the main sections

Figure 2 shows a simplified circuit diagram with four 100 V to 50 V isolated LLC converters configured with their inputs connected in series and their outputs in parallel (ISOP). The result is an isolated 400 V to 50 V converter with a continuous power rating of 5.5 kW.

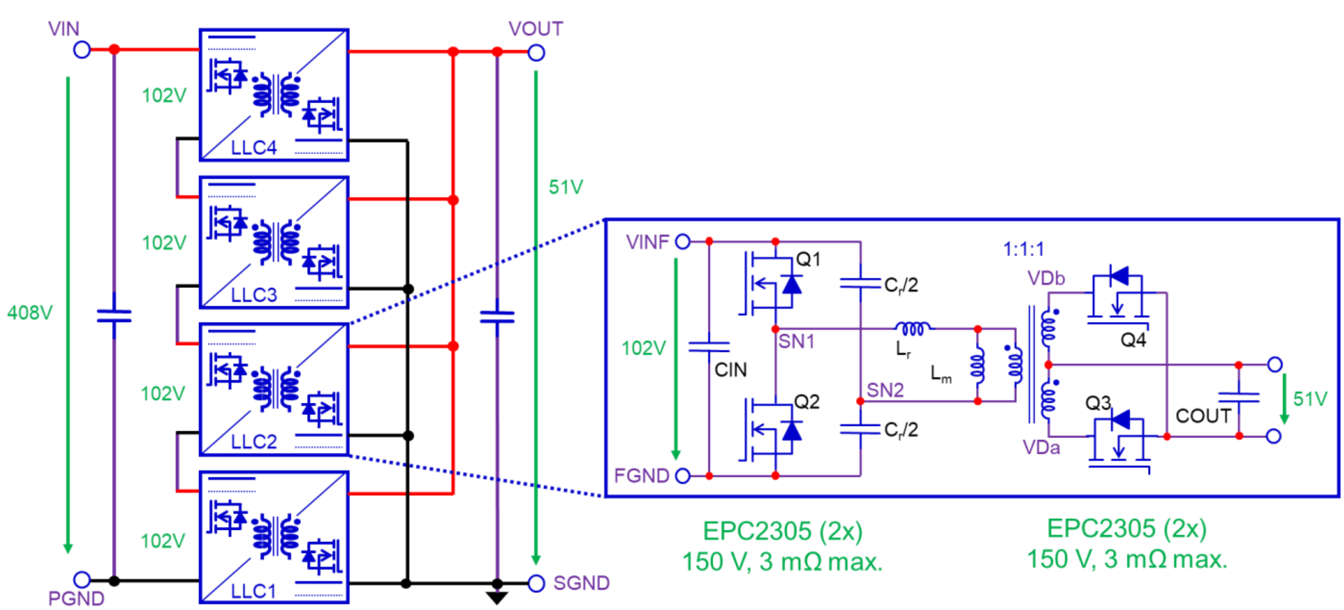

Figure 2. Power schematic of the EPC91110KIT.

MAIN FEATURES

- High efficiency and high power-density isolated 400 V to 50 V converter
- Fixed ratio (8:1) converter using four LLC modules configured in ISOP (Input-Series Output-Parallel)
- Full-load (5.5 kW) efficiency of 98 % and peak load efficiency of 98.2 %
- Self-balancing of the input voltage of each module
- Uses 150 V-rated GaN transistors with better figures of merit than 650 V-rated devices used in equivalent 2-level topologies
- Planar LLC transformer designed to meet isolation requirements per IEC 60950-1
- Meets OCP ORv3 size requirements
- Simple assembly
- No special components

FEATURED eGaN FETs

The EPC91110KIT features 150 V-rated eGaN® FETs with a maximum $R_{DS(on)}$ of 3 mΩ at 25°C. This eGaN FET is packaged in a 3 x 5 mm QFN with exposed top for optimal backside cooling. The same device is used in the primary of the LLC and in the rectifier, for a total of 4 FETs per LLC module, and 16 FETs per EPC91110KIT. More details available at www.epc-co.com.

RECOMMENDED OPERATING CONDITIONS

Table 1: Electrical Specifications (T_A = 25°C) EPC91110KIT

Symbol	Parameter	Conditions	Min.	Nom.	Max.	Units
V_{IN}	Input Voltage		360	408	450	V_{DC}
I_{IN}	Input Current				15	A_{DC}
V_{OUT}	Output Voltage	8:1 fixed ratio	45	51	56	V_{DC}
V_{Omax}	Absolute max. output voltage				60	V_{DC}
I_{OUT}	Output Current			110(1)		A_{DC}
V_{Out_Rip}	Peak-to-peak output Voltage ripple	V_{IN} = 408 V, P_{OUT} = 5.5 kW		xxx		V
f_{sw}	FET switching frequency			1		MHz

(1) EPC91110KIT has no heatsink installed. **High airflow forced air cooling is required at high load power levels. Device temperature must be observed by thermal camera to ensure device temperature is withing datasheet maximum levels.**

DESCRIPTION OF THE EPC91110KIT

The EPC91110KIT consists of 5 PCBs as follows: one motherboard (EPC91110**M**) and four LLC modules (EPC9561), as shown in Figure 3.

- EPC91110M: A motherboard with the input/output connectors, the microcontroller, some input/output ceramic capacitors and power and signal connections to the LLC modules.
- EPC9561: Four identical LLC modules are used in each KIT. Each module contains the primary and secondary FETs and gate drivers, the transformer, the resonant tank, a 5V-to-5V isolated DC/DC converter and some input/output ceramic capacitors.

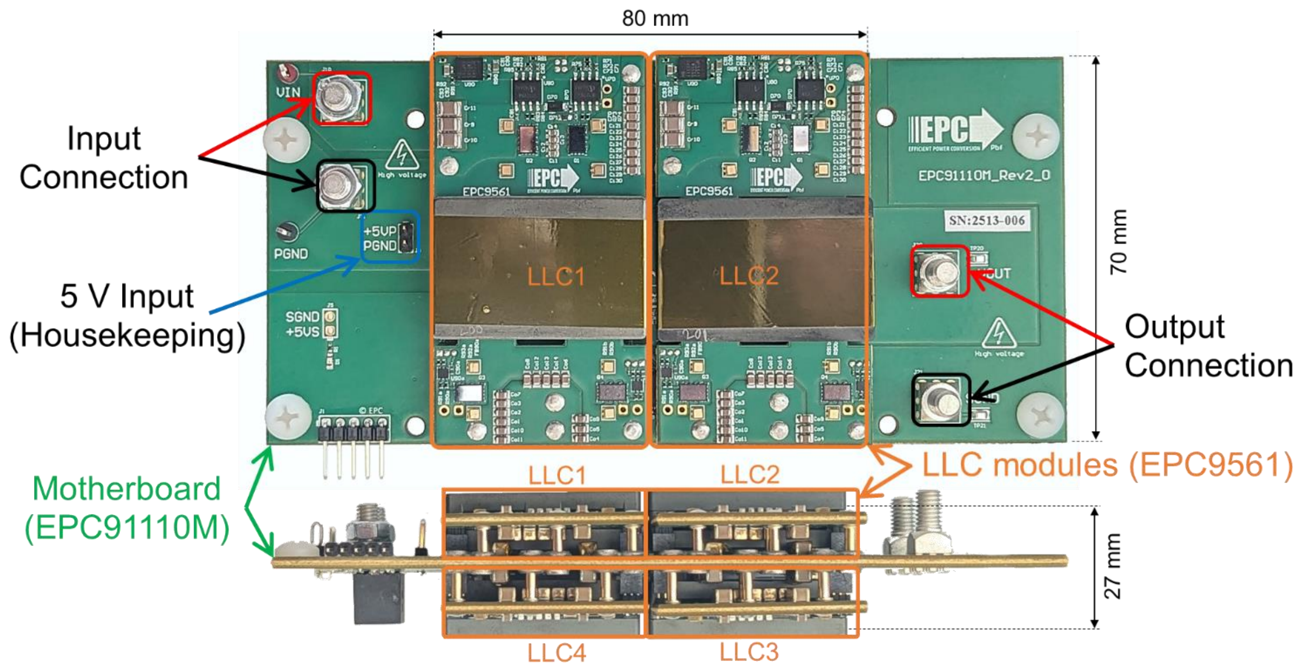

Figure 3: Overciew of the EPC91110KIT with various components highlighted

EPC91110M Motherboard

The motherboard of the converter is sandwiched between the LLC modules providing power and signal connections between the LLC modules to realize the ISOP configuration. It also provides additional input/output ceramic capacitance for each module. The microcontroller, a 16-bit dsPIC33 from Microchip is located on the top side of the board. This microcontroller is packaged in a very compact 48-pin 6x6 mm VQFN, and it has 8 PWM generators with a time resolution of up to 250 ps, which is sufficient to independently control all the FETs in the converter. The controller is referenced to the ground of the secondary side (SGND).

The motherboard also includes a pin header for a 5 V supply to power the gate drivers and microcontroller. This 5 V supply is referenced to the primary side of the converter (PGND), so on the bottom side of the motherboard, an isolated power supply brings the 5 V to the secondary side. Note that this isolated power supply would not be necessary when this isolation converter (the EPC91110KIT) is combined with the PFC stage (the EPC91107KIT) to create a full server power supply.

Finally, the motherboard also provides DC measurements points for input and output voltages as well as intermediate voltages for the input of each LLC module.

All these components are highlighted in Figure 4.

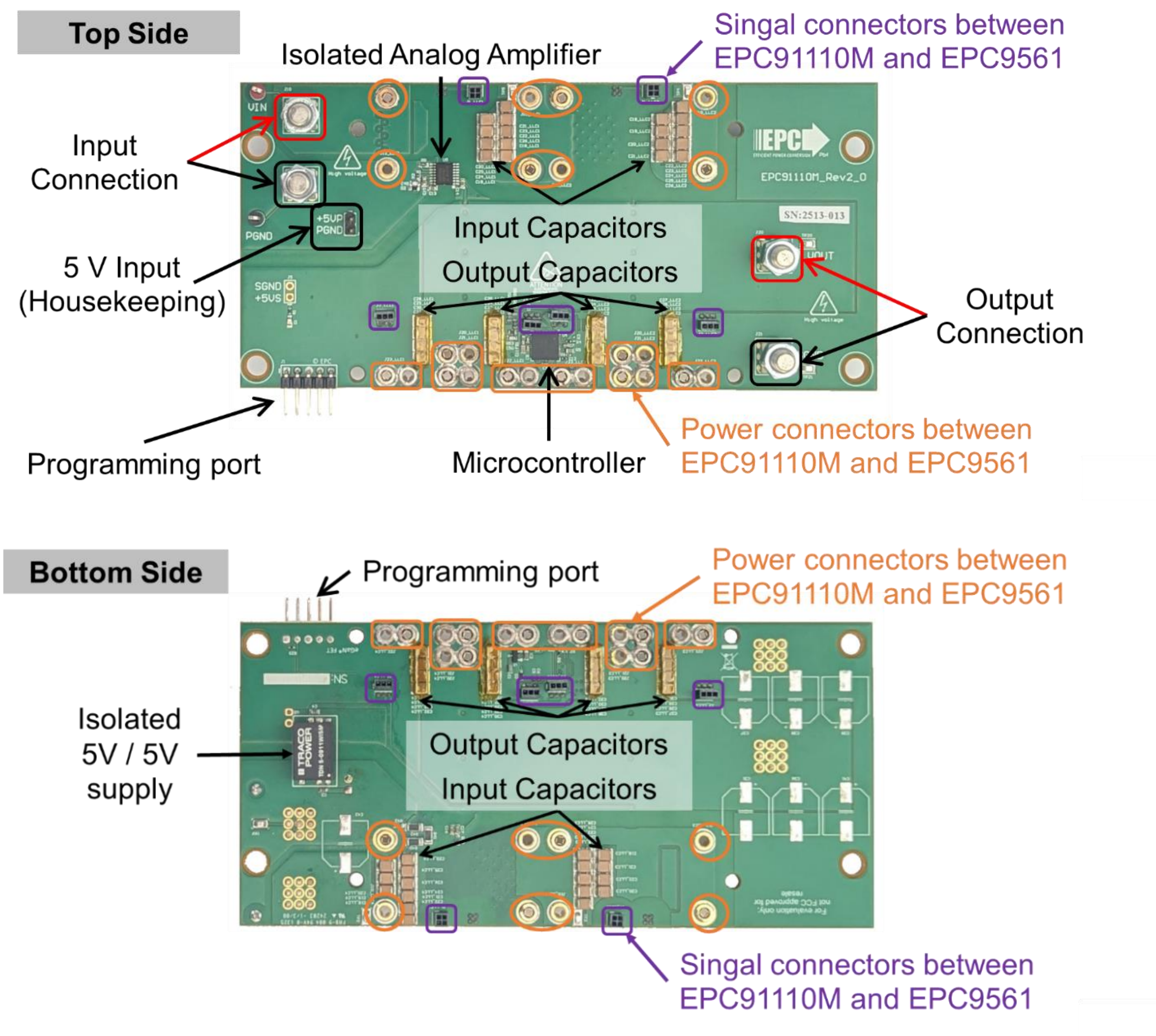

Figure 4: (Top) Photo of the top side of EPC91110M. (Bottom) Photo of the bottom side of EPC91110M.

EPC9561 LLC Module

The EPC91110KIT comprises four EPC9561 boards, one per LLC module. Each EPC9561 board contains all the key components of an LLC converter, thus allowing their operation as a standalone 100 V to 50 V isolated converter. Figure 5 shows photos of the board with the main components highlighted.

The topology used for the LLC converter is based on a half-bridge topology in the primary side of the transformer and a center-tap full-wave rectifier in the secondary, as shown in Figure 2. A total of 4 EPC2305 eGaN FETs are used on each module, two in the primary side controlled by two isolated gate drivers, and two in the secondary controlled by two low-side gate drivers. All the secondary gate drivers are referenced to the secondary side ground (SGND), while the primary gate drivers are referenced to the floating ground of each LLC module (FGND). Because of the ISOP configuration of the converter, only one of the four LLC modules (LLC1 in Figure 2) has FGND at the same level as the input ground (PGND). The other three modules have FGND at ¼, ½, and ¾ of VIN. Therefore, a small 5 V to 5 V isolated power supply is included in each module to level shift the 5 V supply.

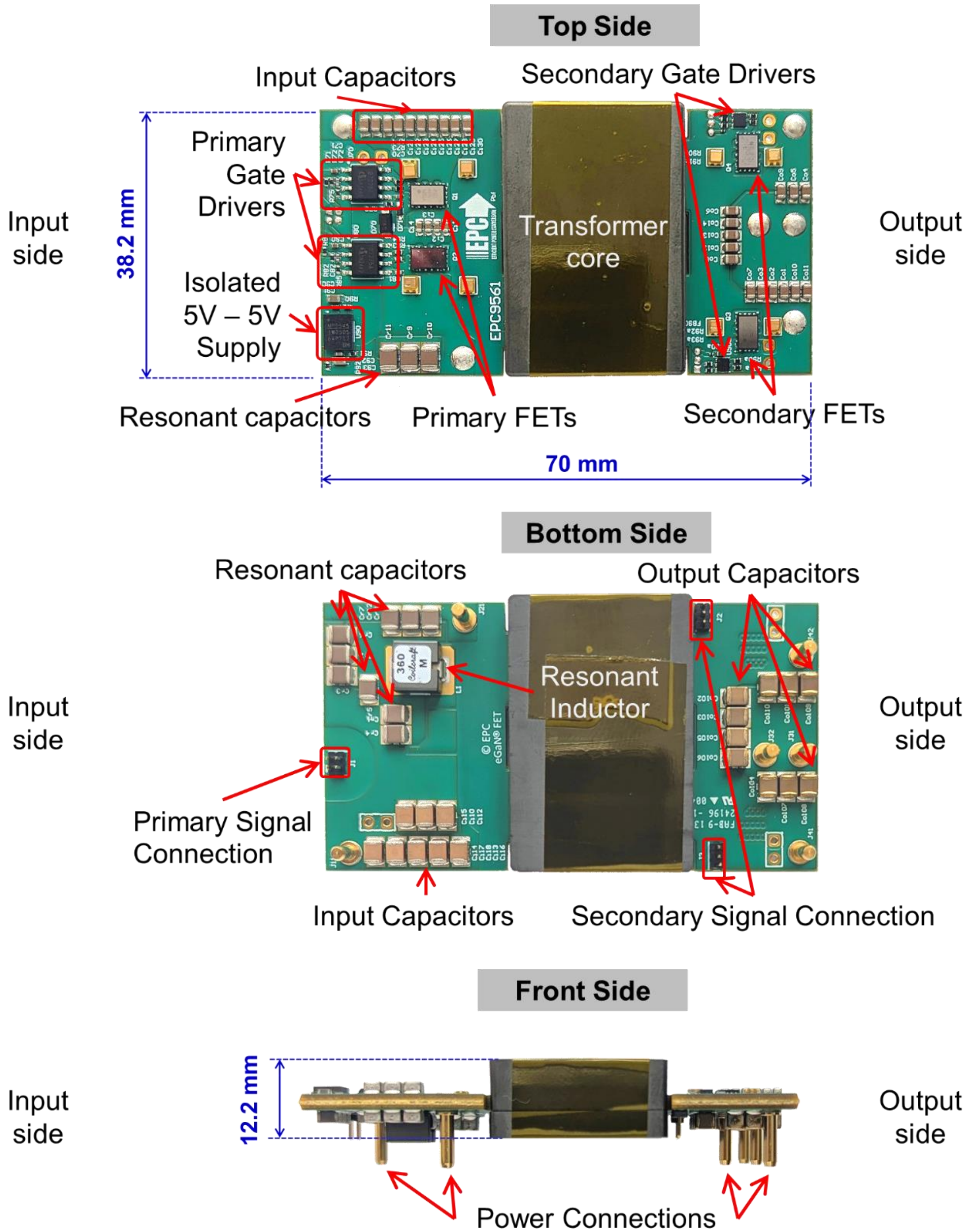

Figure 5: (Top) Photo of the top side of EPC9561. (Center) Photo of the bottom side of EPC9561. (Bottom) Photo of the front side of EPC9561.

The LLC converter uses a planar transformer with its windings built into the PCB. One PCB layer is dedicated to each turn and each winding is paralleled once. So, with a 1:1:1 turns ratio, 6 layers are used for the transformer windings, plus 2 additional layers for components and routing. In total, 8 layers with 2-oz Cu and 2.2 mm of total board thickness. The magnetic core is based on a E + I geometry manufactured by Proterial using its ML95S material. The airgap is set to 100 µm to achieve the desired magnetizing inductance.

The resonant tank is also included in the EPC9561 board. It is designed to have a resonant frequency at approximately 1 MHz, using a total of twelve 200 V-rated, 47 nH and C0G dielectric, in a split configuration. A resonant inductance of approximately 40 nH completes the resonant tank, a combination of the leakage inductance from the transformer and an external 36 nH inductor.

CONNECTIONS

Figure 6 shows the power connections needed to operate the EPC91110KIT. Figure 7 shows the measurement points available on the motherboard to sense the input and output voltages as well as the intermediate input voltages to verify adequate input voltage sharing among LLC modules.

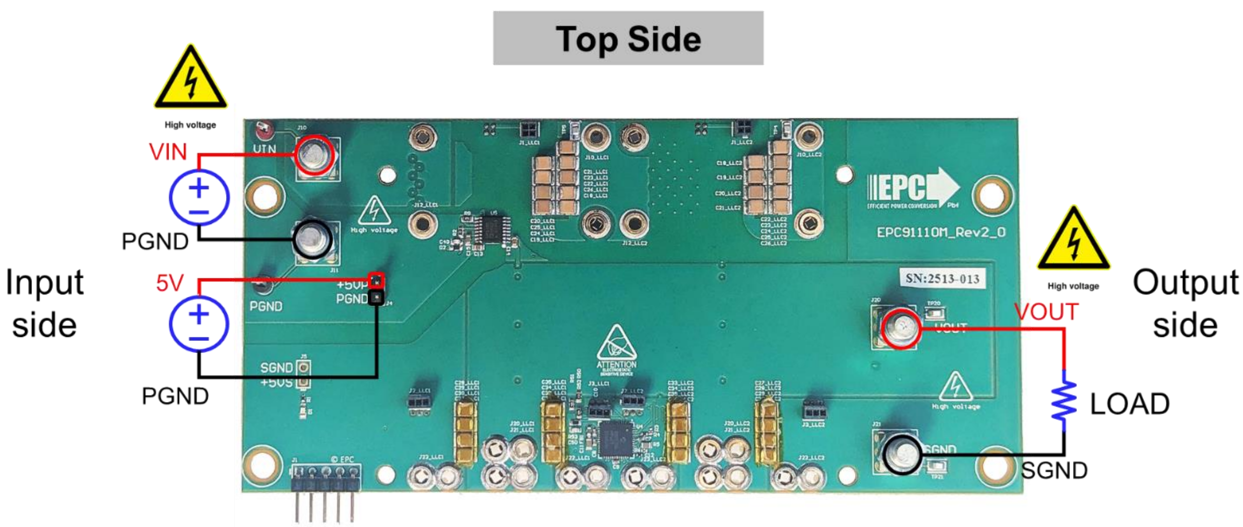

Figure 6: Power connections to the EPC91110KIT.

Figure 8 shows the available probe points to capture the key waveforms within the LLC module. These probe points are available on each EPC9561 board: SN1, the switch-node between the primary FETs; and VDa/VDb, the drains of the rectifier FETs. Note that VDa and VDb are referenced to SGND, common for all LLC modules, while SN1 is referenced to FGND for each module. This means that SN1 for LLC1 is referenced to PGND, whereas SN1 for LLC2, LLC3, and LLC4 are referenced to ¼, ½, ¾ of VIN respectively, all of them isolated from SGND. For this reason, and to prevent damage to the oscilloscope, differential probes are recommended to measure SN1-FGND in LLC1 and required for LLC2, through LLC4.

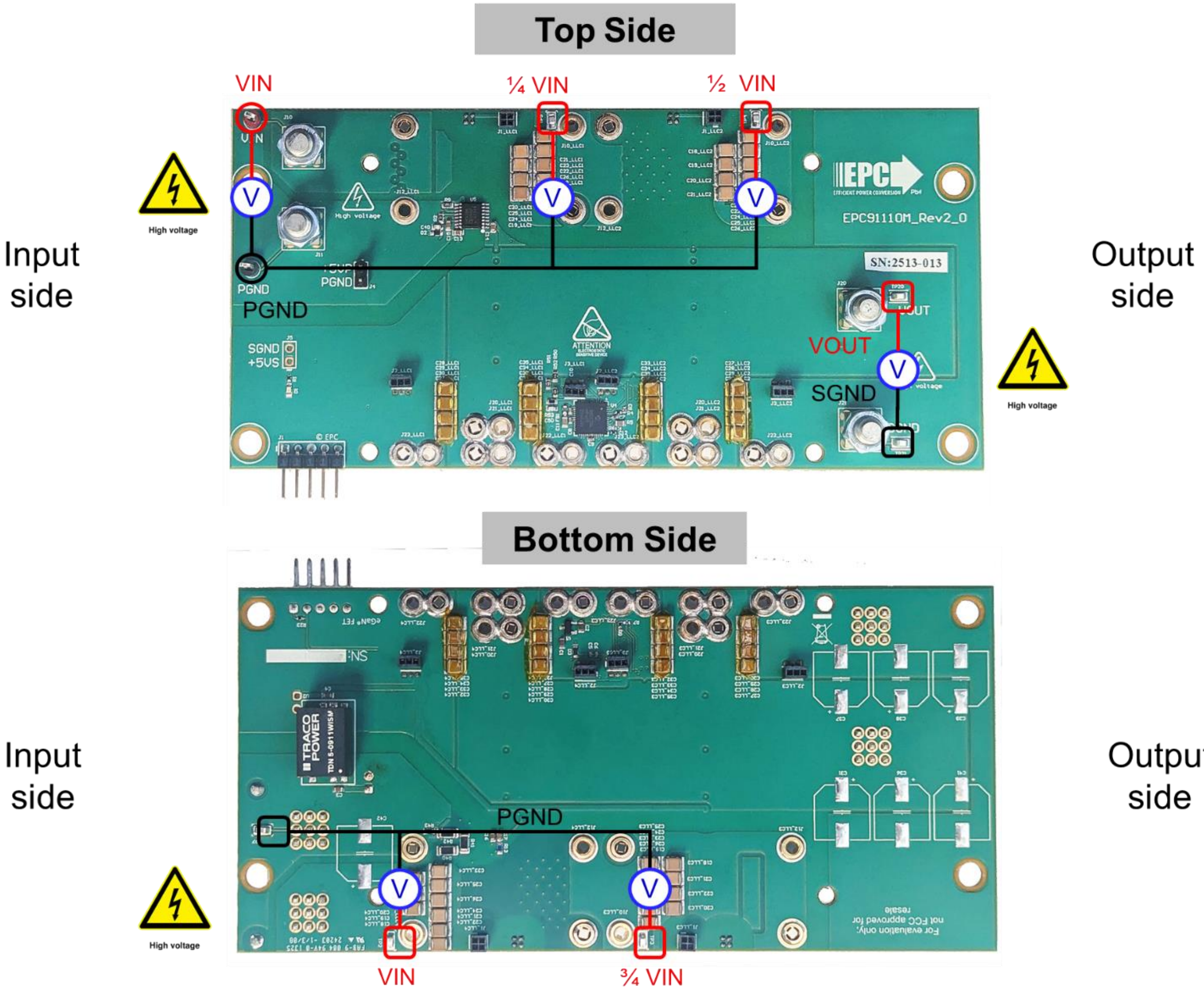

Figure 7: EPC91110KIT hookup locations for DC measurements

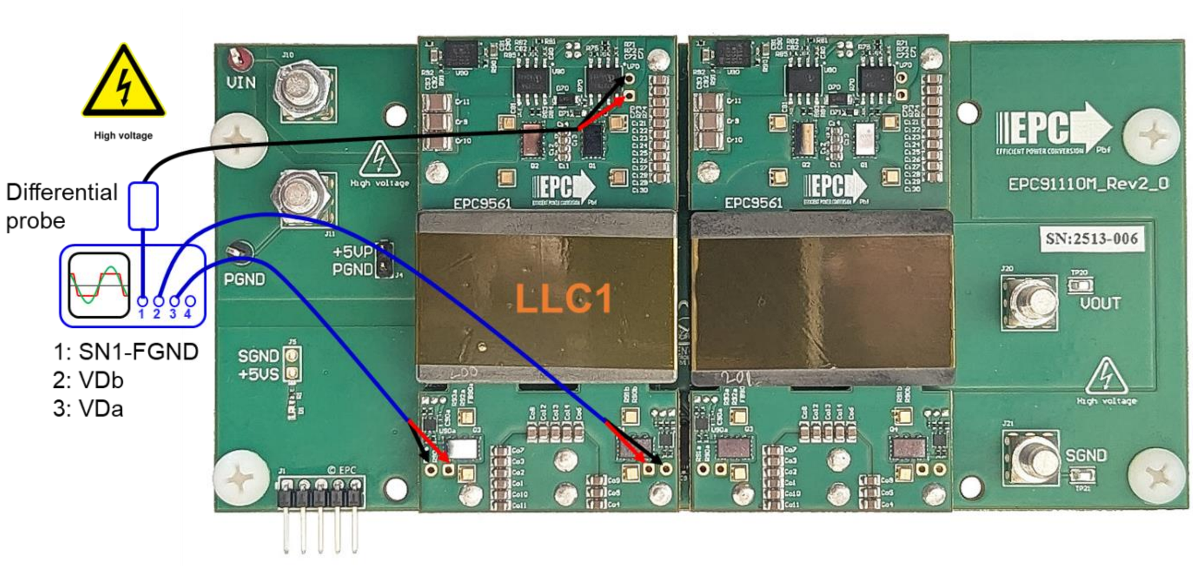

Figure 8: Oscilloscope probe points for waveform measurements

THERMAL CONSIDERATIONS

The EPC91110KIT is not equipped with a heatsink, so caution must be taken when operating at high output power. **It is recommended to use high airflow over the top and bottom surfaces of the KIT while monitoring the FETs' temperature using a thermal camera**. Figure 9 shows the recommended airflow orientation for optimal cooling of the converter.

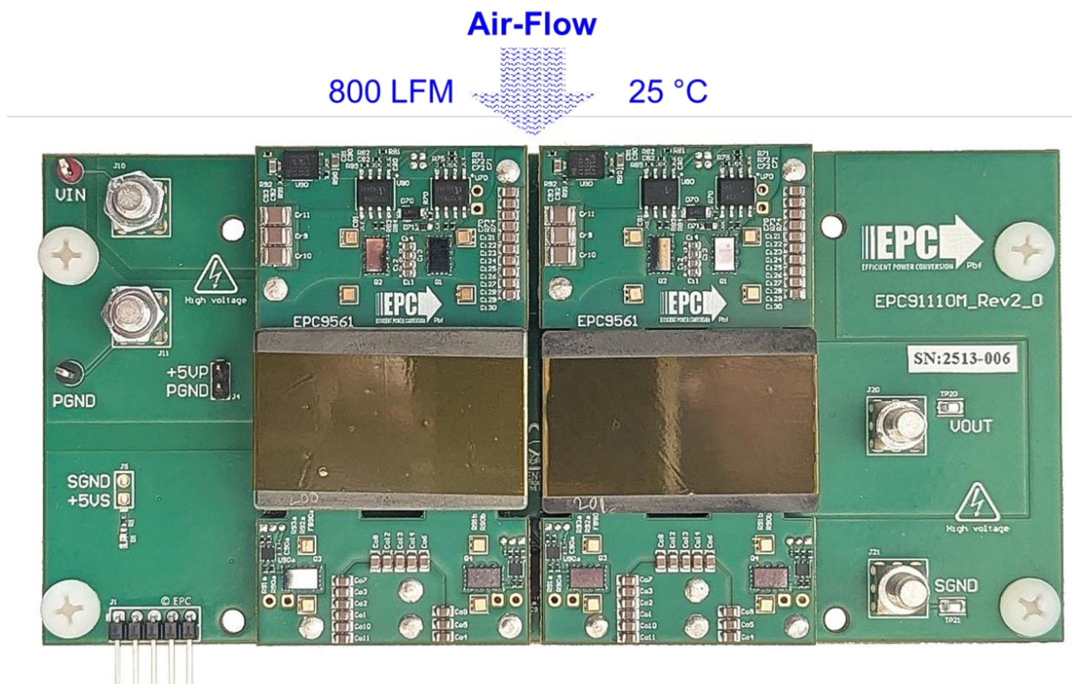

Figure 9: Recommended air-flow orientation for optimal cooling of the converter

The addition of a heatsink can significantly improve the heat dissipation from the GaN FETs by adding cooling from the top side of the device and thus reducing the amount of forced air required to maintain the FET temperatures within the datasheet limits. Figure 10 shows a cross-sectional view of a suitable cooling system for the LLC modules. A 1-mm tall SMD spacer is used to set the correct height for the heat-sink or spreader above the FETs and provide the correct compression for the thermal interface material.

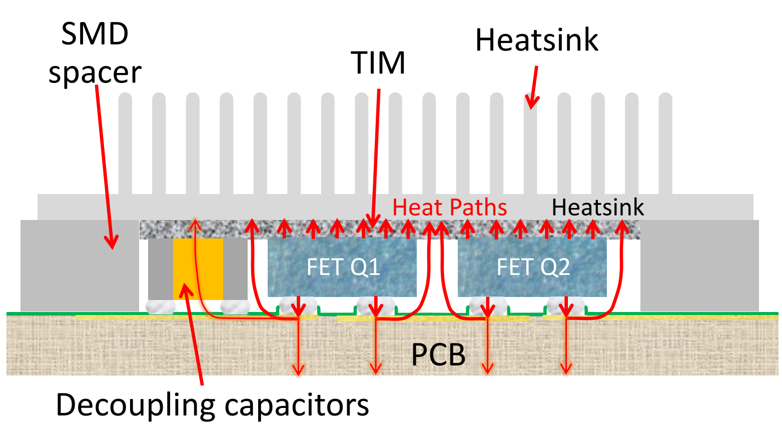

Figure 10: Cross-sectional view of the back-side cooling thermal system.

It is important that the TIM for the eGaN FETs also serves to electrically insulate the back of the GaN FETs from the heatsink. It may be necessary to first place a heat-spreader above the FETs before interfacing to a larger heatsink. In this case, a first TIM is required between the GaN FETs and the heat-spreader and a second TIM is needed between the heat-spreader and the heatsink.

The choice of TIM for the eGaN FETs needs to consider the following characteristics:

Mechanical compliance – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the eGaN FET. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.

Electrical insulation – The backside of the eGaN FET is a silicon substrate that is connected to the Source. Electrical insulation from each GaN FET to the heat-spreader / heatsink is required for the thermal solution.

Thermal performance – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials are preferred to provide higher thermal conductance at the interface.

The thermal requirements for the choice of TIM between the heat-spreader and heatsink can be relaxed due to the larger area which allows the use of lower thermal conductivity materials with negligible impact on thermal performance. To help make up for the lower thermal conductivity, a thinner sheet may be used.

EPC recommends the t-Global Part Number: TG-A1780 for the eGaN FETs TIM as it has a high thermal conductivity of 17.8 W/m·K. For the heat-spreader TIM, the t-Global Part Number: TG-A620 with a moderate thermal conductivity of 6.2 W/m·K can be used.

PROGRAMMING

The controller within the EPC91110KIT (dsPIC33CK256MP605-I/M7) is preprogrammed for easy and quick evaluation of the converter. The default firmware operates the LLC modules in open loop with a constant switching frequency that matches the resonant frequency of the LLC modules. All LLC modules operate synchronously and use the same PWM settings.

It is also possible to program the controller with a different firmware via the programming port located on the bottom edge of the motherboard, as shown in Figure 4. Table 2 shows the controller pin map and peripheral resource allocation. Please contact EPC for help.

Table 2: Controller pin map and description

Pin Number	Signal Name (SCH)	Description	Type	Range
1	PWM1H	PWM for Q1 – LLC1	Output	0 – 3.3 V
2	PWM1L	PWM for Q2 – LLC1	Output	0 – 3.3 V
3	PWM8H	PWM for Q3– LLC4	Output	0 – 3.3 V
4	PWM8L	PWM for Q4 – LLC4	Output	0 – 3.3 V
5	MCLR	Master Clear	Input/Power	0 – 3.3 V
10	400V_sns	Input Voltage Sense	Input	0 – 3.3 V
11	VOUT_sns	Output Voltage Sense	Input	0 – 3.3 V
13	AVDD	Positive Supply for Analog Modules	Power	0 – 3.3 V
14,19,31,42,49	SGND	Secondary Ground	Input	0 – 3.3 V
18	3V3S	Positive Supply	Power	0 – 3.3 V
26	PGD	Data I/O for programming	Input/Output	0 – 3.3 V
27	PGC	Clock in for programming	Input	0 – 3.3 V
32	3V3S	Positive Supply	Power	0 – 3.3 V
33	PWM6L	PWM for Q4 – LLC3	Output	0 – 3.3 V
34	PWM6H	PWM for Q3 – LLC3	Output	0 – 3.3 V
35	PWM4L	PWM for Q4 – LLC2	Output	0 – 3.3 V
36	PWM4H	PWM for Q3 – LLC2	Output	0 – 3.3 V
38	PWM5H	PWM for Q1 – LLC3	Output	0 – 3.3 V
39	PWM5L	PWM for Q2 – LLC3	Output	0 – 3.3 V
40	PWM7H	PWM for Q1 – LLC4	Output	0 – 3.3 V
41	PWM7L	PWM for Q2 – LLC4	Output	0 – 3.3 V
43	3V3S	Positive Supply	Power	0 – 3.3 V
45	PWM3H	PWM for Q1 – LLC2	Output	0 – 3.3 V
46	PWM3L	PWM for Q2 – LLC2	Output	0 – 3.3 V
47	PWM2H	PWM for Q3 – LLC1	Output	0 – 3.3 V
48	PWM2L	PWM for Q4 – LLC1	Output	0 – 3.3 V

QUICK START PROCEDURE

1) Install the standoffs provided with the KIT.
2) Connect the housekeeping power supply to 5V/PGND as shown in Figure 6. It is recommended to use a power supply of at least 2 A, even though the current consumption should be lower, between 700-800 mA.
3) Connect the load to VOUT/SGND as shown in Figure 6. Set the load to 0 A.
4) Connect the input supply to VIN/PGND as shown in Figure 6.
5) Place a high airflow fan (~800 LFM or more) as shown in Figure 9.
6) Turn-on the housekeeping supply – this will startup the controller and power supplies on the LLC modules. Current consumption should be approximately 700-800 mA.
7) Turn-on the input supply and gradually increase the voltage. The output voltage will also increase proportionally (VOUT = VIN / 8). Make sure the input supply remains below the maximum value listed in Table 1.
8) Once the input voltage is set to the desired value, gradually increase the load. Make sure to remain within the specifications listed in Table 1.
9) After the test is finished, undo the previous steps in reverse (8 → 7 → 6 → 5)
10) For tests different than those described here, please contact EPC.

EXPERIMENTAL VALIDATION

Efficiency and Power Loss Results

Figure 11 shows the efficiency and power loss measurements of the EPC91110KIT operating between a 410 V input bus and a 51 V output load, while processing up to 5.5 kW. Peak efficiency of 98.2% is achieved at 50-70% of the full load, and full load efficiency is approximately 98%.

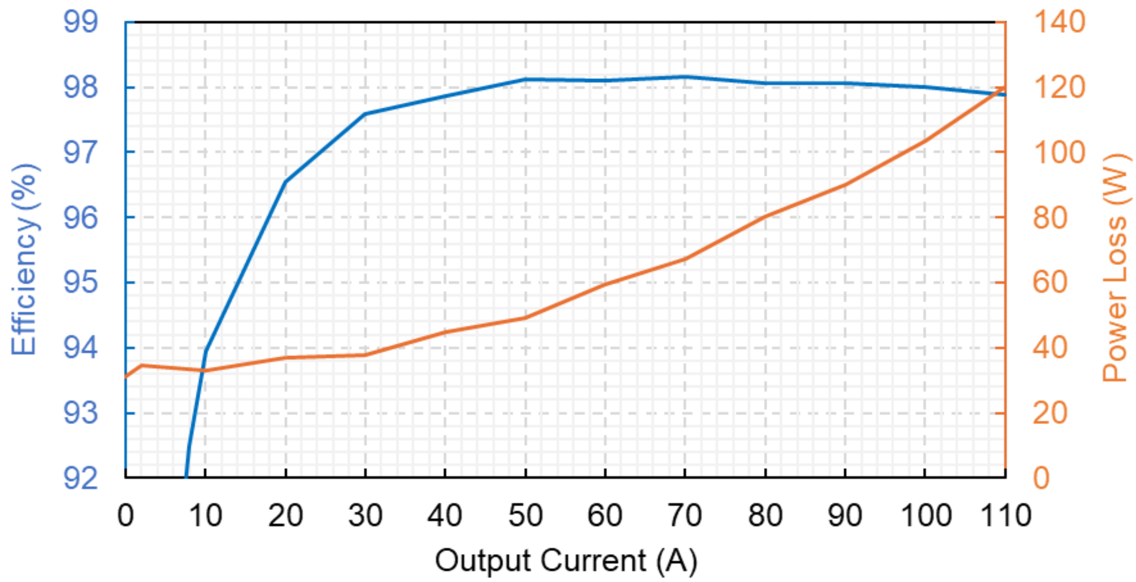

Figure 11: Measured efficiency and power loss curves for the EPC91110KIT delivering up to 5.5 kW into a 51 V load from a 410 V supply.

Waveforms

Waveforms for the key voltages and currents in the converter are shown in Figure 12. Channel 1 shows the PWM signal for the HS FET in the primary (Q1 in Figure 2) coming from the controller. Channel 2 shows the switch-node waveform between Q1 and Q2 in the primary side of the LLC converter. Channel 3 and Channel 4 show the drain voltages of the rectifier FETs on the secondary side of the LLC (Q3 and Q4 in Figure 2). Channel 5 shows the resonant current. Waveforms for two different output powers are overlapped to show the resonant current under load (P_{OUT} = 1225 W), as well as the magnetizing current (P_{OUT} = 0 W).

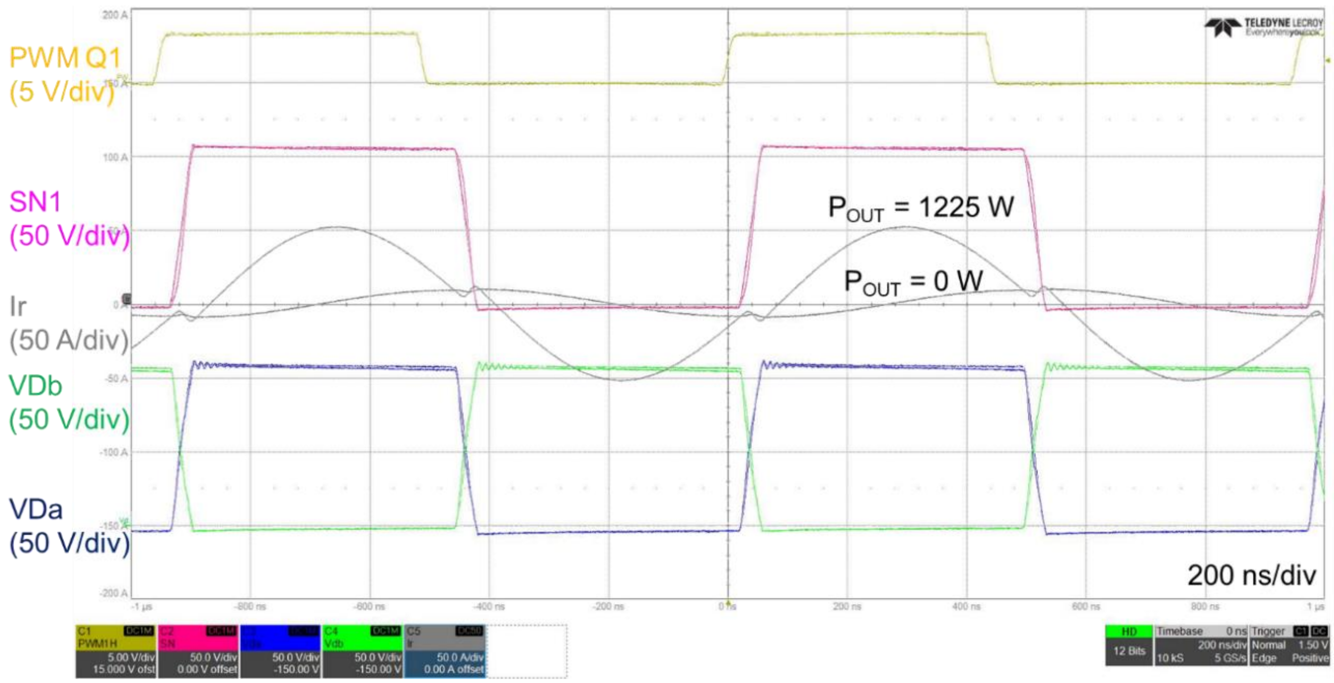

Figure 82: Measured waveforms of one of the LLC modules operating between V_{IN} = 102 V and V_{OUT} = 51 V and two different output powers, P_{OUT} = 0 W and 1225 W.

Input Voltage Sharing

ISOP converters rely on even voltage sharing of the input voltage among all the modules connected in series. Failure to achieve this can result in overvoltage of some of the components, potentially leading to failures. In general, LLC topologies are inherently adequate for ISOP configurations because the same output voltage is applied to all the secondary sides of the transformers. This means that the same voltage is also reflected to the primary side of the transformer. In addition, the resonant tank and the magnetizing inductance of the EPC9561 are designed in such a way that the gain of LLC module is frequency and load independent when operating at or near the resonant frequency (the default operating point). As a result, the EPC91110KIT achieves self-balancing or even input voltage sharing, without the need for a dedicated closed loop control algorithm. This can be observed in Figure 13, where the differential input voltages for all LLC modules within a EPC91110KIT are shown when the converter is operating from a 410 V supply and delivering up to 5.5 kW into a load.

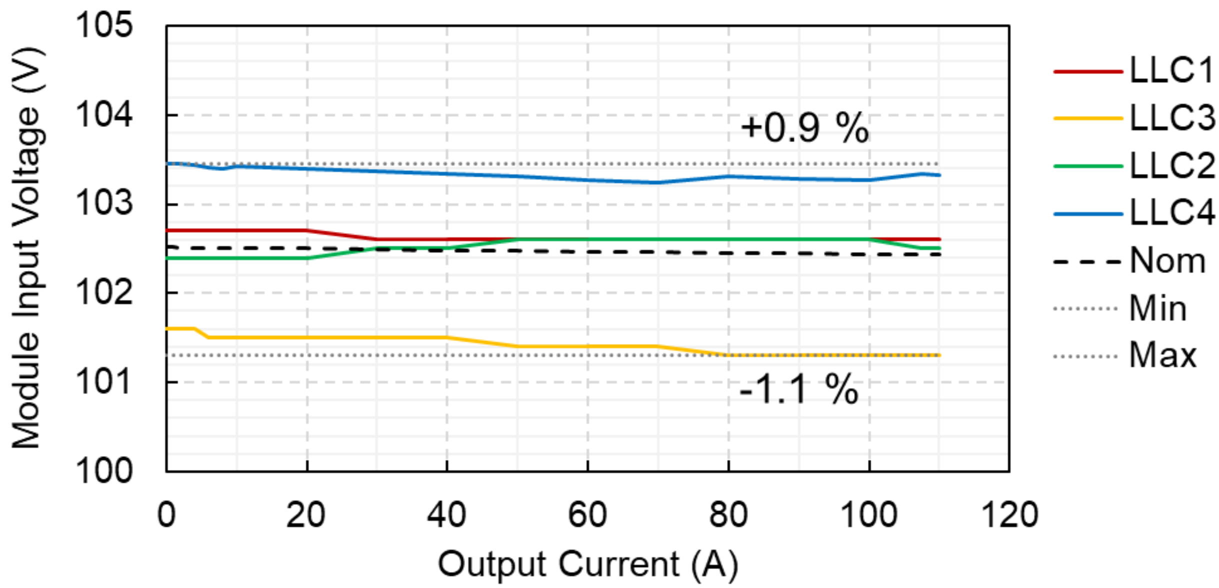

Figure 13: Differential voltages for all EPC9561 modules within a EPC91110KIT while operating from a 410 V supply and delivering up to 5.5 kW into a load.

Thermal Performance

Figure 14 shows the different component temperatures within a EPC9561 module while running continuously at full load with high airflow.

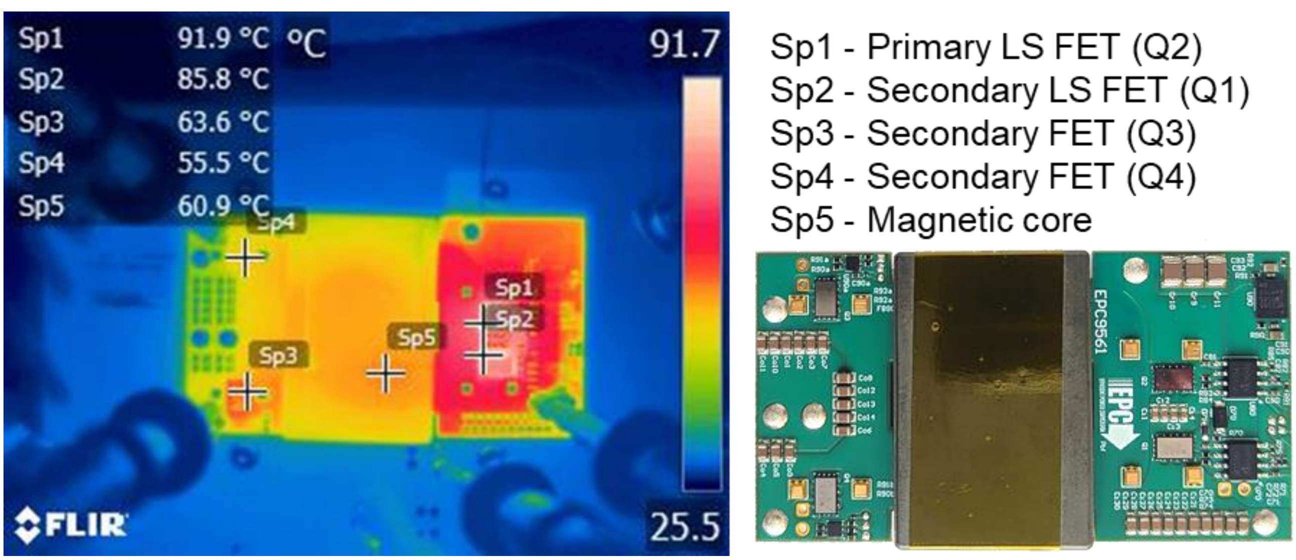

Figure 14: Thermal steady state image of one of the EPC9561 modules without the heatsink kit and high airflow while processing 1250 W into a 51 V load from a 102 V supply.

PRECAUTIONS

The EPC91110KIT is a demonstration board and has not been fully tested to comply with all OCP or other standards. Please contact EPC for advanced tests and to verify if the KIT can pass such tests.

Never operate the EPC91110KIT with a Microchip programmer connected to the unit. If communications to the unit is required during testing, EPC recommends using a USB isolator to prevent damage to the computer should a failure occur.

BOARD VERSIONS AND FIRMWARE

Table 3: EPC91110KIT board number versions

Board Number	EPC91110M	EPC9561
Schematic Revision	2.1	2.1
PCB Revision	2.0	2.0
Firmware	1.0	

DOCUMENT HISTORY

Initial release: 30 June 2025

ACKNOWLEDGEMENTS

Proterial, Ltd.

EPC would like to acknowledge Proterial Ltd. (https://www.proterial.com/e/) for their support with the transformer cores.

EPC would like to acknowledge Microchip Technology Inc. (www.microchip.com) for their support of this project. Microchip Technology Incorporated is a leading provider of smart, connected and secure embedded control solutions. Its easy-to-use development tools and comprehensive product portfolio enable customers to create optimal designs, which reduce risk while lowering total system cost and time to market. The company's solutions serve customers across the industrial, automotive, consumer, aerospace and defense, communications and computing markets. The EPC91110KIT demonstration board features the dsPIC33CK256MP605-I/M7 16-Bit Digital Signal Controller with High-Speed ADC, Op Amps, Comparators and High-Resolution PWM. Learn more at www.microchip.com.

For support files including schematic, Bill of Materials (BOM), and Gerber files please contact an EPC representative.

For More Information:

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Evaluation Board Notification

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