Evaluation Board EPC91116 Quick Start Guide

High Frequency 40 V, 17 A Laser Driver using EPC2203

March 25, 2025

Version 1.0

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC91116 is a demonstration board suitable for driving laser diodes with short current pulses, achieving minimum pulse widths as low as 5 ns. It supports peak currents of more than 10 A, and a bus voltage of 40 V. This high-speed performance is enabled by EPC's gallium nitride enhancement mode (eGaN®) FET technology. The board utilizes the fully automotive qualified EPC2203, an ultrafast eGaN transistor with a very low total gate charge (Q_G) of 670 pC. The eGaN transistor has a rated pulse current of 17 A, a rated voltage of 80 V, and a very low $R_{DS(ON)}$ of 80 mΩ while maintaining an exceptional small footprint of 0.9 x 0.9 mm. The board is accompanied by the EPC9989 interposer board to provide the user with a simple means of mounting a small set of commercially available lasers. The EPC9989 comprises a collection of breakaway 5 mm square interposer PCBs with footprints for different lasers and various alternative loads. The use of the interposers allows many different lasers or other loads to be mounted on the demonstration boards. The boards do not include a laser diode or load, which must be supplied by the user.

The EPC91116 features a printed circuit board equipped with inputs, outputs, and test points to evaluate and demonstrate the capabilities of both the EPC2203 and performance of the connected load. The printed circuit board is designed to minimize the power loop inductance while maintaining mounting flexibility for the laser diode or other load. It includes multiple on-board passive probes for voltages and is equipped with MMCX connections for input and sensing. The exceptionally low gate charge of the EPC2203 eGaN FET means that it can be driven directly by a low cost CMOS logic bidirectional level shifter, the automotive qualified 74LVC2T45GS-Q100X. While the level shifter's output requires a 5 V supply to drive the EPC2203 GaN FET and 3.3 V for logic families, both voltages can be generated from a 5.25 V-12 V supply using an on-board linear regulator. Alternatively, the linear regulator can be bypassed if 5V supply is readily available.

Table 1: Electrical Specifications (TA = 25°C) EPC91116

Symbol	Parameter	Min	Nom	Max	Units
V_{Logic}	Gate drive and logic supply	5.25		12	V
V_{BUS}	Pulse charging supply	0		40	
V_{IN}	Input voltage range	0		5.5	
t_{PIN}	Input pulse width	5			ns
F_{PIN}	Pulse input frequency (does not account for thermal limitations)	0		100	MHz

Table 1 provides the recommended operating conditions for the EPC91116. These conditions consider the electrical characteristics of the unmodified board and do not take into account thermal limitations, since the latter depend on the load and use case.

LASER SAFETY WARNING: This board is capable of driving laser diodes to generate high power optical pulses. Such pulses are capable of causing **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. Laser diodes may emit infrared (IR) light that is invisible to the user, but which can still cause **PERMANENT VISION DAMAGE AND BLINDNESS** as well as additional injury or property damage. User is fully responsible for following proper laser safety procedures to prevent injury or damage.

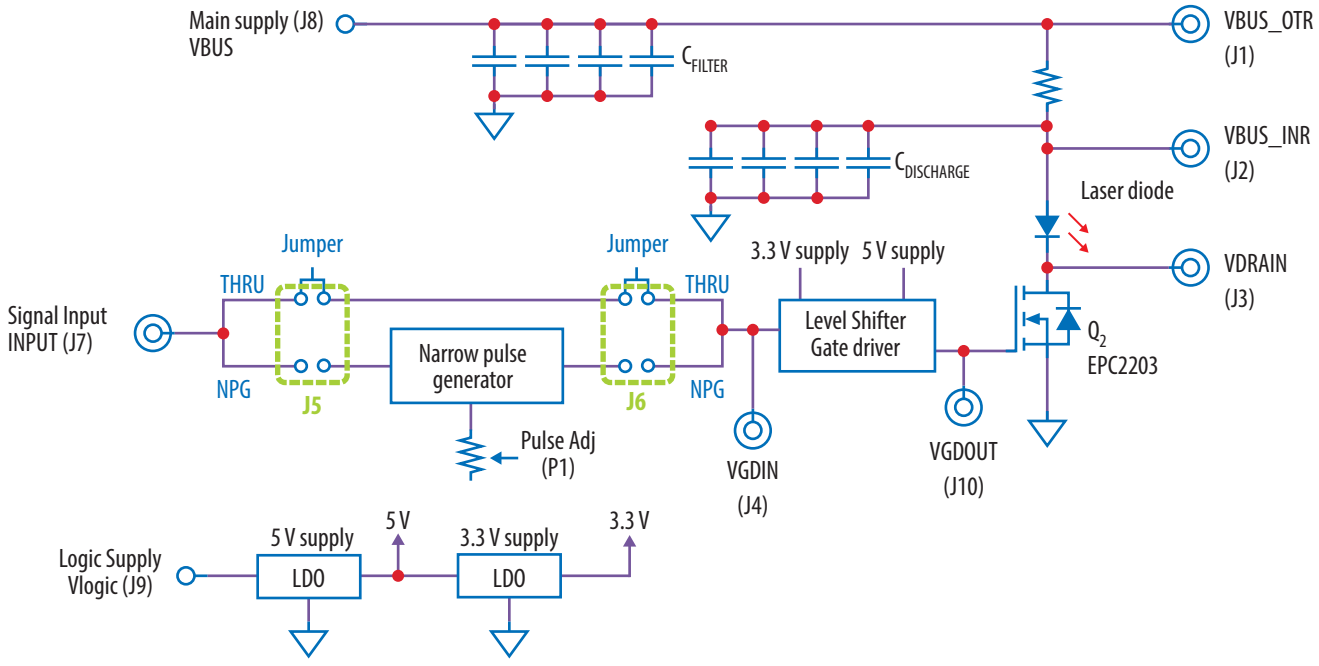

Figure 1. Block diagram of EPC91116 evaluation board

Notably, the signal input (level shifter's input) can accommodate a wide logic voltage range, from as low as 1.2 V to as high as 5.5 V. Furthermore, the board's versatility extends beyond laser diode driving, enabling its application in various circuits requiring a ground-referenced eGaN IC, such as Class E amplifiers, boost converters, and other similar topologies. A complete block diagram of the circuit is illustrated in Figure 1, and a detailed schematic is provided online for comprehensive reference.

More information on the EPC91116 is available from EPC at www.epc-co.com. The full schematics, bill of materials (BOM), and PCB layout files, along with links to information and datasheets on the EPC2203 automotive qualified eGaN FETs can be found at the following links to the demonstration board pages: https://epc-co.com/epc/products/evaluation-boards/epc91116. The datasheets and schematics should be read in conjunction with this quick start guide (QSG). In addition, EPC provides an application note: AN032 Design of High Current Nanosecond Resonant Pulse Drivers for Laser Diodes, Lidar, and other Applications. While the note's discussion of resonant laser drivers is not directly applicable, the layout methods for reducing inductance are applicable to the EPC91116.

MAIN FEATURES

- Fast current pulse generation with nanosecond pulse width
- Integrated high bandwidth measurements for key waveforms
- Optional narrow pulse generator to simplify operation with typical pulse and function generators
- The input pulse can be sourced from wide range of logic family voltage levels

OPERATING PRINCIPLE

The EPC91116 is intended as both a demonstration board and a flexible development platform. It is functional out of the box but is designed to be modified to accommodate a broad range of applications. It is highly recommended that the user read the entire guide in order to get maximum value from the EPC91116. Please refer to the block diagram (Fig. 1) and the schematic online.

The EPC91116 operates as a high-speed pulse generator by driving the EPC2203 eGaN FET with a standard two-channel CMOS level shifter IC. The two channels are connected in parallel to increase the gate drive speed. When a high-level pulse voltage applied to the input of the level shifter (U2), the eGaN FET is turned on, enabling current flow from the bus voltage to the laser diode or other connected load. Conversely, when a low-level applied to the input of U2, eGaN FET turns off, halting current flow to the load. While load characteristics can influence switching speeds, the EPC2203 eGaN FET demonstrates exceptional performance, with turn-on and turn-off times typically faster than 2 ns, for a 10 A load current. The drain voltage of the FET can be measured at MMCX connector J3, which is terminated with a 50 Ω impedance. The input to U2 itself is controlled by an input pulse delivered through MMCX connector J7, also with a 50 Ω input impedance. The input pulse to control U2 can be directly fed from the source (THRU) to U2 or routed through a Narrow Pulse Generator (NPG) circuit. Regardless of the input path, the input impedance at J7 remains approximately 50 Ω.

When using the THRU path, the NPG circuit is bypassed, allowing direct input at J7 to control the level shifter's output and thus the eGaN FET.

The NPG provides convenience for generating extremely short pulses with adjustable widths, providing a cost-effective solution for producing short pulses when a dedicated high frequency pulse generator is unavailable. Detailed operation is described in the "Additional Features (Narrow Pulse Generator)" section.

The voltage bus for the laser diode or other load is bypassed via the capacitor bank (C6, C7, C8, C9). This capacitor bank is part of the main power loop inductance, and the layout is designed to minimize the effect of the resulting parasitic inductance. The capacitor bank is fed through a relatively small resistance formed by R3, R4, R5, and R6. This resistance serves to limit continuous current value of the laser or load in the case of long pulses and also serves to damp parasitic resonance in the power loop. The bus voltage is further filtered via capacitors to minimize any transients appearing at the V_{BUS} (J8) input. Measurements of key waveforms can be made through the provided MMCX test points. These test points can provide waveform measurements with equivalent bandwidths greater than 3 GHz. However, they have requirements and properties that differ from most conventional oscilloscope probes. More details on the usage of these test points are provided in "MEASUREMENT CONSIDERATIONS" section.

LASER DIODE OR LOAD CONSIDERATIONS

The EPC91116 has a set of pads which can be used as is to mount a laser diode or alternative load. Figure 2 highlights the output pad locations. However, many laser suppliers have different mounting footprints, making it difficult to optimize the performance of the driver while still maintaining the desired flexibility. The use of an interposer PCB provides a solution to this problem with only a small impact on performance.

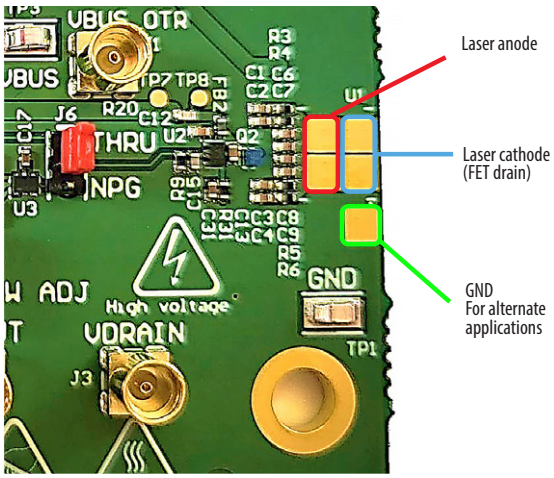

Figure 2. Output terminals of the EPC1116

The EPC91116 ships with the EPC9989 interposer PCB, shown in Figure 3. The EPC9989 has an assortment of 5 mm square interposer PCBs that can be snapped off the board. These interposers have various footprints on the top side that can accommodate several surface mount laser diodes, RF connectors, and several patterns designed to accommodate a wide variety of possible loads. These interposers mount between the EPC91116 and the laser diode or other load.

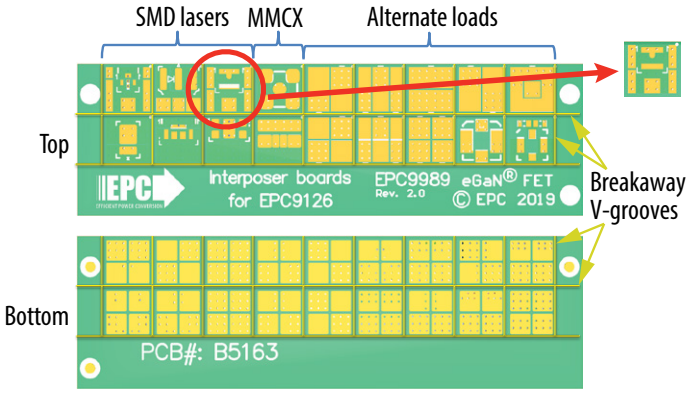

Figure 3. EPC9989 interposer PCB for mounting different lasers and loads

The user should note that it is considerably more difficult to achieve rectangular load current pulses than resonant pulses of equal width because the higher bandwidth of rectangular pulses makes the circuit much more sensitive to parasitic inductance. For best performance, one should choose a laser or load with minimum inductance. Figure 4 shows an example of a laser diode, EGA2000 from ams-OSRAM USA INC., mounted directly to the PCB.

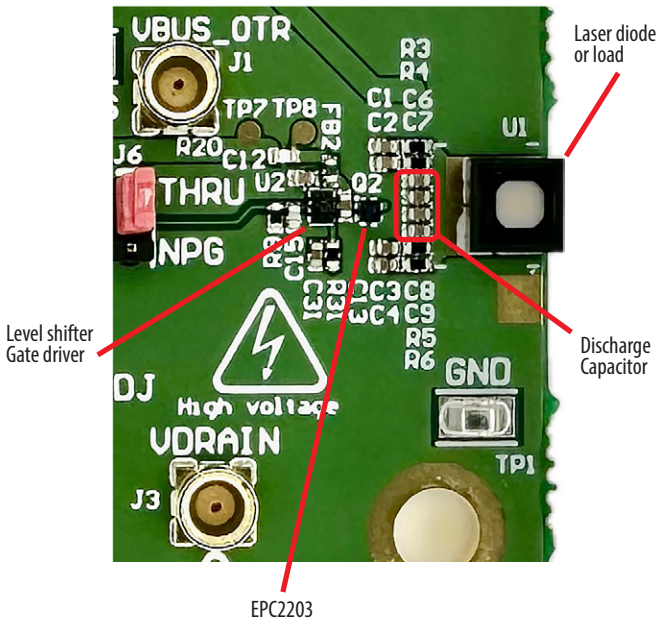

Figure 4. Zoomed-in laser diode driver area with laser diode, EGA2000, mounted

The following procedure can be used to hand mount a laser diode or other load using the interposer:

1. Prepare the EPC91116 by removing the jumpers on J5 and J6 so that they do not deform during reflow soldering. Use best practice to avoid electrostatic discharge (ESD) damage to the laser diode or other load, or to the EPC91116, during the following steps. Laser diodes are often extremely sensitive to ESD damage.
2. Select the interposer with the top side that fits the desired load.
3. Apply solder paste to the appropriate pads on the top side of the interposer.
4. Place the laser diode or desired load on the interposer such that the pads of the load line up with the matching pads on the interposer. Set this assembly gently aside, taking care not to bump it or displace the load since the solder paste is still soft.
5. Apply solder paste to the U1 pads on the EPC91116 PCB.
6. Using tweezers or other means, pick up the assembly of the interposer and laser or alternative load that was set aside in Step 4. Carefully position the assembly with the bottom side of the interposer facing the top side of the EPC91116 on the U1 footprints and set in place.
7. Reflow the EPC91116 together with the interposer-load assembly using the laser or load manufacturer's recommended temperature profile for the selected solder. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user, but it should be noted that many lasers have a polymer optical assembly that is sensitive to overheating.
8. Replace jumpers on J5 and J6.
9. Replace jumpers on J5 and J6.

If the interposer is not used, a modified procedure should be used:

1. Prepare the EPC91116 by removing the jumpers on J5 and J6 so that they do not deform during reflow soldering. Use best practice to avoid electrostatic discharge (ESD) damage to the laser diode or other load, or to the EPC91116, during the following steps. Laser diodes are often extremely sensitive to ESD damage.
2. Apply solder paste to the appropriate U1 pads on the top side of the PCB. If possible, one should cover unused parts of the U1 pads with solder mask to prevent solder from flowing where it is not needed or wanted. A solder mask pen of the type used for PCB repair works well here.
3. Using tweezers or other means, pick up the laser or alternative load. Carefully position the assembly with the bottom side pads of the laser or load facing the top side of the EPC91116 on the U1 footprints so that the pads are aligned and set in place.

4. Reflow the EPC91116 together with the interposer-load assembly using the laser or load manufacturer's recommended temperature profile for the selected solder. The use of a reflow oven that can meet the recommended soldering specifications is highly recommended. Other reflow methods may also be used based on the experience of the user, but it should be noted that many lasers have a polymer optical assembly that may be damaged by overheating.

5. Replace jumpers on J5 and J6.

The power loop inductance, including that of the laser diode, is a primary factor that determines the shape of the laser pulse. Considerable effort has been made to minimize power loop inductance while maximizing the choice of laser diode and its orientation. Maxwell's Laws dictate that the discharge capacitors and the eGaN FET must all be mounted in close proximity to the laser or load to minimize inductance. The resulting proximity of all these components to the laser or other load means that the user must take extra care not to damage any components when mounting the laser or changing other components in the power loop.

The schematic and layout files for the EPC9989 interposer can be found on the main information pages for the EPC91116. In addition, a PCB footprint is available so that the user may design their own custom interposer.

Laser diode current pulses can result in peak optical powers of tens of watts. Laser diodes for lidar applications are designed with this in mind, but thermal limitations of the laser package mean that pulse widths, duty cycles, and pulse repetition frequency limitations must be observed. Read laser diode data sheets carefully and follow any manufacturers' recommendations.

Measurement Considerations

SMA jacks are provided to measure key signals in the circuit, including level shifter input (J4), Q2 drain voltage (J3), bus voltage (J1) and bus capacitor voltage (J2) (see Table 2). All measurement points are designed to be terminated in 50 Ω; hence, when viewing waveforms, the oscilloscope inputs should be set to a 50 Ω input. Ideally, unused outputs should be also terminated with a 50 Ω load to prevent the probes from creating additional resonances. While the reflection coefficient at these 50 Ω termination measurement points is small, and resulting resonances are typically small if left unterminated, users should verify this for their specific requirements.

All sense measurement SMA connectors use the transmission line voltage probe principle to obtain waveform fidelity at sub-nanosecond time scales. They have been verified to produce near-identical results to a Tektronix P9158 3 GHz transmission line probe. As a result of their design, they have a built-in attenuation factor. These factors are given in Table 2. The impedance of the probes at the measurement node is relatively small (~1 kΩ). To minimize the effects of the low probe impedance on the operation of the demo board and prevent overheating of the probe input resistors, the output voltage (J3) and capacitor voltage (J1) probes have DC blocking capacitors on the PCB. As a result, measured pulse waveforms will not have any DC component and will exhibit droop as pulse widths and other waveform features approach the RC time constant of the probe. The user should keep these factors in mind if accustomed to more conventional oscilloscope probes. If long pulse widths are used, the droop will become substantial, and an external probe may be used to measure these slower waveforms more accurately.

Table 2: Key properties of SMA measurement outputs

Designator	PCB label	Description	Attenuation factor	PCB propagation delay (calculated)	DC blocking cap	DC blocking LF time constant	On-PCB termination
J1	VBUS_OTR	Bus Voltage	41 V/V	82 ps	100 nF	10 µs	YES
J2	VBUS_INR	Bus capacitor voltage (VCHARGE on schematic)	41 V/V	110 ps	100 nF	10 µs	YES
J3	VDRAIN	Q2 drain voltage	41 V/V	127 ps	100 nF	10 µs	YES
J4	VGDIN	U2 input voltage	20 V/V	177 ps	none	n/a	NO
J10	VGDOUT	Q2 gate voltage/ U2 output voltage	20 V/V	168 ps	none	n/a	NO

QUICK START PROCEDURE

The EPC91116 demonstration board is simple to set up for evaluation of the performance of the EPC2203 eGaN FETs.

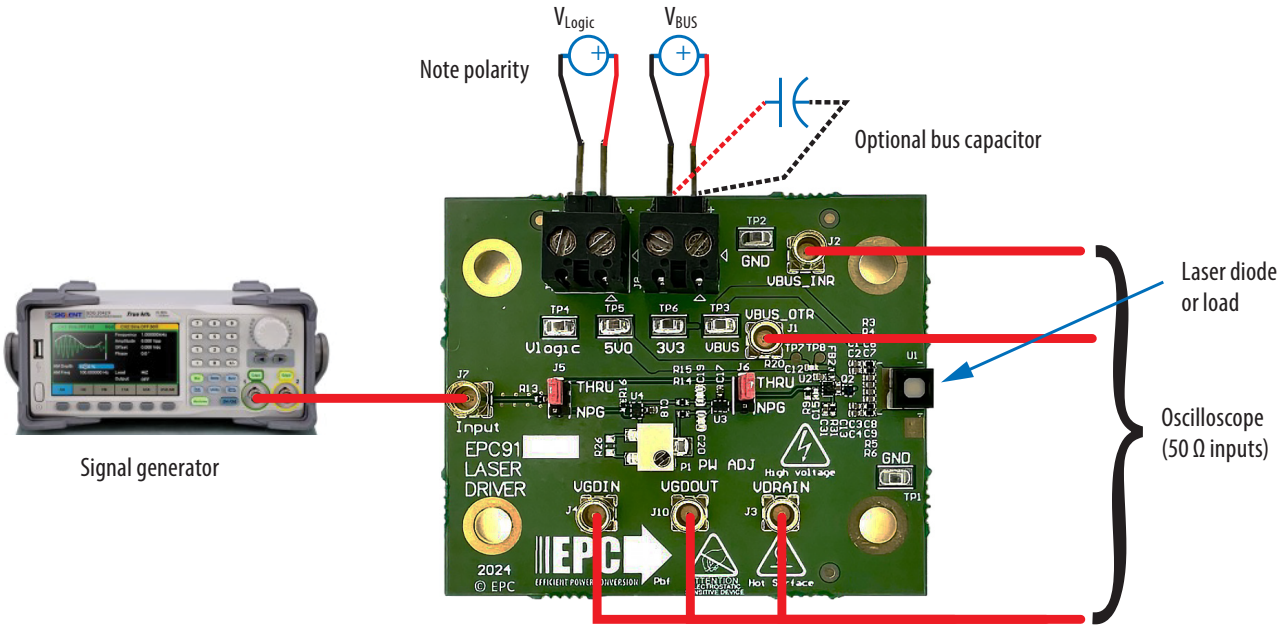

Figure 5. Connection and measurement setup

The procedure in this section provides basic instructions to operate the boards in the default (as shipped) configuration. Refer to Figure 5 for proper connection and measurement setup and follow the procedure below:

1. **Review laser safety considerations when using a laser load. Observe all necessary laser safety requirements including the use of personal protection equipment (PPE) as required. Review high voltage safety considerations since the demonstration boards may operate with voltage levels that may present a safety hazard. Refer to qualified safety personnel as necessary.**
2. With power off, install laser diode U1 or alternative suitable load. The use of one of the interposers from the included EPC9989 can be used to mount the laser or alternative load. This is discussed in the section **LASER DIODE OR LOAD CONSIDERATIONS**.
3. With power off, connect the main power supply to V_{BUS} (J8), taking care to observe the correct polarity. Note that under certain conditions, e.g. bursts of high frequency pulse trains, some combinations of power supply and cabling may cause transients on V_{BUS}. This can be mitigated with the addition of an electrolytic capacitor at the V_{BUS} terminals on the PCB. A recommended starting point is 330 µF (see Fig. 5).
4. With power off, connect the logic supply (5.25-12 V_{DC}) V_{Logic} (J7), taking care to observe the correct polarity.
5. With power off, connect the signal pulse generator to the signal input (J7). J7 is terminated with 50 Ω and is designed for a 1.2-5.5 V logic input. Ensure that the pulse repetition frequency is within the recommended range.
6. Connect the remaining measurement SMA outputs to an oscilloscope, using 50 Ω cables and with the scope inputs set to 50 Ω impedance. See section **MEASUREMENT CONSIDERATIONS** for more information, including the attenuation values for each output.
7. Verify that the logic supply voltage is set to a value within the specifications and turn on the logic supply voltage.
8. Verify that the bus supply voltage is set to a value within the specifications and turn on the bus supply voltage.
9. Turn on the pulse source and observe switching operation via the outputs and any additional desired probing. Laser diode output may be observed with an appropriate opto-electronic receiver.
10. Once operational, adjust the bus voltage, input pulse width, and pulse repletion frequency (PRF) as desired within the operating range and observe the system behavior.
11. For shutdown, please follow steps in reverse.

ADDITIONAL FEATURES

The EPC91116 is designed to accommodate a range of use scenarios. Some of these are available with no modifications to the PCB. The locations of key adjustments are indicated in Figure 6. Advanced features require the ability to remove and replace SMT chip components. It is recommended that these are done by qualified personnel with experience in SMT rework. When reading this section, please have the full schematic available for reference.

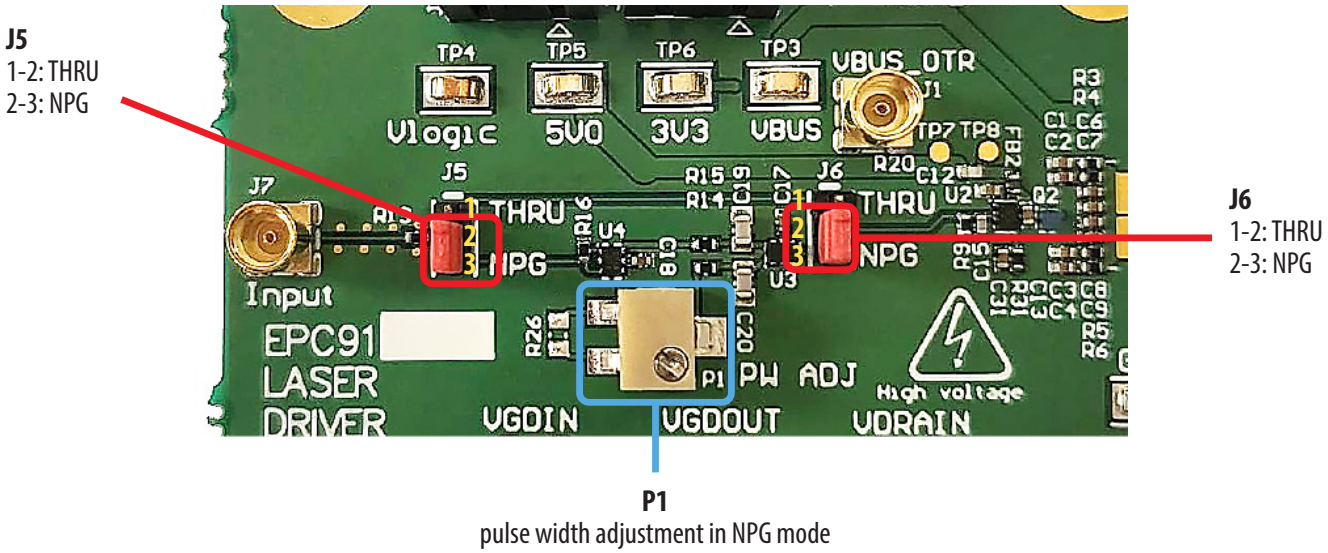

Figure 6. Jumper settings to enable or disable NPG mode

NARROW PULSE GENERATOR

Many signal generators cannot produce an accurate short pulse with sub-nanosecond edges. The EPC91116 incorporates a Narrow Pulse Generator (NPG) function to overcome this limitation. This feature allows for the generation of narrow output pulses with adjustable widths. The NPG is enabled by positioning the jumper on J5 and J6 onto pins 2-3 (refer to Figure 6). When the NPG is enabled, the input pulse signal is divided into two separate paths, each passing through a dual input/output buffer. Please refer to the short pulse generator schematic.

• Path 1: The signal travels through buffer input, then through a fixed RC delay circuit (R15, C19), and finally to one input of a logic gate (U3).

• Path 2: The signal travels through buffer input, then through an adjustable RC delay circuit (P1, R14, C20), and finally to the other inverted input of the logic gate (U3).

The longer delay of the second path means that after some interval, the inverted input of U3 goes high. When this occurs, the output of U3 goes low, triggering the gate driver U2 to transition to a low state. This, in turn, switches off transistor Q2, effectively terminating the output pulse. By adjusting the delay within the second path (through adjustment of potentiometer P1), precise control over the output pulse width of the gate drive is achieved. An increase in the second path's delay translates to a wider output pulse. Clockwise rotation of P1 increases the delay, leading to a wider input pulse applied to the gate of Q2. It is recommended to use a non-conductive tool to adjust P1 due to the sensitivity of the adjustment to stray capacitance.

Note that the minimum delay setting causes both turn-on and turn-off paths to have an approximately equal delay, which would result in a zero-width pulse. The minimum attainable pulse width that results in reliable peak gate voltage is around 5 ns. The maximum pulse width that can be obtained with the NPG is approximately 60 ns, so if longer pulses are needed, the NPG should be disabled. When using the NPG, it is recommended that the input pulse should be at least 10 ns longer than the desired output pulse to guarantee reliable operation under all ambient conditions.

ADVANCED FEATURES

As shipped, the EPC91116 expects 3.3 V LVCMOS inputs. However, the gate drive U2 also has a logic level translator capable of accepting input LVCMOS levels from 1.2 to 5.5 V. The EPC91116 is designed so that a simple modification allows the user to access this capability. This is done by removing R18, which disconnects the 3.3 V supply to U2 and the short pulse generator. These can now be powered using an external supply connected to TP6 and GND.

Note that the maximum operating frequency of U2 will decrease as the supply voltage decreases. The user should consult the manufacturer's data sheet of U2 for details.

IMPROVED LASER COOLING

Some pulse laser applications are thermally limited by laser power dissipation. Usually, the laser die substrate forms the cathode, which is attached to the drain of Q2. Since this terminal is the most electrically active terminal in the whole circuit, it must be kept small and electrically isolated from anything else in the circuit. This makes it difficult for heat to flow out of the laser. This terminal is connected to a small copper land on the bottom of the PCB with a thermally conductive via array. Hence, the thermal resistance from the laser cathode to the bottom thermally conductive ground plane of the PCB can be reduced by populating R27, R28, R29, and R30. The high electrical resistance of these parts means they have negligible electrical effect, but the thermal resistance of the chip resistors is much lower than the PCB substrate. Note that thermal performance can be further improved with the use of thermal bridges, which are essentially a blank resistor chip made with an aluminum nitride body for enhanced thermal performance.

PERFORMANCE EXAMPLES

The following figures show typical performance with resistive loads and laser load. The resistor loads are constructed with four 1% 0603 thick film resistors in parallel, soldered directly across the load mounting pads. The resistors are mounting upside down, i.e. the resistive element is adjacent to the PCB top surface as shown in Figure 7 This reduces the current loop areas and thus minimizes inductance. Load resistors of 1.2 Ω and 2.2 Ω were selected to demonstrate the pulse and burst waveforms in figure 8-11. The 1.2-Ω resistor was created by connecting four 4.6 Ω resistors in parallel, while the 2.2-Ω resistor was formed by connecting four 8.6 Ω resistors in parallel. A 20-cycle burst pulse with a 5 ns width at 25 MHz was applied to the signal input.

The laser load is an ams OSRAM EGA2000-940-W VCSEL. It is selected based on availability and because it can be mounted directly to the PCB with no interposer (see Figure 5). This allows one to minimize the power loop inductance.

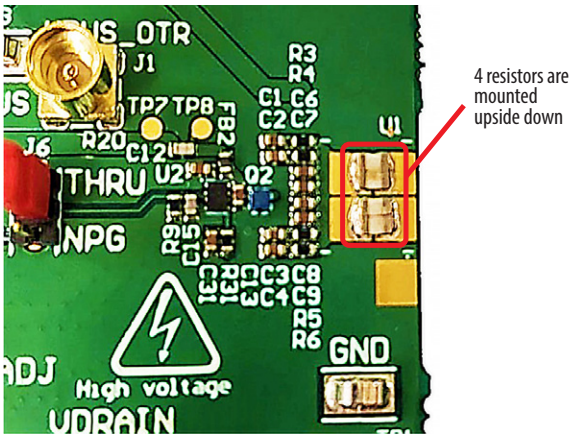

Figure 7. Load resistor placement for resistive load testing. Four parallel 0603 resistors are mounted upside down (resistive element adjacent to PCB) to minimize power loop inductance.

5 V Bus Supply, 1.2 Ω Load Resistor

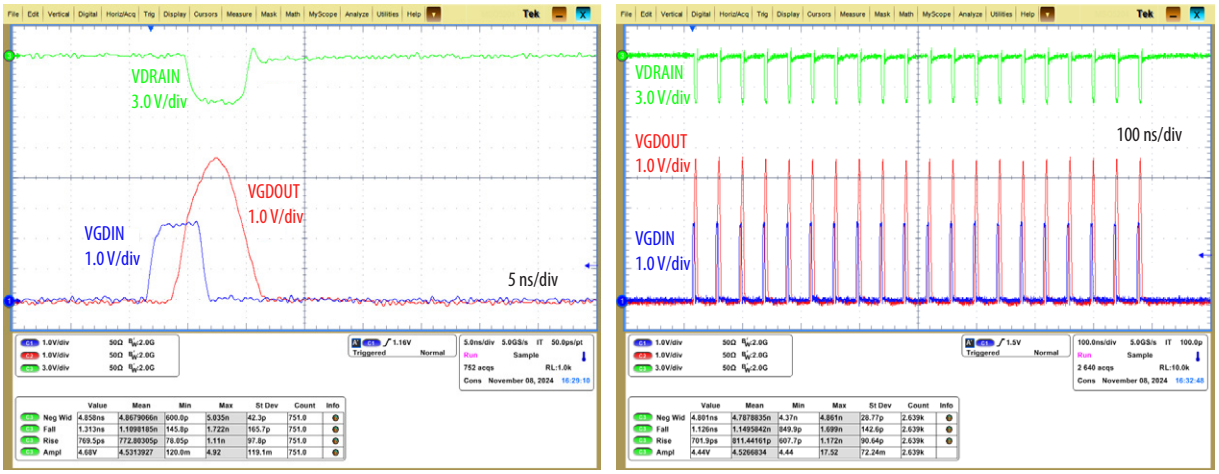

Figure 8. Resistive load waveforms for a single pulse (left) and a 20-cycle burst at 25 MHz waveform (right), both operating at 5 V_{BUS} supply and 1.2 Ω load resistance.

10 V Bus Supply, 1.2 Ω Load Resistors

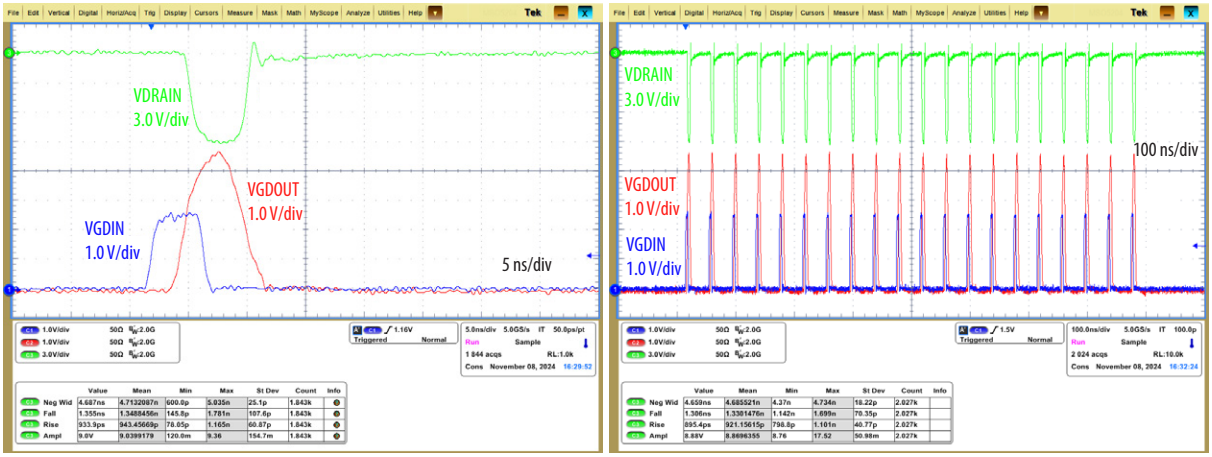

Figure 9. Resistive load waveforms for a single pulse (left) and a 20-cycle burst at 25 MHz waveform (right), both operating at 10 V_{BUS} supply and 1.2 Ω load resistance.

10 V Bus Supply, 2.2 Ω Load Resistors

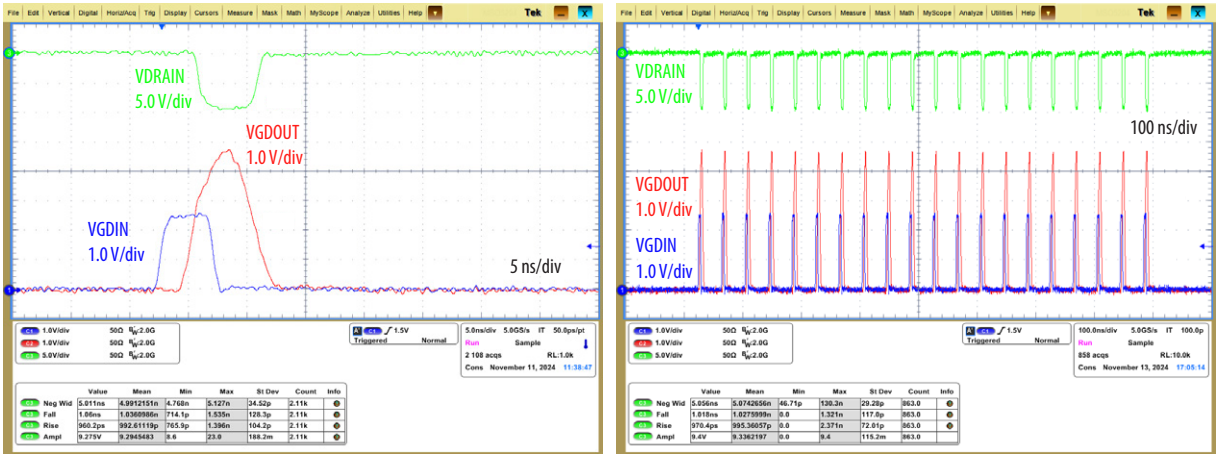

Figure 10. Resistive load waveforms for a single pulse (left) and a 20-cycle burst at 25 MHz waveform (right), both operating at 10 V_{BUS} supply and 2.2 Ω load resistance.

20 V Bus Supply, 2.2 Ω Load Resistors

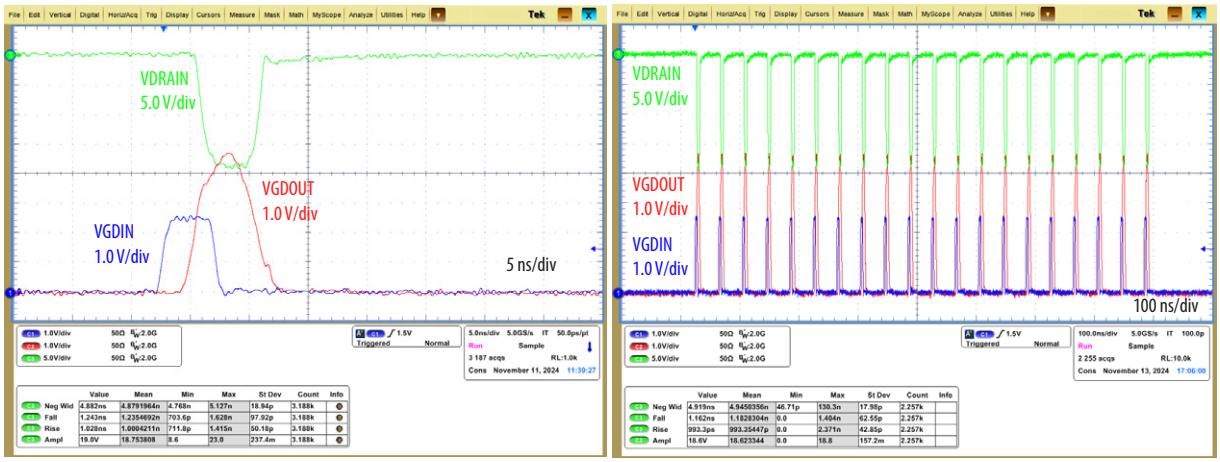

Figure 11. Resistive load waveforms for a single pulse (left) and a 20-cycle burst at 25 MHz waveform (right), both operating at 20 V_{BUS} supply and 2.2 Ω load resistance.

Laser

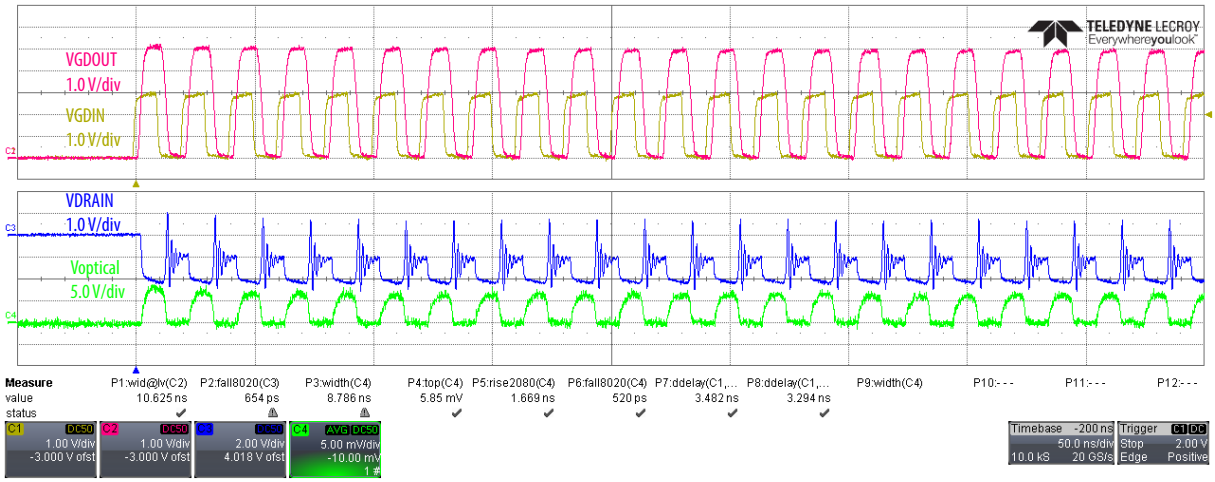

Figure 12 shows waveforms from the beginning of a 1000-cycle, 50 MHz burst at at a burst repetition frequency of 100 Hz waveform, driving a laser load. The laser supply voltage is V_{BUS} = 5 V and and the laser is an ams OSRAM EGA2000-940-W VCSEL mounted directly to the EPC91116 (without interposer).

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC91116 landing page at: https://epc-co.com/epc/products/evaluation-boards/EPC91116

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