EPC91108

High Power Density, Synchronous Buck Converter Quick Start Guide

Featuring the EPC2055 eGaN® FET and LTC7891 Controller

Revision 1.1

EFFICIENT POWER CONVERSION

DESCRIPTION

The EPC91108 is a half bridge buck configuration evaluation board with onboard controller, featuring the 40 V rated EPC2055 GaN field effect transistor (FET). The EPC91108 measures 61 x 61 mm that operates at 800 kHz with an input voltage range from 20 V through 32 V and can deliver up to 252 W power output into a 12 V load. A block diagram overview of the functional blocks of the EPC91108 with two EPC2055 GaN FETs is shown in figure 1.

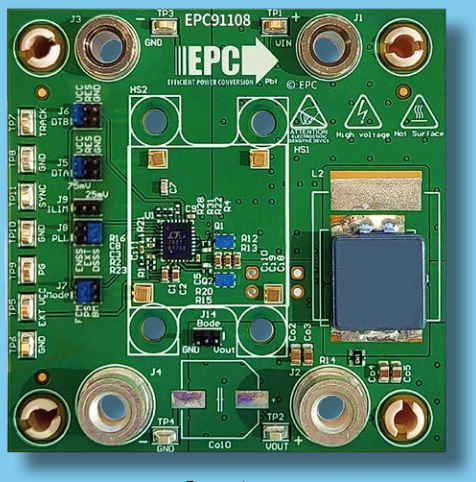
REGULATORY INFORMATION

This power module is for evaluation purposes only. It is not a full-featured power module and cannot be used in final products. No EMI test was conducted. It is not FCC approved.

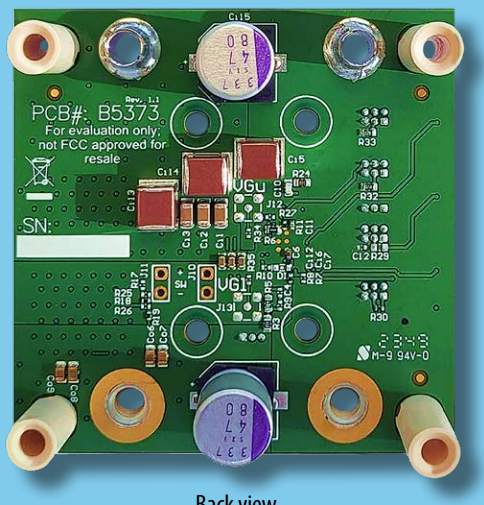
KEY FEATURES OF THE EPC91108 EVALUATION BOARD

- Employs two low conduction and switching loss EPC2055 GaN FETs in half-bridge buck power stage,
- Simple, high power-density, compact layout of 15 x 15 mm of the power converter circuit area,
- Configured with a small inductor of just 11 x 11.9 mm size,
- Synchronous buck configuration for high efficiency,
- Low component count solution.

EPC91108 Evaluation Board



Front view



Back view

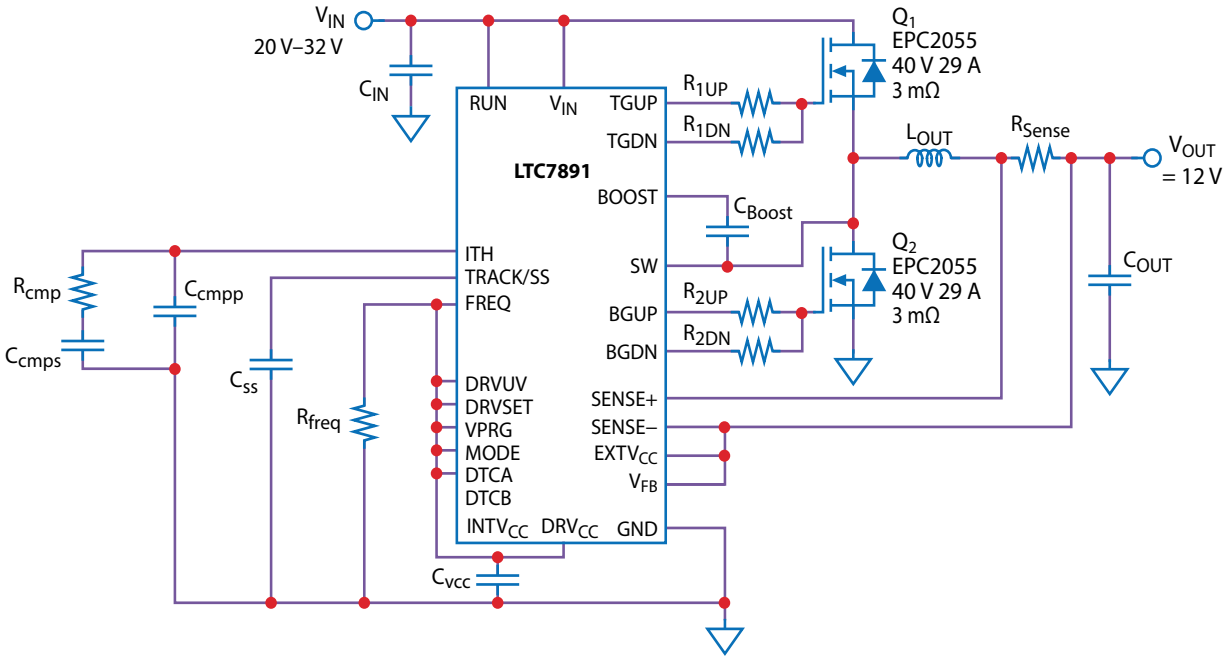


Figure 1: Block diagram overview of the EPC91108 evaluation board

FEATURED GaN FET

The EPC91108 evaluation board features the two 40 V rated, 3 mΩ $R_{DS(on)}$ EPC2055 GaN FETs in a half bridge buck configuration. The symbol of GaN FET and photo with pin assignment are shown in figure 2.

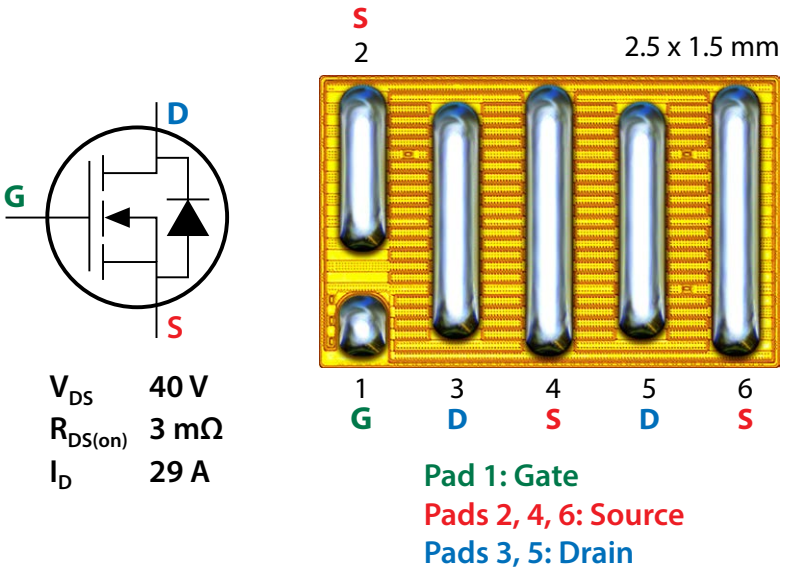


Figure 2: Symbol and photo with pin assignment of the EPC2055

Refer to the **EPC2055 datasheet** for additional details.

OVERVIEW OF THE EPC91108 EVALUATION BOARD

Figure 3 shows an image of both sides of the EPC91108 evaluation board with the location of the various functional circuits highlighted.

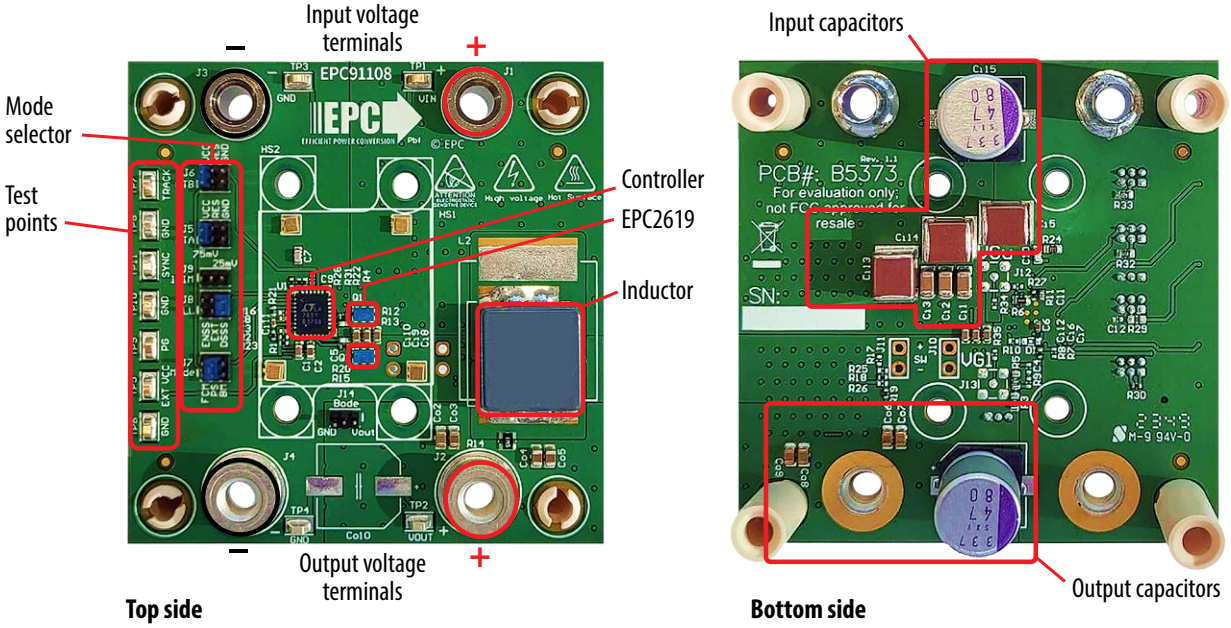


Figure 3: Photo overview of the EPC91108 evaluation board with various functional blocks highlighted

Figure 4 shows a photo of the zoomed-in area of both sides of the application circuit.

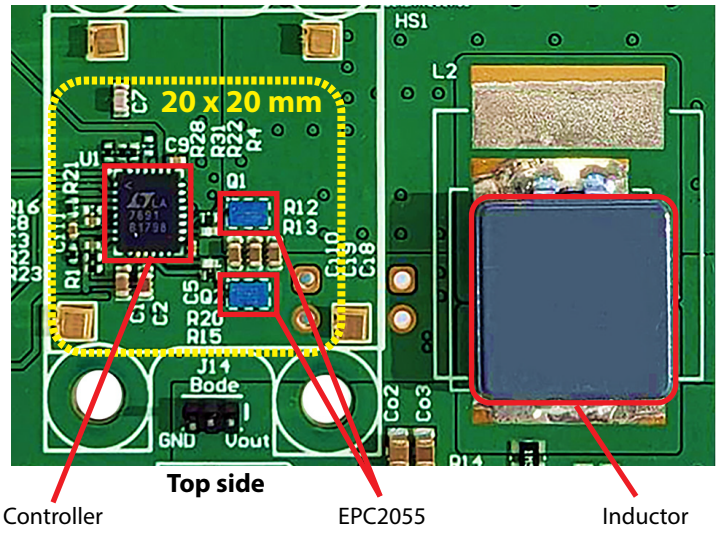


Figure 4: Zoomed-in photo details of the EPC91108 evaluation board with power circuit highlighted

It can be seen from figure 4 that the circuit is compact and can fit in a small area of approximately 20 x 20 mm excluding the inductor, input capacitors, and output capacitors.

RECOMMENDED OPERATING CONDITIONS

Table 1: Performance Summary (T_A = 25°C) EPC91108

Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{IN}	Input Voltage Port (VIN)	Iout up to 21A	20	28	32 [1]	V
V_{OUT}	Output Voltage Port (VOUT)	Vin = 20 V to 40 V		12		
I_L	Output Current	With no heatsink & 400 LFM airflow			21 [2,3]	A
f_{SW}	Nominal Switching frequency			800 [4]		kHz
TP11: Ext SYNC	Fclock Synchronizable Range	PLL (J8) = EXT (Pin2-3) Rise and Fall time < 10 ns	0.1		5.5	MHz
	Clock Input High		2.2			V
	Clock Input Low				0.5	
PG	Power Good logic output	Low			0.4 [5,6]	

[1] *Maximum voltage limited by the voltage rating of two GaN FETs (40 V). In addition, the board was not tested in closed loop beyond 32 V input voltage.*

[2] *Maximum current capability is lower than stated in EPC2055 datasheet as it is dependent on thermal conditions and die temperature, and on component choice and board design – actual maximum current is affected by switching frequency, bus voltage, inductor current and thermal limits, and thermal cooling. Refer to thermal performance section in this guide and to EPC2055 datasheet for details.*

[3] *Due to inductor limitations, the current must stay below the saturation current and the temperature within its rated range.*

[4] *LTC7891 controller can operate from 200kHz through 3MHz switching frequency. EPC91108 is set to operate at a fixed switching frequency of 800 kHz.*

[5] *The power good open-drain output is connected to the 5 V INTVCC pin through a 1 Megaohm resistor.*

[6] *Power good logic output is low when the output voltage is not within +/- 10% of 12 V output voltage.*

HIGHLIGHTED PARTS OF THE EPC91108 CIRCUIT

Refer to figures 1 and 4 for the main blocks and components that comprise the EPC91108 evaluation board.

Power Stage

The EPC91108 features a half-bridge buck converter using the EPC2055 GaN FETs. For more information on the EPC2055, please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Current and Voltage Sense

The EPC91108 evaluation board is equipped with voltage and current sense for feedback. Voltage is measured using simple resistor divider networks and bode measurement points are provided for closed loop tuning. **J14** is used for signal injection and measurement for bode plots.

Inductor current is measured using a current sense shunt of 1.5 mΩ (**R14**). This shunt provides a voltage signal proportional to the current, which the controller then uses for both current limiting and output voltage regulation. The controller compares this voltage signal with a reference output voltage to control the duty cycle of the PWM signal. The current sense shunt provides real-time feedback on the inductor current, enabling the controller to achieve both current limiting and output voltage regulation.

Controller

The power circuit of the EPC91108 evaluation board is controlled using the LTC7891RUFD synchronous step-down controller from Analog Devices and is configured in fixed frequency and peak current mode control. The functions of the LTC7891RUFD controller can be adjusted using the appropriate jumper-setting. For information on configuring the controller, please refer to the jumper section.

Center Capacitor Layout

The EPC91108 board utilizes a center capacitor layout technique to enhance both thermal and electrical performance [1]. This technique involves positioning the input bypass capacitor between the high-side and low-side FETs. Since capacitors act as thermal barriers, placing them on either side of the FET creates an asymmetrical thermal distribution. Off-center placement causes the FET closer to the capacitors to experience higher thermal resistance, leading to more trapped heat. By centering the capacitor, both FETs have a more balanced thermal path as shown in Figure 5.

The center capacitor layout offers an additional benefit. Unlike the one-sided capacitor layout (Figure 6(a)) where the switch node plane resides on the outer layer, the center capacitor layout buries the switch node plane within the inner layer and shields it with DC voltage planes (ground and input voltage) (Figure 6(b)). This design results in lower radiated electromagnetic emissions, which is crucial for applications where minimizing EMI is important.

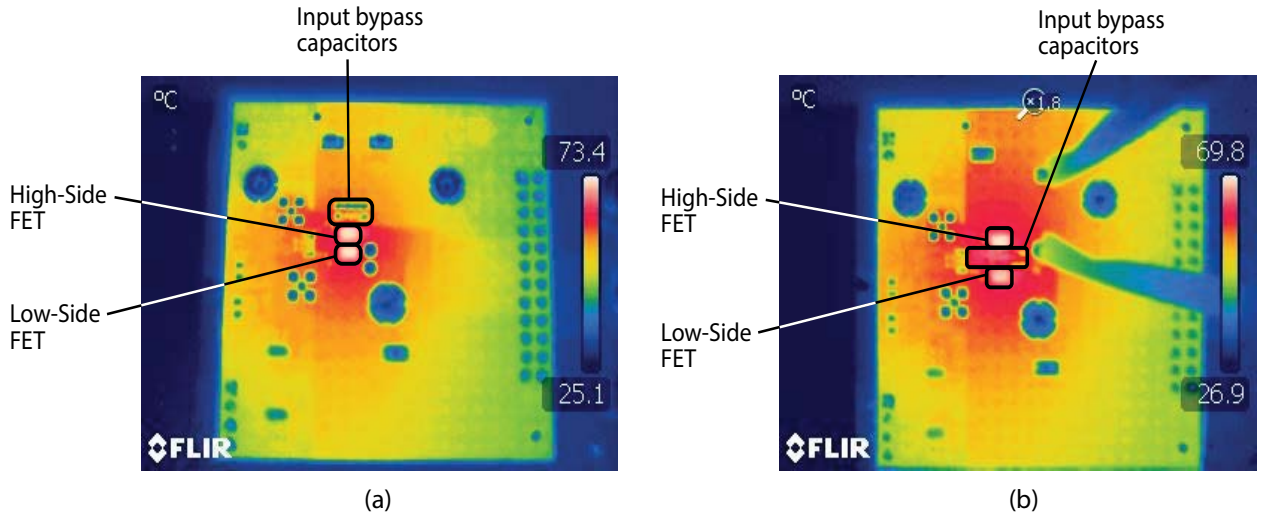


Figure 5 shows the difference of the heat dissipation between (a) with bus capacitors are located next to the high-side FET, and (b) with the bus capacitors located between the FETs.

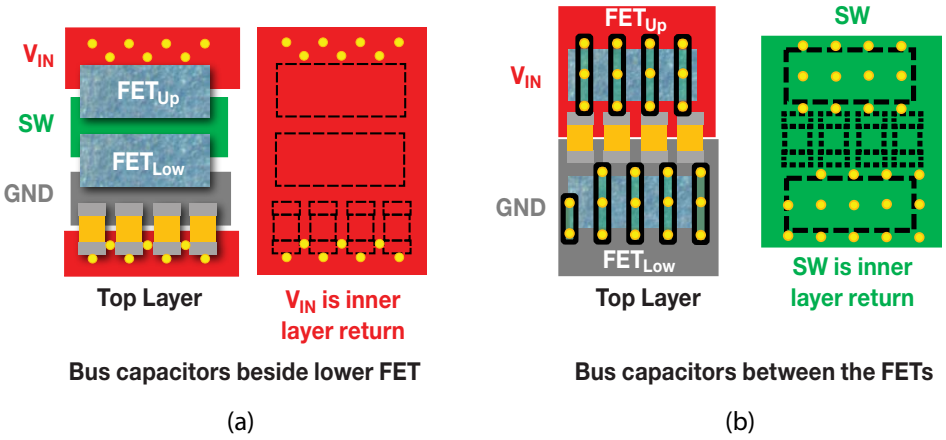


Figure 6 shows the switch node layer in (a) with bus capacitors located next to the low-side FET, and (b) with the bus capacitors located between the FETs.

CONNECTIONS, MEASUREMENT TEST POINTS & JUMPERS

Power Connections

To operate the EPC91108, connect the input supply and the load as shown in figure 7.

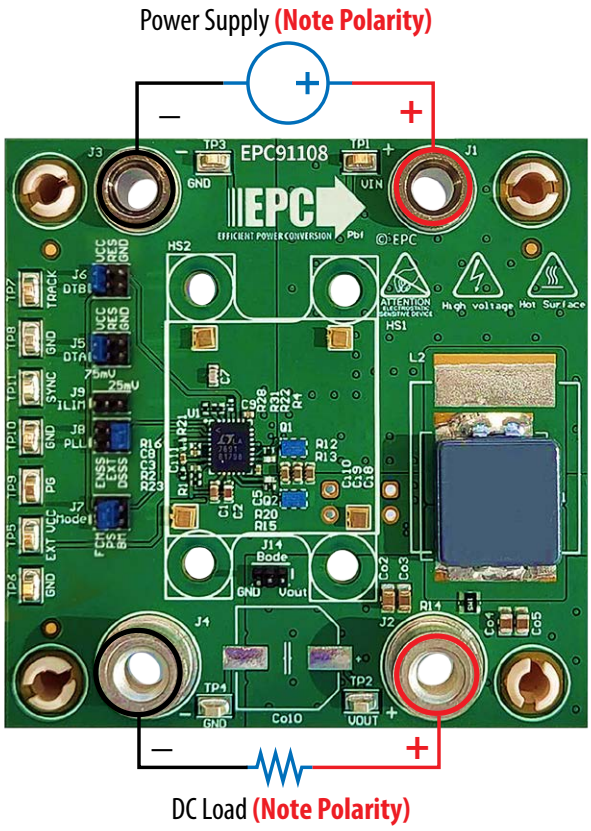


Figure 7: Power connections to the EPC91108 evaluation board.

Test Points and Measurement Setup

Figure 8 and 9 show the various measurement connections of the EPC91108 evaluation board.

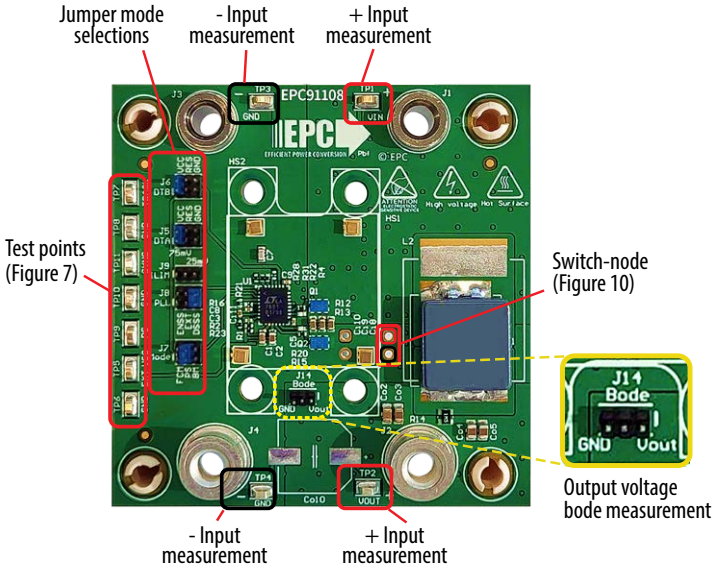


Figure 8: EPC91108 test point pad and hookup locations and designations.

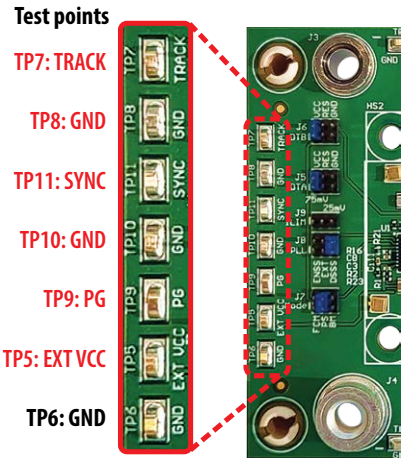


Figure 9: Details of the test points of EPC91180 evaluation board.

The available measurement nodes with their respective reference are:

- **VIN-GND**: High voltage port voltage (**TP1** & **TP3**)
- **VOUT-GND:** Output voltage **(TP2 & TP4),**
- **SYNC-GND:** Clock waveform when external clock is applied **(TP11 & TP10),**
- **TRACK-GND:** Initial ramp soft start (**TP7 & TP8),**
- **EXTVCC-GND:** External supply voltage to controller **(TP5 & TP6),**
- **PG-GND:** Power good logic output **(TP9 & TP10).**
- **VOUT-BODE-GND:** Low voltage port bode injection and measurement **(J14)**

Note: Exercise caution when using the bode measurements to ensure proper connection to the instrument.

Switch-node

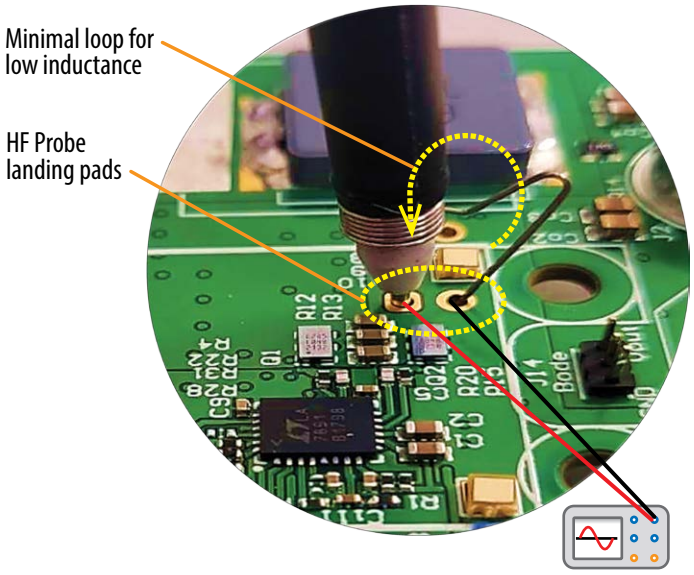


Figure 10: Recommended method to measure the switch- node measurement voltage waveform.

Jumper Settings

Note: A jumper must be inserted to select a mode at each jumper connector.

Dead-Time settings

The EPC91108 has two dead-time settings; 1) switch-node rising edge, and 2) switch-node falling edge. The rising edge is the dead time between Q2 turn-off (lower device) and Q1 turn-on (upper device) set using J5 and the falling edge is the dead time between Q1 turn-off and Q2 turn-on set using J6. The available settings for both J5 and J6 are; 1) position 1-2 (VCC) for near zero dead-time (default), 2) position 3-4 (RES) for approximately 10 ns dead-time, and 3) position 5-6 (GND) for 20 ns dead-time. Details are shown in figure 11.

Light-Load Mode Selection

The EPC91108 has three light-load operating modes available which are 1) forced continuous inductor current (FCM), 2) pulse skipping (PSM), and 3) burst mode (BM). See the LTC7891 datasheet for details on each operating mode. The desired operating mode can be selected by inserting a jumper into the appropriate position on J7 with position 1-2 for FCM, position 3-4 for PSM (default) and position 5-6 for BM. Refer to Figure 12.

Oscillator Settings

The EPC91108 has three oscillator setting options; 1) Disable spread spectrum (DS SS), 2) External clock, and 3) Enable spread spectrum (EN SS). See the LTC7891 datasheet for details on each setting and refer to table 1 for external clock voltage levels. The desired setting can be selected by inserting a jumper into the appropriate position on J8 with position 1-2 for EN SS, position 3-4 for External clock (Ext SYNC), and position 5-6 for DS SS (default). When selecting the external clock option, the external signal can be connected between SYNC (TP11) and GND (TP10) and must be within the specifications of the LTC7891 IC given in table 1. See Figure 12 for the location of the oscillator jumper settings.

Current sense settings

The LTC7891 internal current comparator can be configured with one of three maximum current sense threshold settings which are 25 mV, 50 mV and 75mV. The threshold level can be selected by inserting the jumper on J9 (Figure 12) with position 1-2 for 75 mV threshold, position 2-3 for 25 mV threshold, and without inserting jumper for 50 mV threshold (default). Please refer to the LTC7891 datasheet for more information.

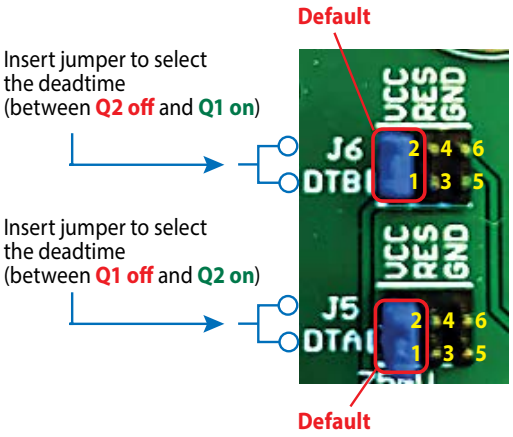


Figure 11: EPC91108 selector point locations and designations for dead time setting.

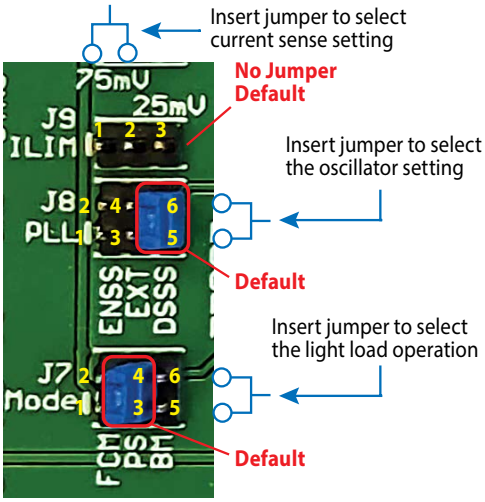


Figure 12: EPC91108 selector point locations and designations for oscillator and light load mode settings.

QUICK START PROCEDURE

The EPC91108 evaluation board is easy to set up to evaluate the performance of the EPC2055 GaN FETs. Refer to figures 7, 8, 9, 10, 11 & 12 for proper connection and measurement setup and follow the procedure below to operate the board:

1. With power off, connect the input power supply between VIN (**J1**) and GND (**J3**). Pay careful attention to the polarity of the supply as shown in figure 7. A shunt can be inserted in series with the positive supply to measure the input current.
2. Ensure the jumpers settings of **J5**, **J6**, **J7**, and **J8** are in the default positions.
3. With power off, connect a suitable load between VOUT (**J2**) and GND (**J4**). Pay careful attention to the polarity as shown in figure 7.
4. With power off, connect the various measurement probes as shown in figure 8 and 9.
5. **Keeping the load off**, turn on the main power supply. Observe that the output voltage is 12 V.
6. Adjust the load current within the current capability of the EPC91108 per table 1. Observe the temperature of the GaN FET and ensure that it does not exceed the maximum value given in the **EPC2055 datasheet**.
7. Collect the data measurements while adjusting the supply voltage and load current Ensure that all operating parameters remain within the specifications provided in table 1.
8. To shut down the EPC91108 evaluation board, decrease the main power supply to 0 V before turning off.

The operating instructions in this document do not cover how to perform bode measurements. Please refer to the equipment manufacturer for those instructions.

THERMAL MANAGEMENT (Optional)

The EPC91108 is intended for bench evaluation at room ambient temperatures and under forced air convection cooling. The addition of heatsink along with forced air cooling is not required but can significantly improve the heat dissipation from heating parts by adding cooling from the top side of the device and thus increase the current capacity of the application.

Figure 13 shows an exploded 3D view of the simple cooling system for the EPC91108 evaluation board that comprises just 3 elements; 1) a heatsink, 2) a 4 mm x 8.5 mm Thermal interface material (TIM) shown in figure 14, and 3) Heatsink resting posts.

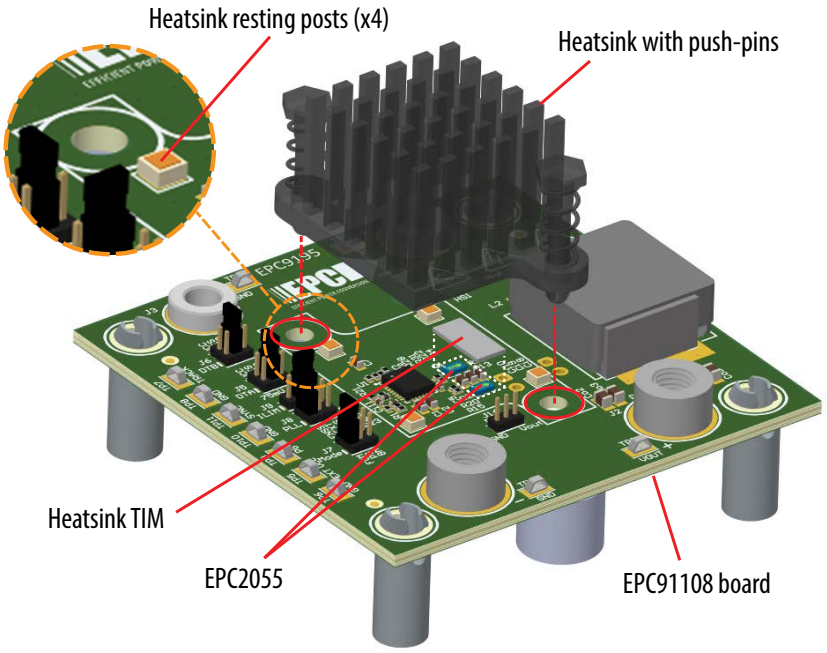


Figure 13: Exploded view of the EPC91108 heatsink assembly.

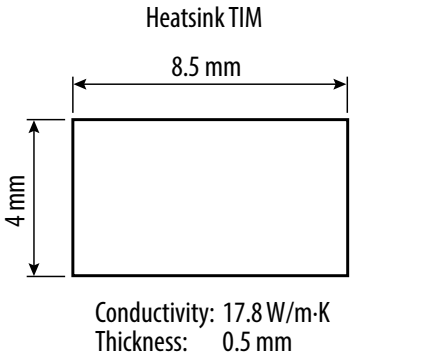


Figure 14: Details of the recommended TIM's used on the EPC91108 evaluation board.

It is important that the TIM properly covers both eGaN FETs. The heatsink is then carefully placed on top aligned with the pop-in pins located into their respected holes in the EPC91108 PCB. The heatsink rests on custom 2 x 2 mm a 1 mm tall standoff posts located at the corners of the heatsink landing made from low cost FR4. The pins are then carefully popped into place to secure the heatsink.

The choice of TIM for the eGaN IC needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the eGaN FET/IC. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the eGaN FET/IC is a silicon substrate that is connected to ground. Electrical insulation is not required but is still recommended to isolate the GaN IC from the thermal solution.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials are preferred to provide higher thermal conductance at the interface.

EPC recommends the t-Global Part Number: TG-A1780 for the eGaN FETs TIM as it has a high thermal conductivity of 17.8 W/m·K.

EXPERIMENTAL VALIDATION

The EPC91108 evaluation board is designed to demonstrate its capabilities in battery chargers for inboard USB PD 3.1 laptops powered by 12 V batteries. The board is configured using the default jumper settings and operated from a supply ranging from 20 V through 32 V.

Power Performance

The measured efficiency of the EPC91108 operating with various supply voltages is shown in figure 15.

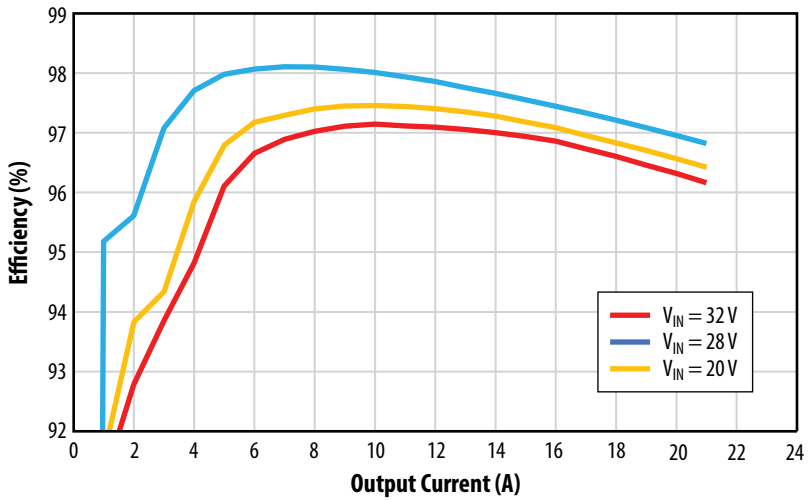


Figure 15: Measured the efficiency of the EPC91108 board for multiple input voltages and V_{OUT} = 12 V, 400 LFM airflow and without a heatsink installed.

The measured system power loss of the EPC91108 operating from various supply voltages is shown in figure 16. The power loss includes the power consumption of the controller and switching losses of the EPC2055 eGaN FET.

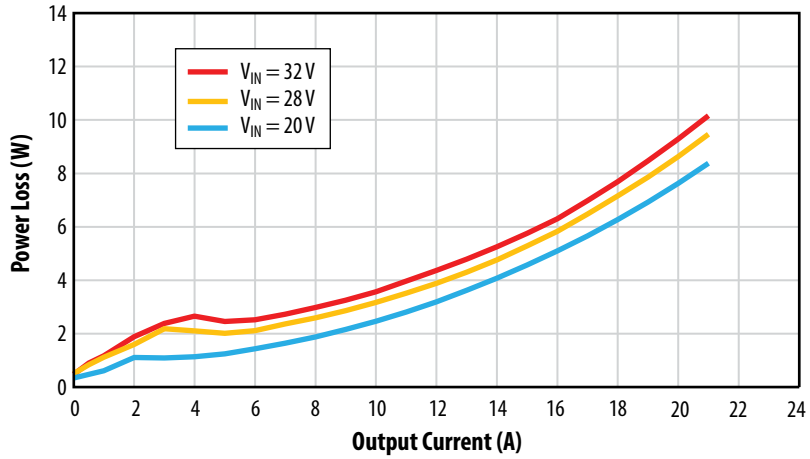


Figure 16: Measured system power loss of the EPC91108 board, operating for multiple input voltages and VOUT = 12 V, 400 LFM airflow and without a heatsink installed.

Waveforms

Figure 17 shows the measured switch-node waveform taken with the EPC91108 operating with 28 V input, 12 V output and delivering 12 A into the load.

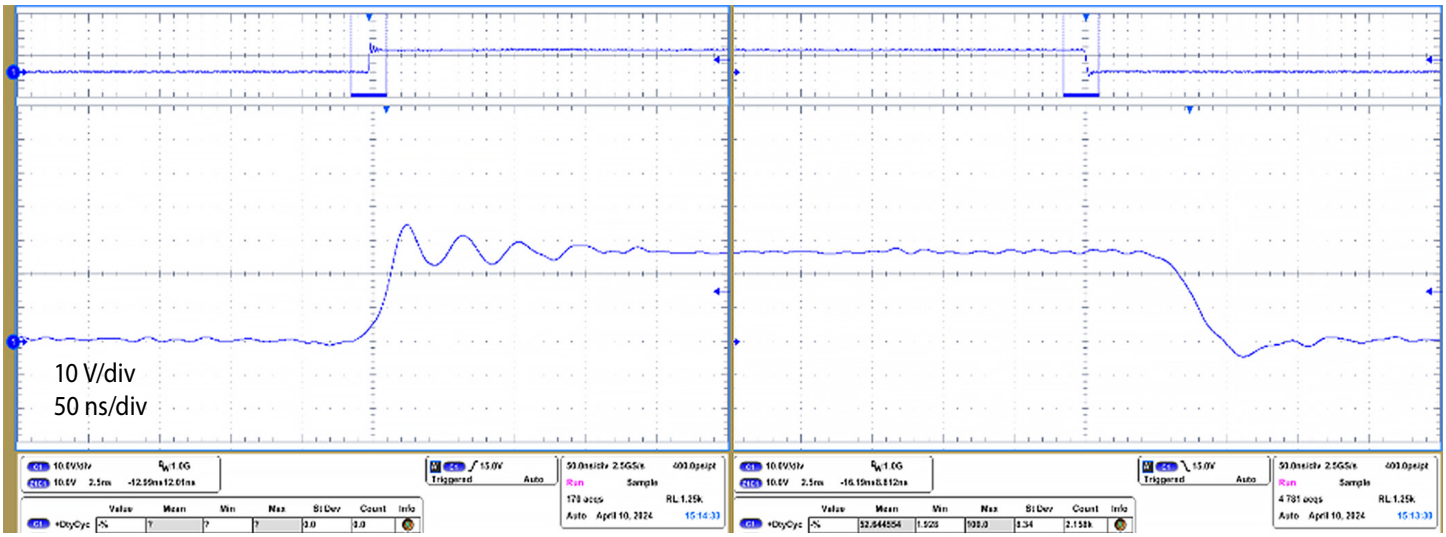


Figure 17: Measured switch-node voltage waveform of the EPC91108 operating with 28 V input, 12 V output and delivering 12 A into the load.

Figure 18 shows the measured output ripple voltage taken with the EPC91108 operating with 28 V input, 12 V output and delivering 12 A into the load.

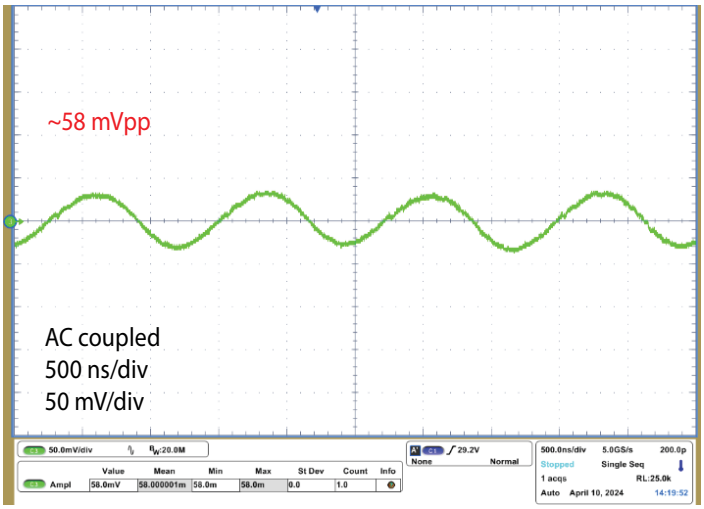


Figure 18: Measured ripple output voltage waveform of the EPC91108 operating with 28 V input, 12 V output and delivering 12 A into the load.

Transient Response

Figure 19 shows the measured transient response taken with the EPC9195 operating with 28 V input, 12 V output with a load step change of 10% to 90% and 90% to 10% of 12 A output.

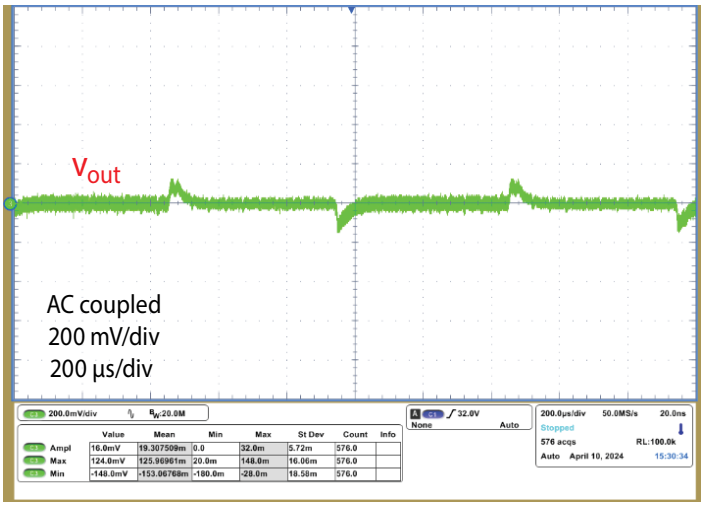


Figure 19: measured transient waveform of the EPC91108 operating with 28 V input, 12 V output and with a load step change of 10% to 90% and 90% to 10% of 12 A.

Voltage Regulation Performance

Figure 20 shows the measured output voltage regulation taken with the EPC91108 operating with different input voltages and delivering 12 V into the load as function of load current.

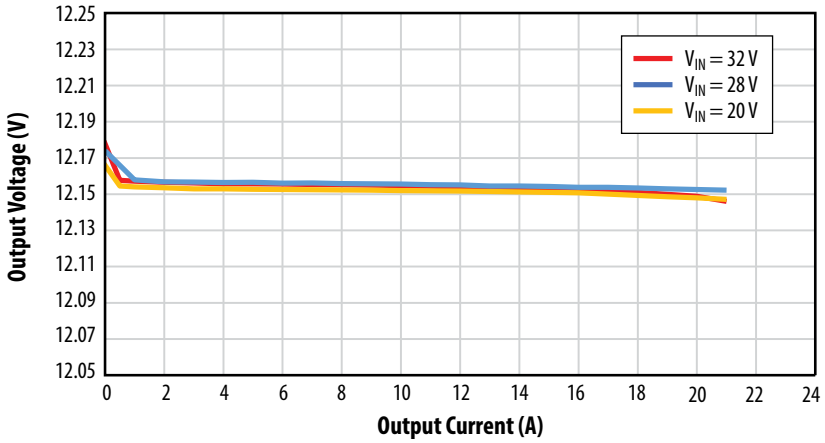


Figure 20: Measured output voltage regulation of the EPC91108 operating with various input voltages and delivering 12 V into the load as function of load current.

Thermal Performance

Figure 21 through 23 shows the measured thermal performance of the EPC91108 converter under 20 V, 28 V, and 32 V input. The output was set to 12 V and the converter delivered 21 A to the load. The converter operated with no heatsink installed and with 400 LFM airflow.

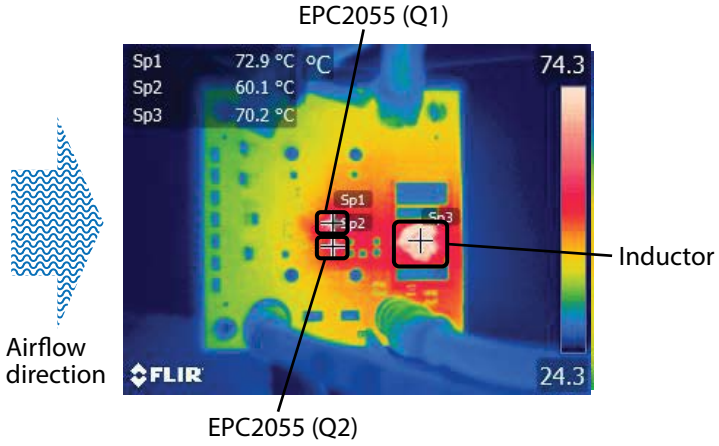


Figure 21: Steady state measured thermal image of the EPC91108 operating with 20 V input, 12 V output and delivering 21 A into the load, 400 LFM airflow and no heatsink attached.

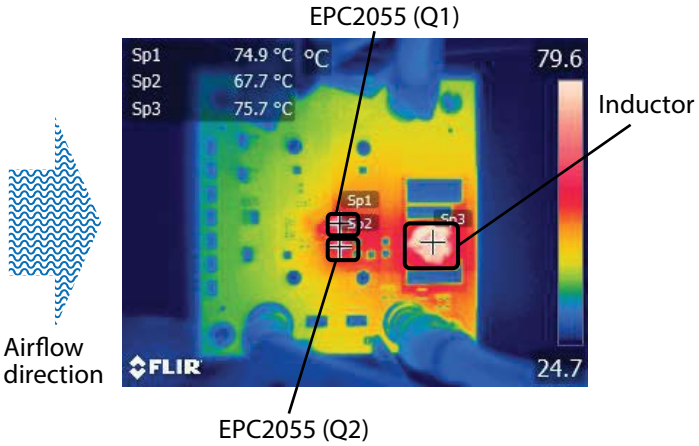


Figure 22: Steady state measured thermal image of the EPC91108 operating with 28 V input, 12 V output and delivering 21 A into the load, 400 LFM airflow and no heatsink attached.

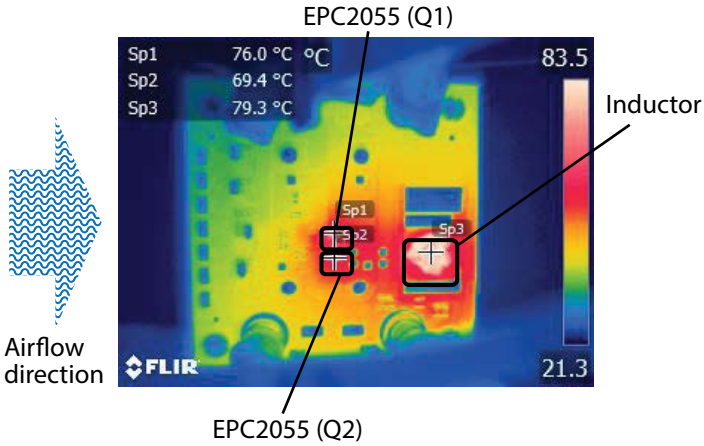


Figure 23: Steady state measured thermal image of the EPC91108 operating with 32 V input, 12 V output and delivering 21 A into the load, 400 LFM airflow and no heatsink attached.

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC91108 landing page at: https://epc-co.com/epc/products/evaluation-boards/epc91108

Reference

[1] Glaser, J.S., Helou, A. (2022). PCB layout for chip-scale package GaN FETs optimizes both electrical and thermal performance. IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, (20–24 March 2022).

ACKNOWLEDGEMENTS

ANALOG DEVICES

EPC would like to acknowledge Analog Devices Inc. (www.analog.com) for their support of this project. Analog Devices (NASDAQ: ADI) is a world leader in the design, manufacture, and marketing of a broad portfolio of high performance analog, mixed-signal, and digital signal processing (DSP) integrated circuits (ICs) used in virtually all types of electronic equipment. Since their inception in 1965, they have focused on solving the engineering challenges associated with signal processing in electronic equipment. Used by over 100,000 customers worldwide, their signal processing products play a fundamental role in converting, conditioning, and processing real-world phenomena such as temperature, pressure, sound, light, speed, and motion into electrical signals to be used in a wide array of electronic devices.

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Evaluation Board Notification

The EPC91108 board is intended for product evaluation purposes only. It is not intended for commercial use nor is it FCC approved for resale. Replace components on the Evaluation Board only with those parts shown on the parts list (or Bill of Materials) in the Quick Start Guide. Contact an authorized EPC representative with any questions. This board is intended to be used by certified professionals, in a lab environment, following proper safety procedures. Use at your own risk.

As an evaluation tool, this board is not designed for compliance with the European Union directive on electromagnetic compatibility or any other such directives or regulations. As board builds are at times subject to product availability, it is possible that boards may contain components or assembly materials that are not RoHS compliant. Efficient Power Conversion Corporation (EPC) makes no guarantee that the purchased board is 100% RoHS compliant.

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