Paralleling eGaN® FETs for Efficient Power Conversion

The eGaN® FET Journey Continues

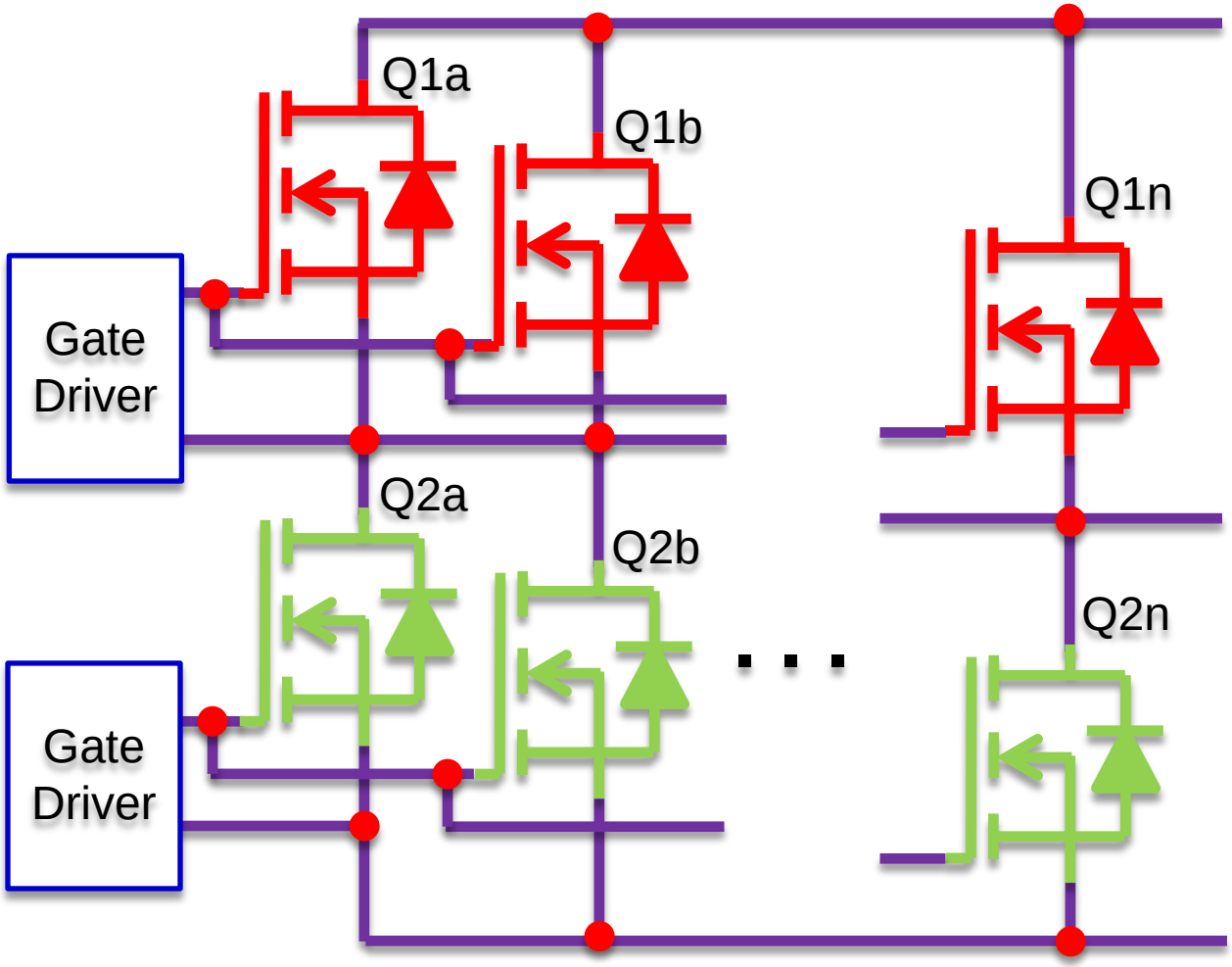
Alex Lidow and Michael de Rooij

Efficient Power Conversion Corporation

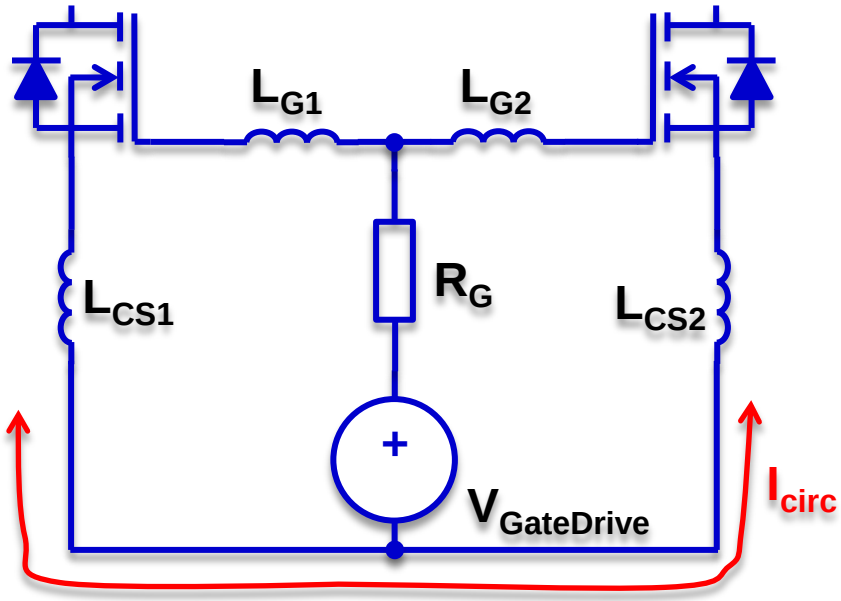
Agenda

- What happens when eGaN® FETs are paralleled?
- What are the best solutions?
- Introducing the Parallel Impact Figure (PIF)
- Layout Do's and Don'ts
- Summary

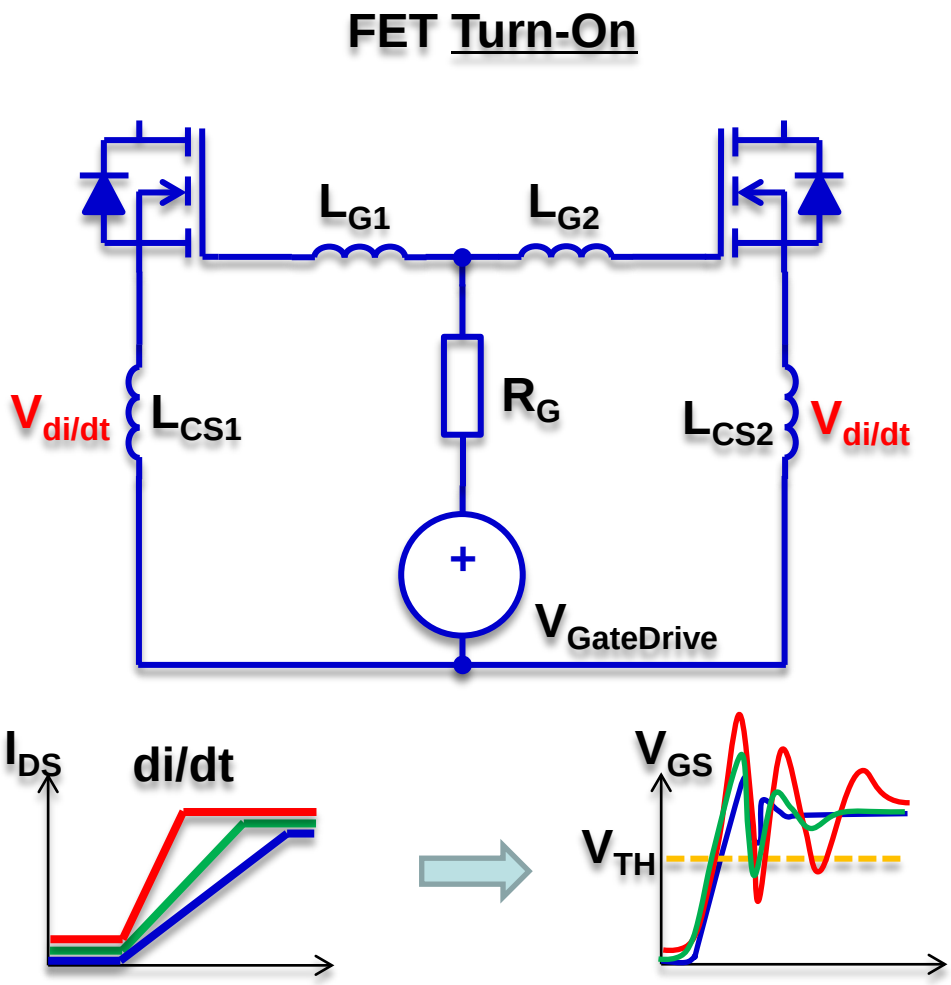
Half-Bridge topologies



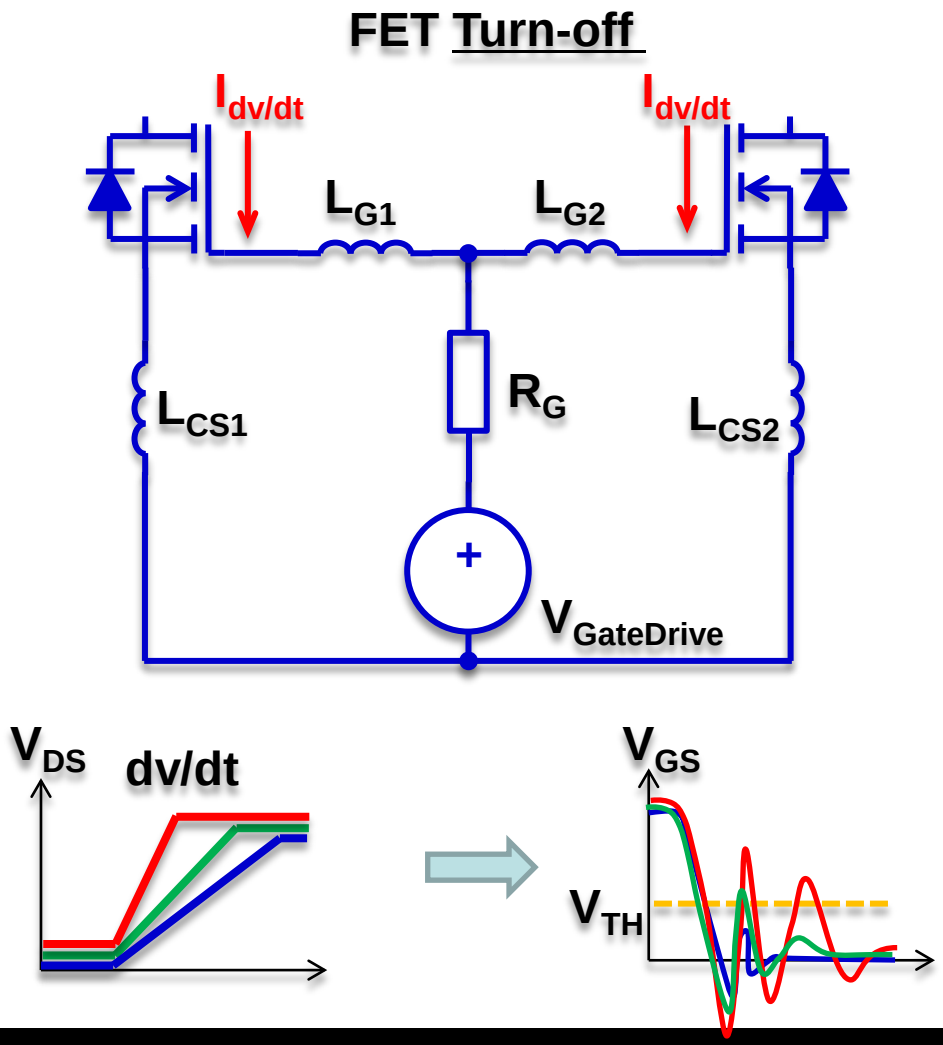
Switching Dynamics



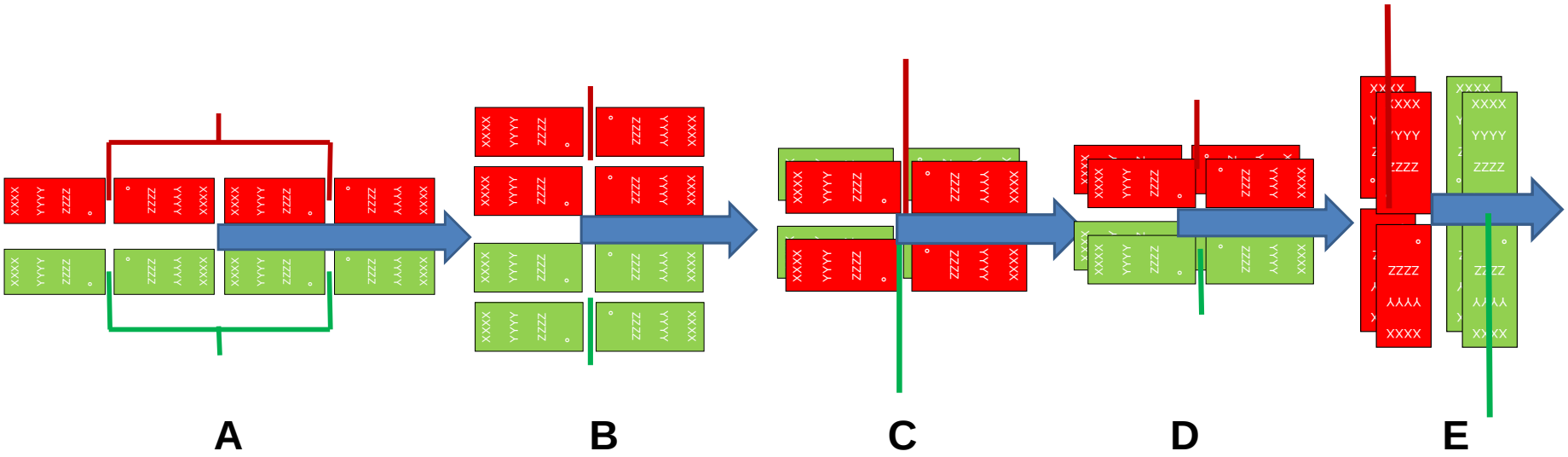
Switching Dynamics – Turn On



Switching Dynamics – Turn Off



Half Bridge Layout Evaluations



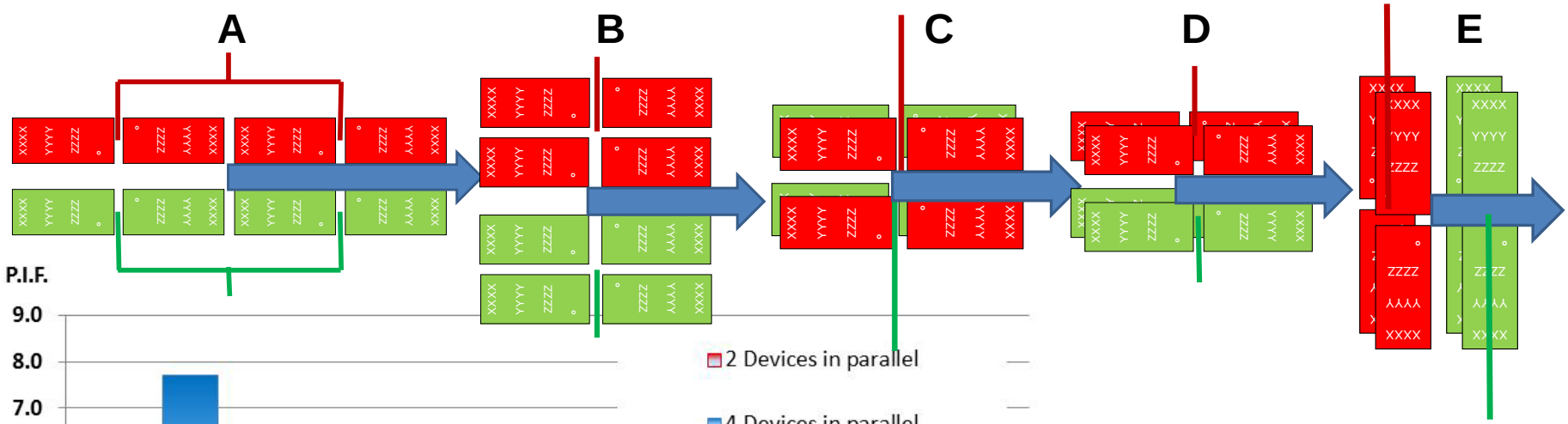
Single Component Sided ***Double Component Sided***

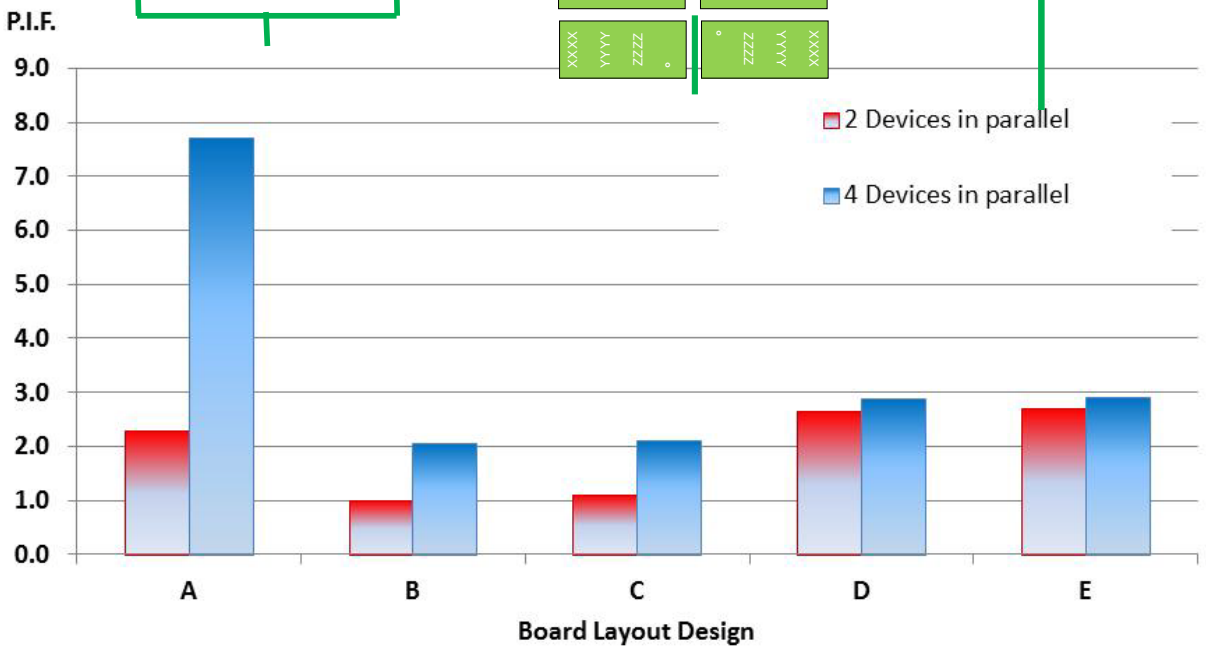
Introducing the PIF

- **Based on dv/dt and di/dt immunity**
- **Normalizes evaluations relative to a single FET**
- **Can be used to predict switching performance**

$$PIF_n = \frac{\frac{dv_1}{dt} + \frac{di_1}{dt}}{\frac{dv_n}{dt} + \frac{di_n}{dt}}$$

PIF for Half Bridge Layouts

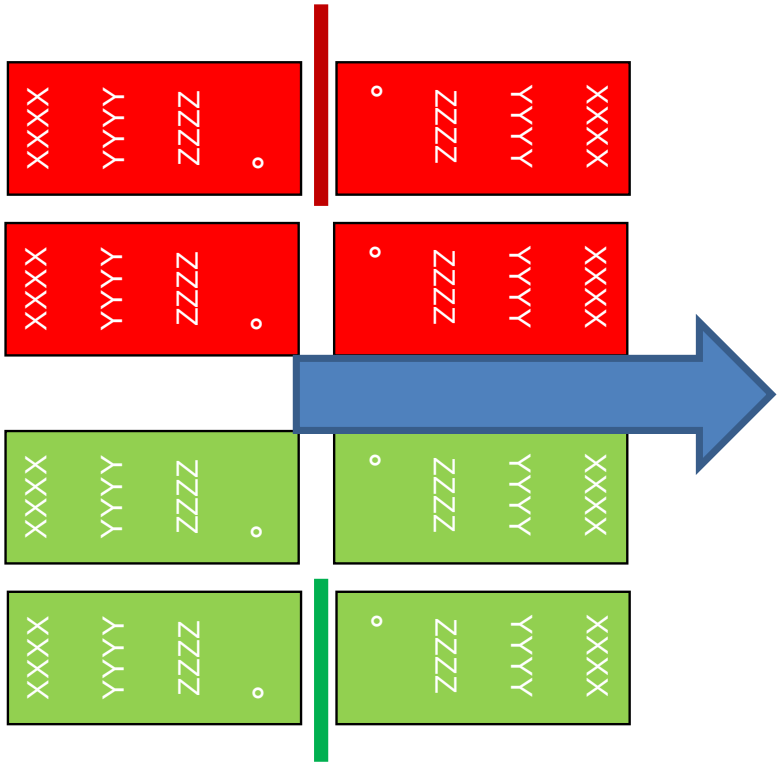




2 Devices in Parallel

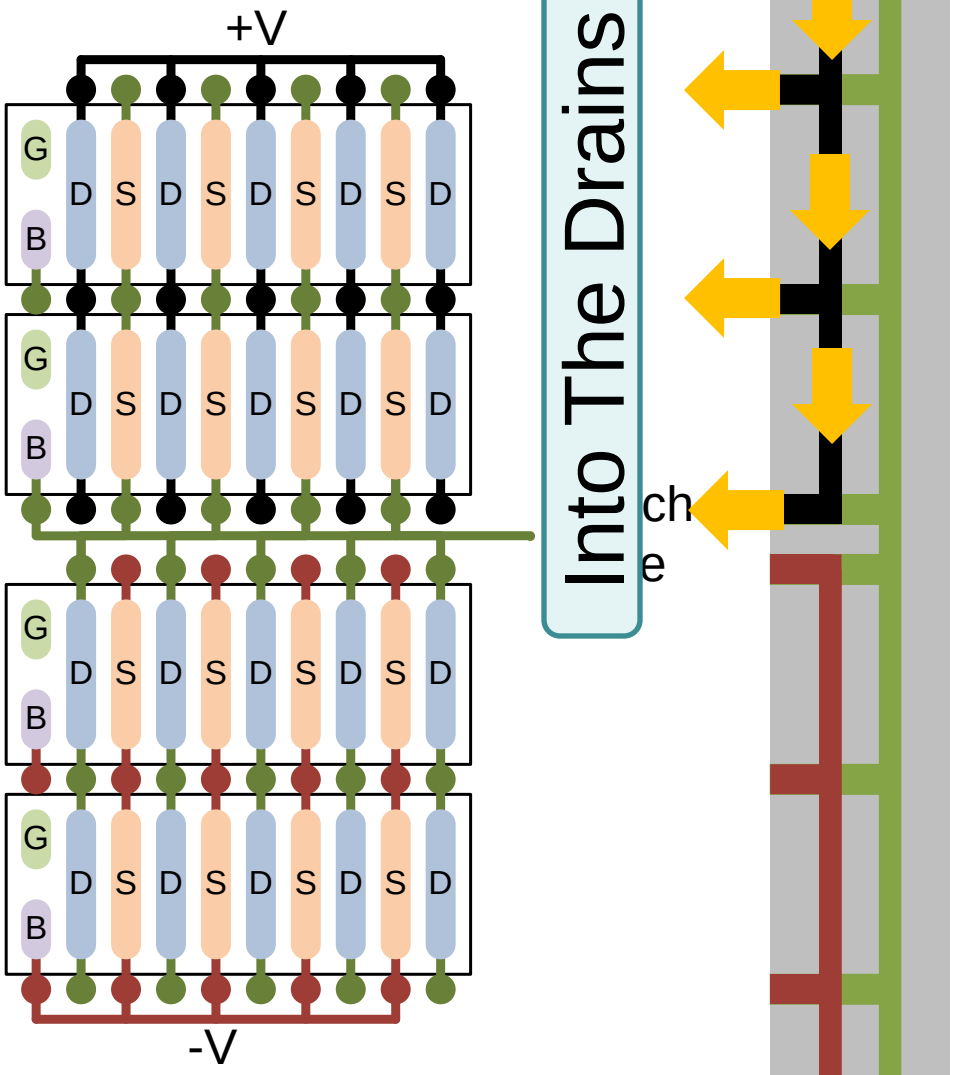
4 Devices in Parallel

Best Layout Configuration



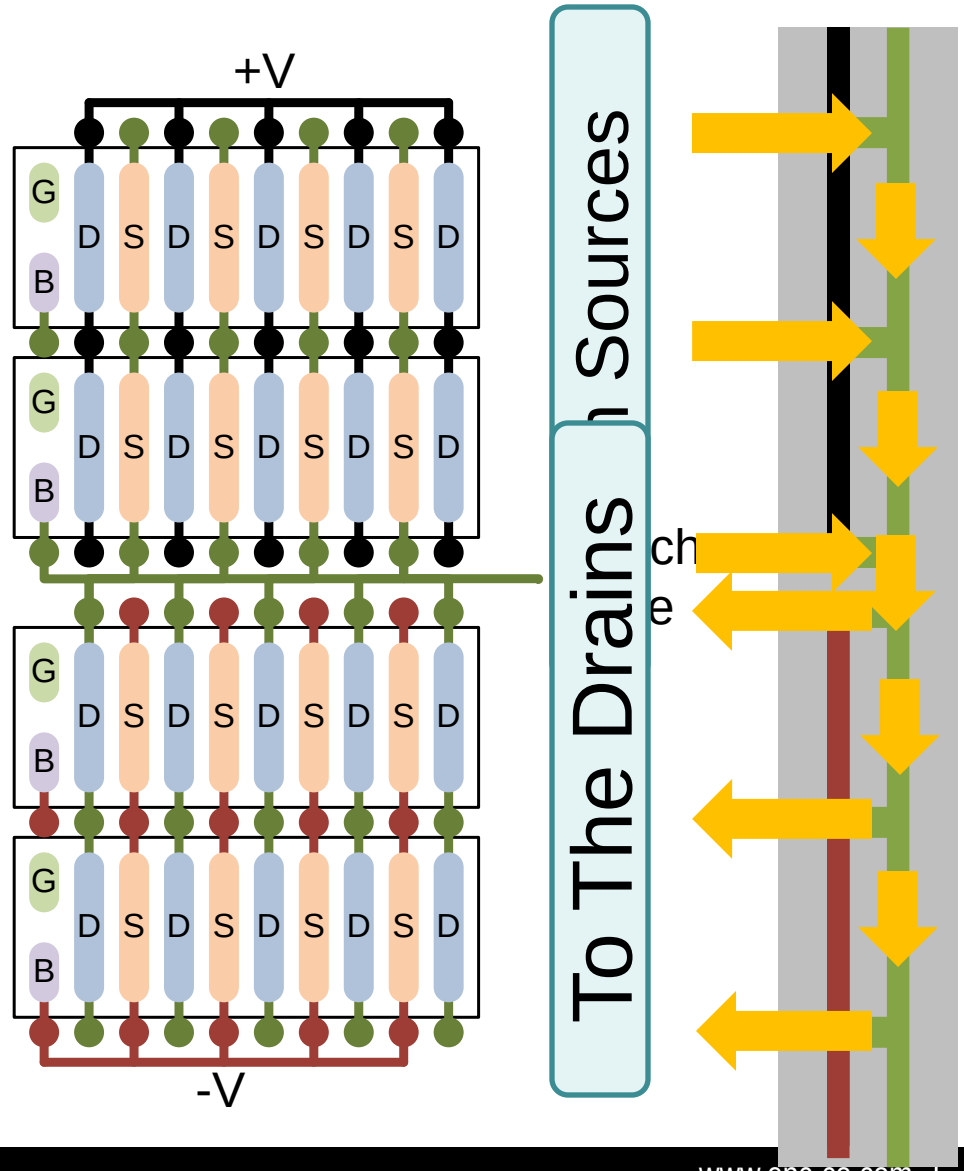
Layout Recommendation

Half Bridge Layout To Minimize And Balance Source Inductance



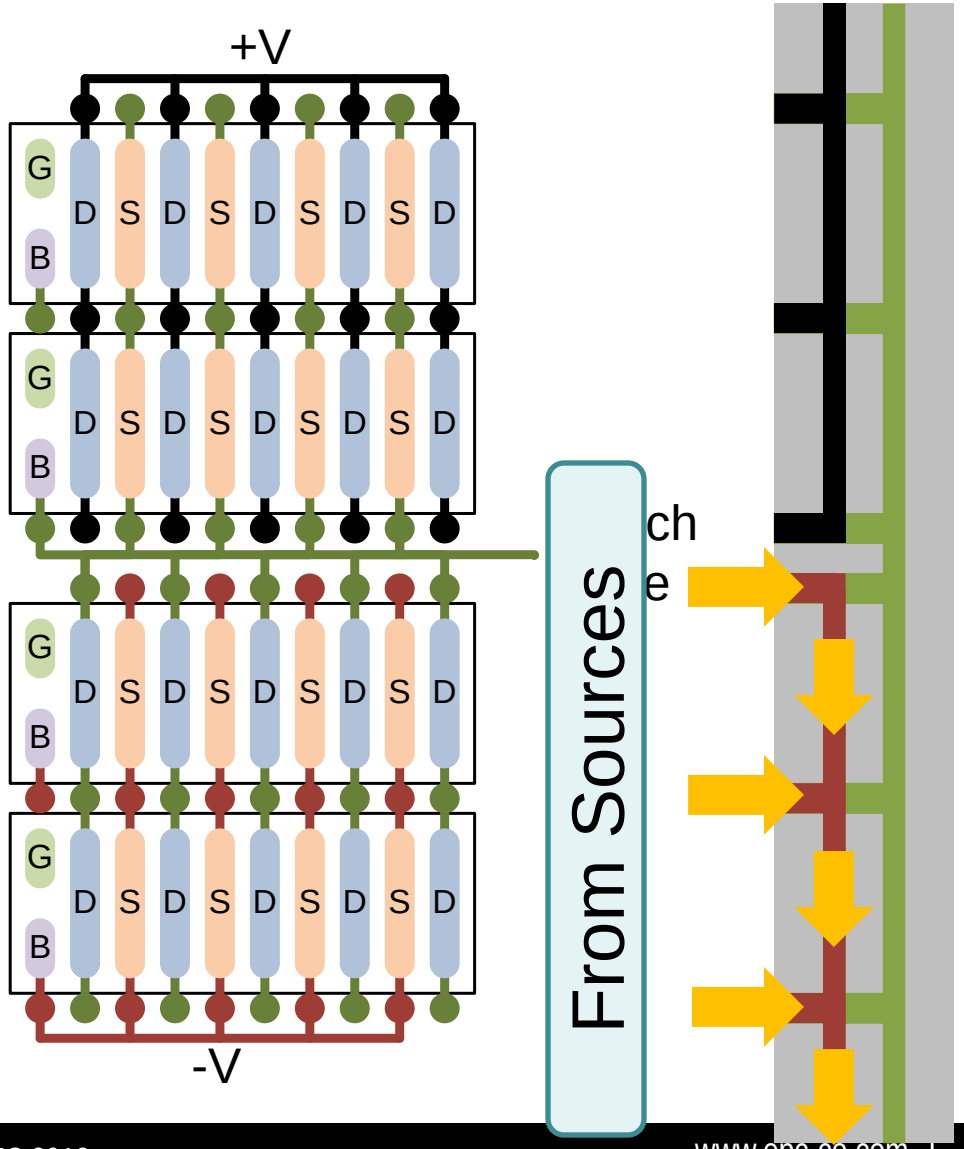
Layout Recommendation

Half Bridge Layout To Minimize And Balance Source Inductance



Layout Recommendation

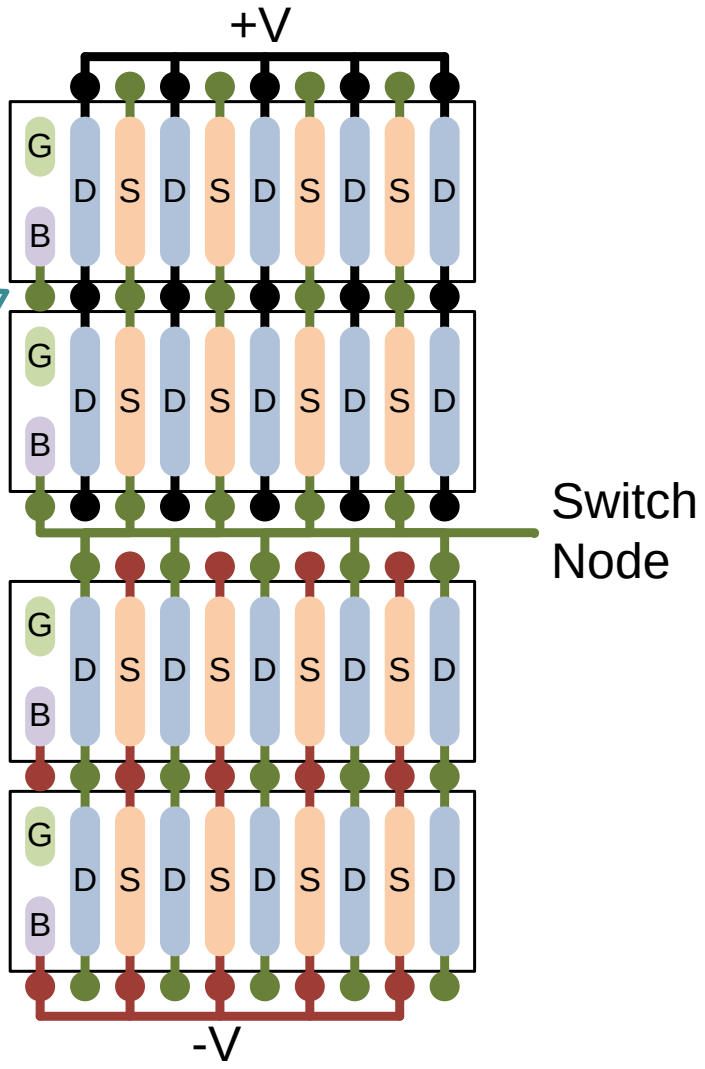
Half Bridge Layout To Minimize And Balance Source Inductance

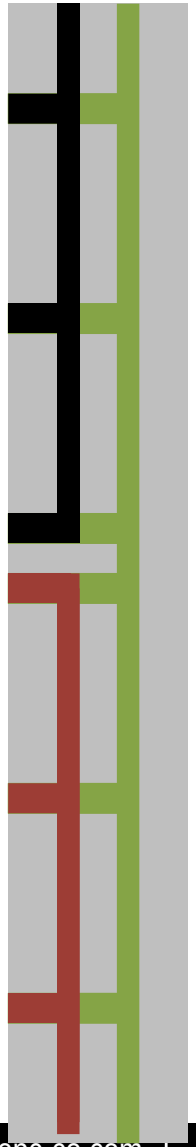


Layout Recommendation

Use Lots Of Vias To Stitch The Contacts To Inner Planes

And Balance Source Inductance





Layout Recommendation: Gates

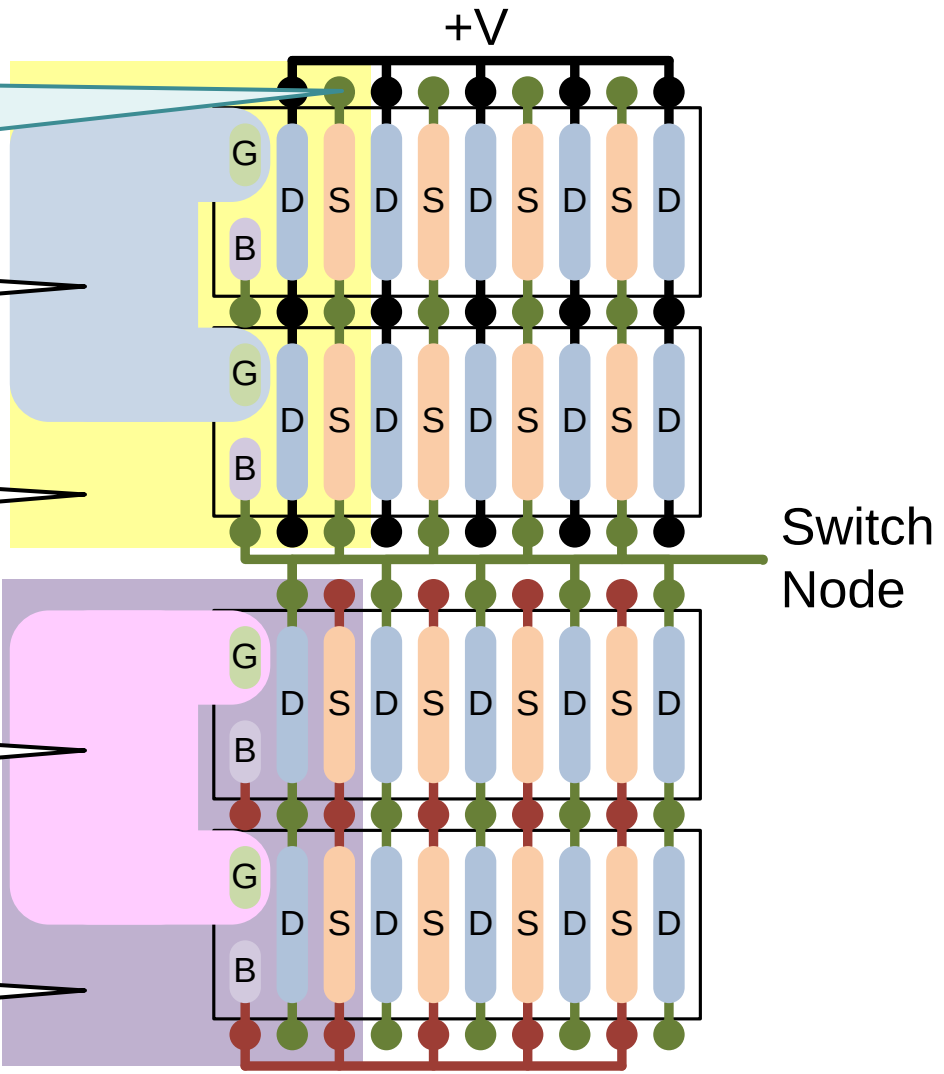
Gate Return Planes Connect To At Least First Set Of Source Vias

High Gate

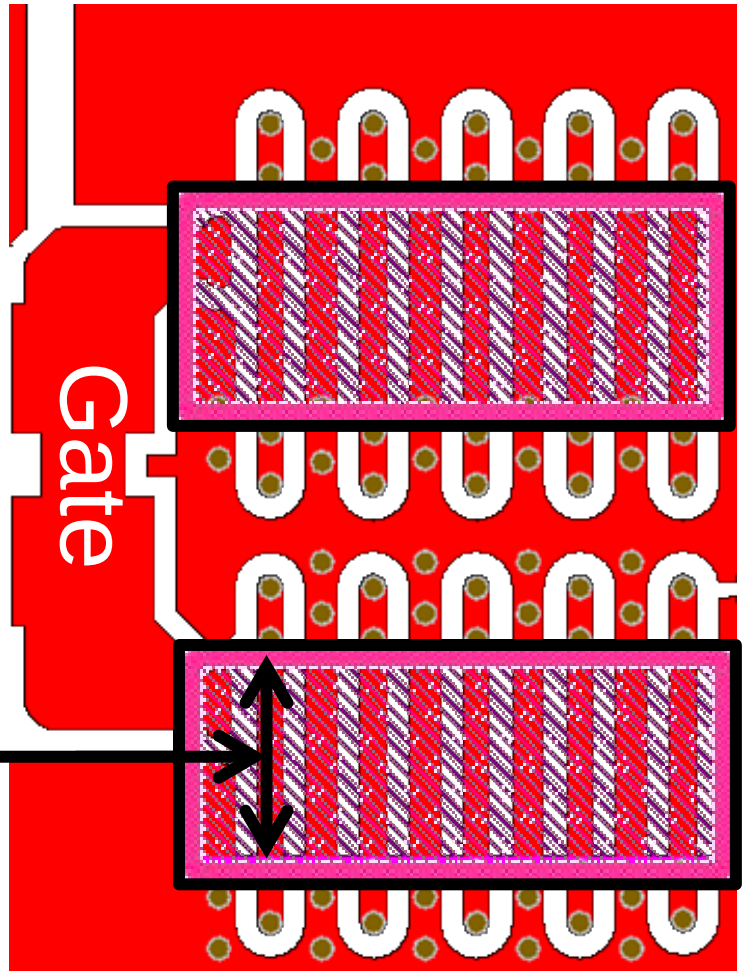
High Gate Return

Low Gate

Low Gate Return



Layout Detail

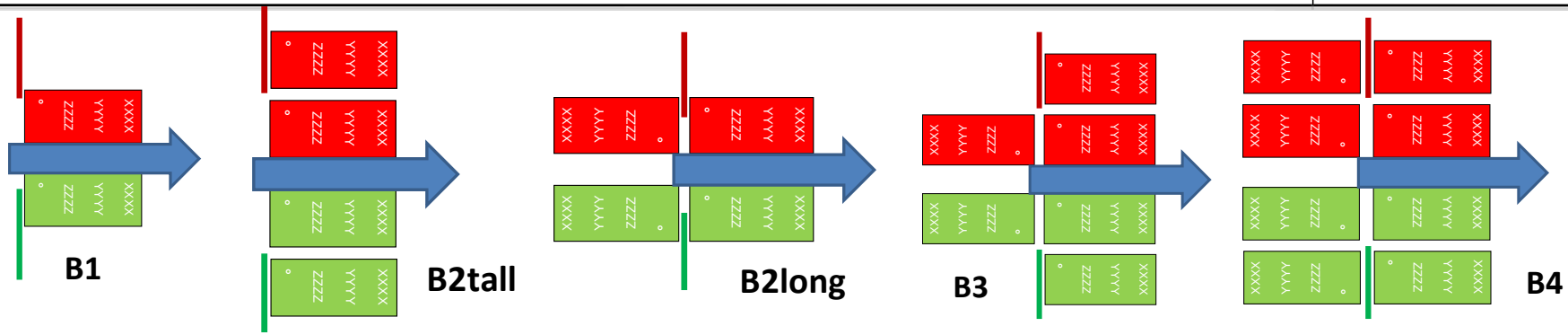


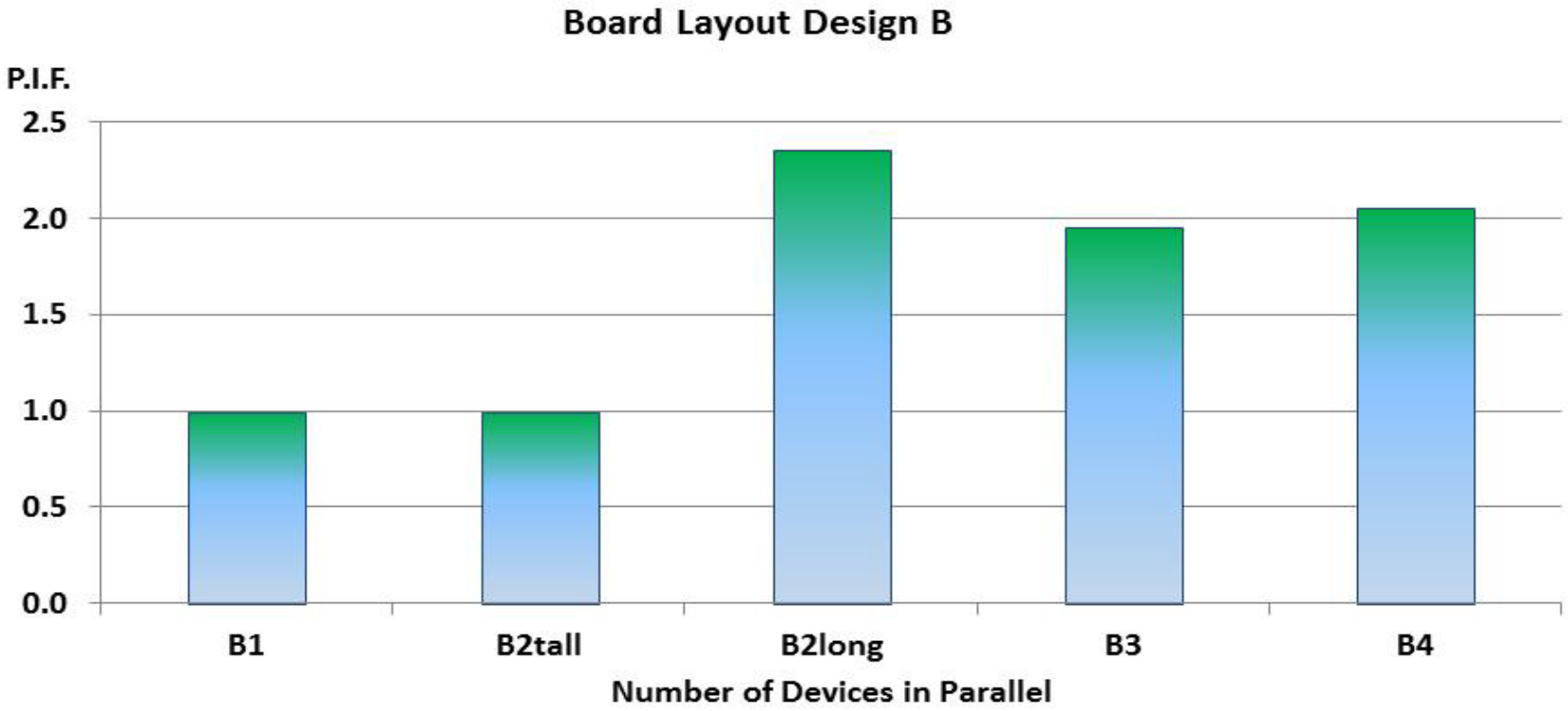
eGaN FET

eGaN FET

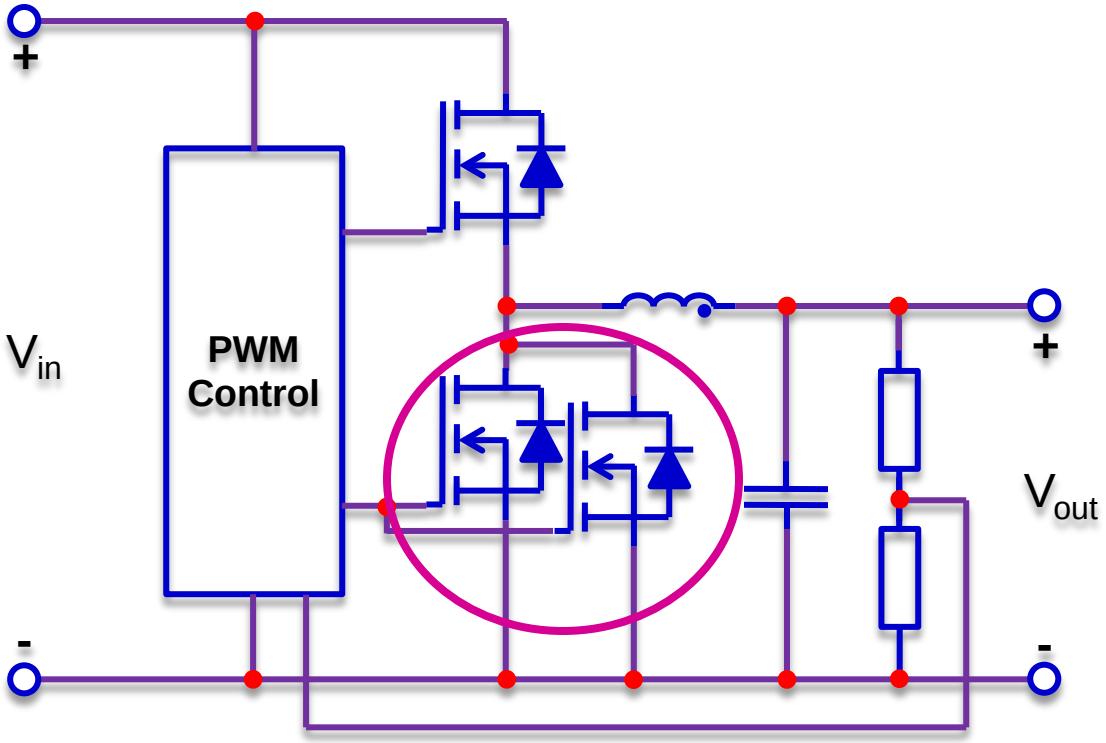
Vias on both sides of the FET. Current exits pad in two directions

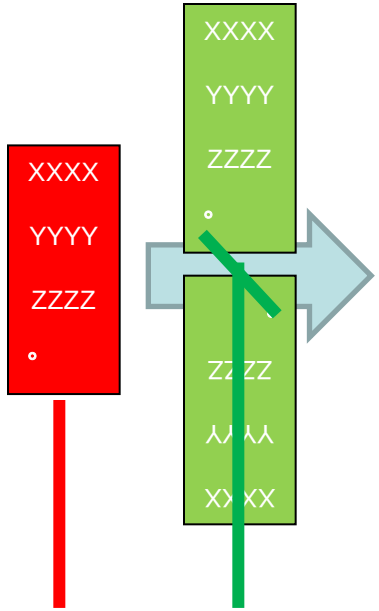
PIF for Best Layout





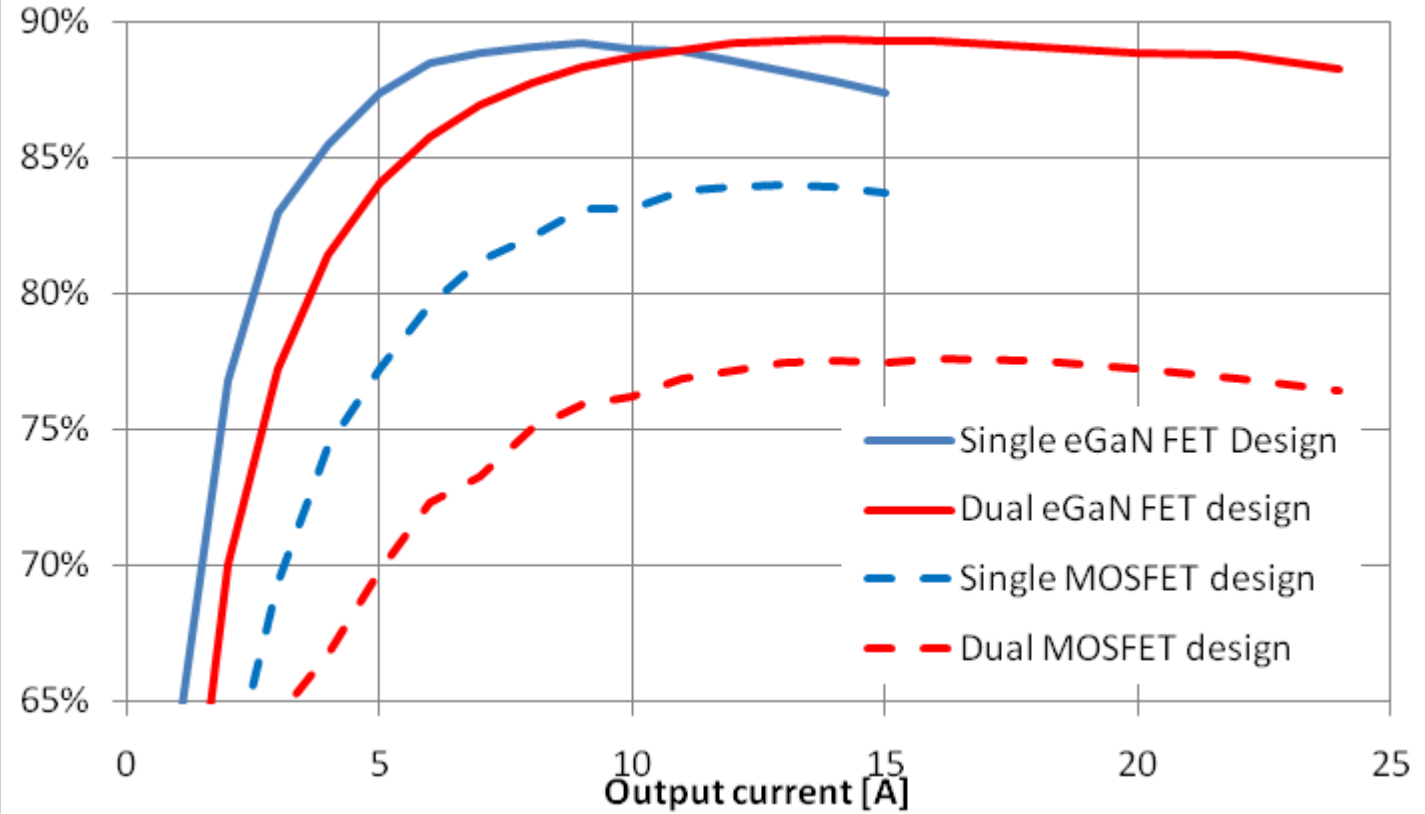
Parallel eGaN FET Buck Converter





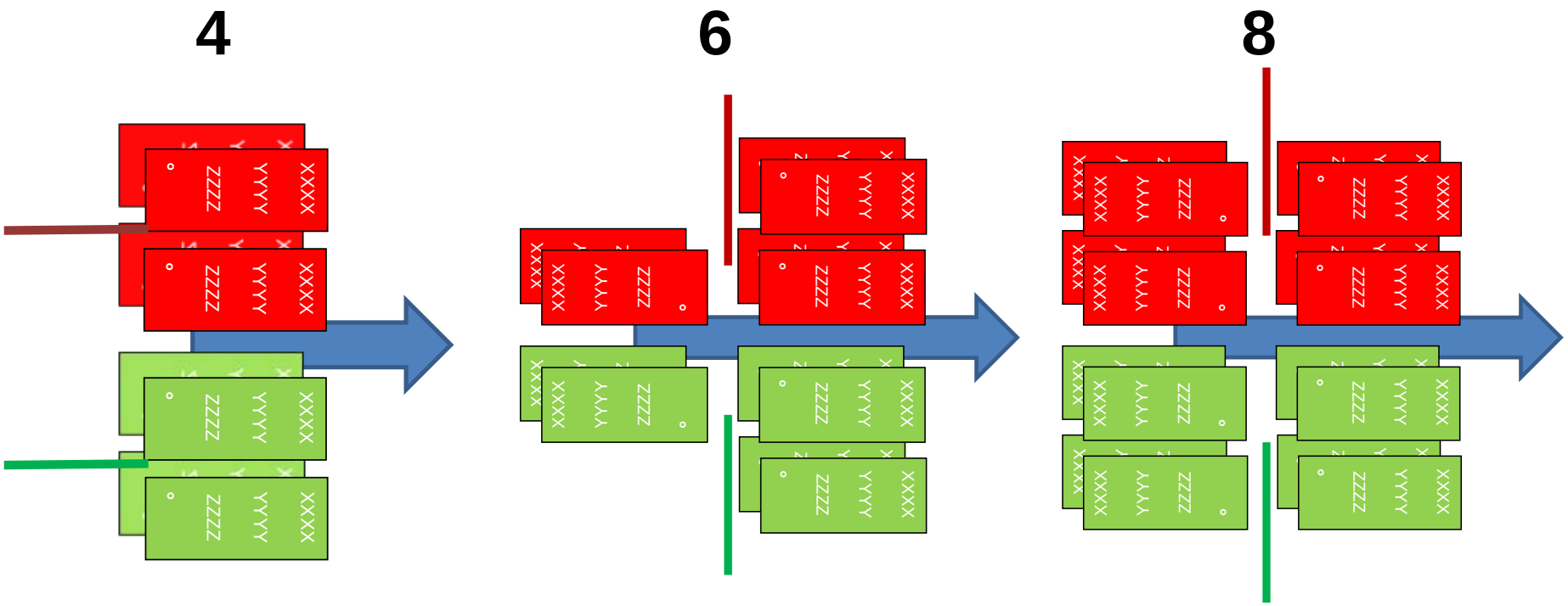
Parallel eGaN® FET Buck Converter

Efficiency at 1 MHz



$12\ V_{IN} – 1.2\ V_{OUT}$

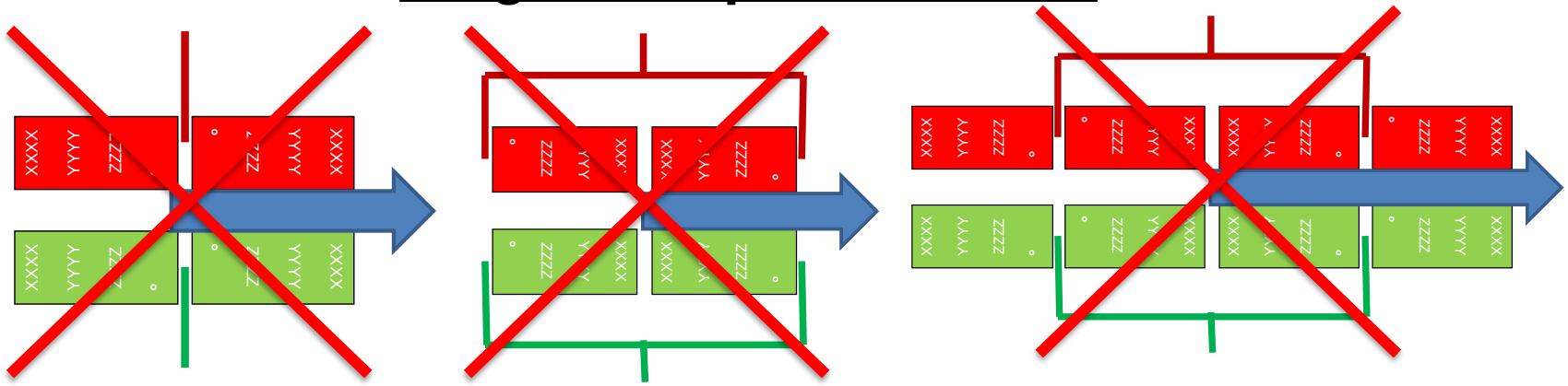
Half Bridge Layout *Best* Practice



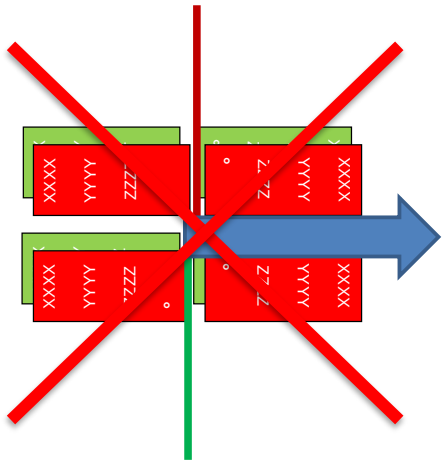
Double Component Sided

Layout *Don'ts*

Single Component Sided



Double Component Sided



Summary

- eGaN FETs can be paralleled
- Two devices can be paralleled without loss of performance
- The PIF is a useful tool for comparing layouts and predicting switching performance

EFFICIENT POWER CONVERSION

The end of the road for silicon…..

is the beginning of the eGaN FET journey!