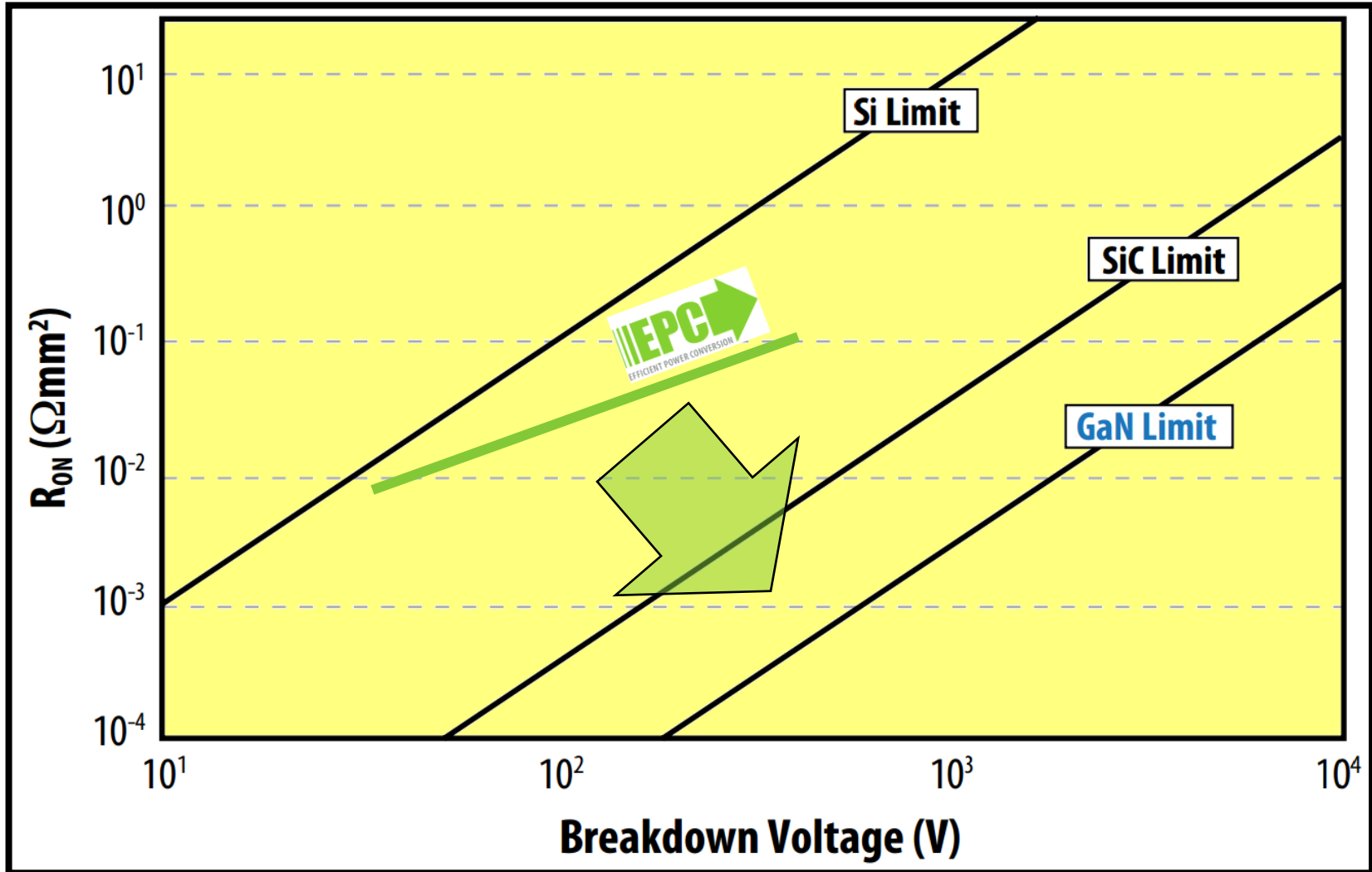


A green rectangular road sign with a white border is mounted on a wooden post. The sign contains the text "The eGaN® FET Journey Continues". The background of the entire slide is a desert landscape with a road leading towards a building at sunset. The sky is blue with white clouds, and the sun is low on the horizon, creating a golden glow. The building in the distance is a multi-story structure with a grid-like facade.

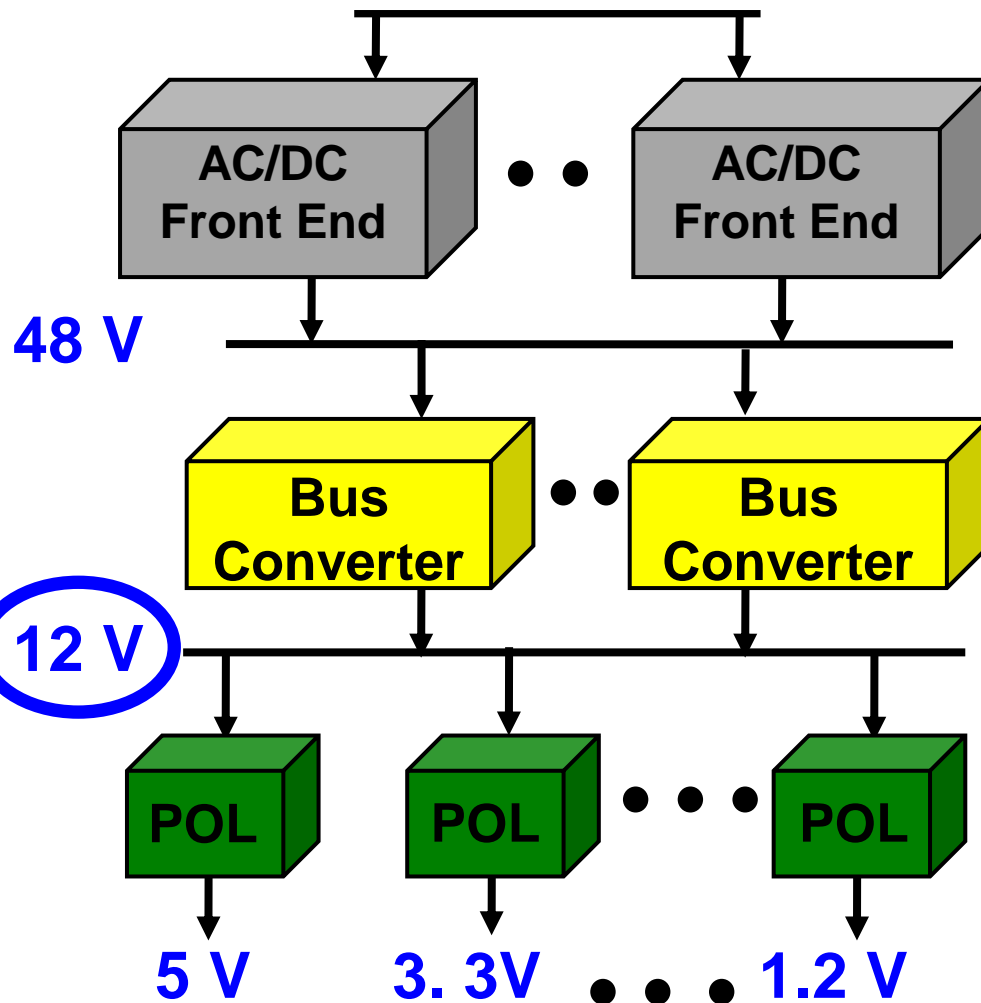
The eGaN® FET  
Journey Continues

# Improving System Performance with eGaN® FETs in DC-DC Applications

David Reusch, Johan Strydom, Alex Lidow  
*Efficient Power Conversion Corporation*

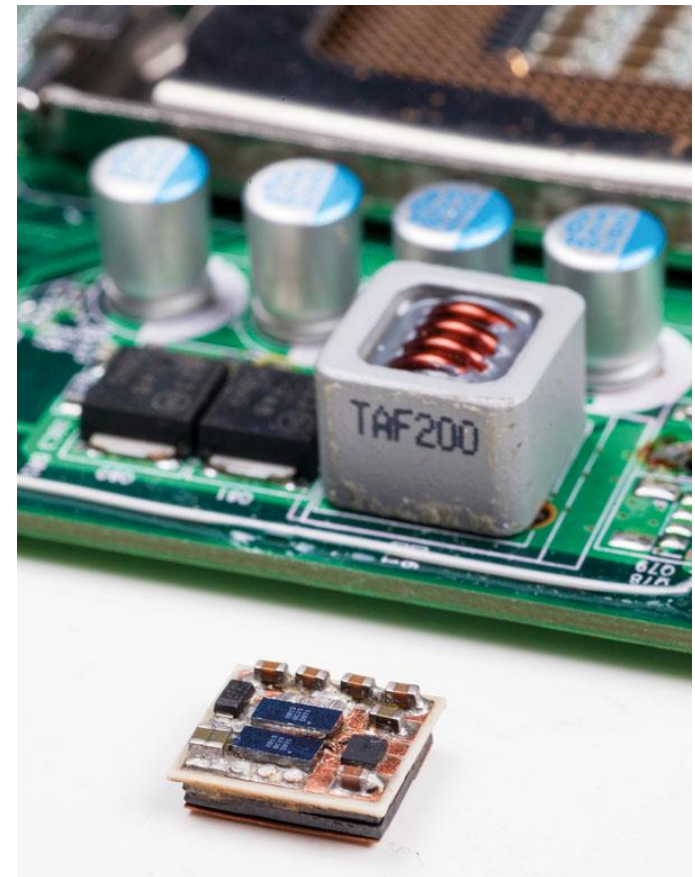


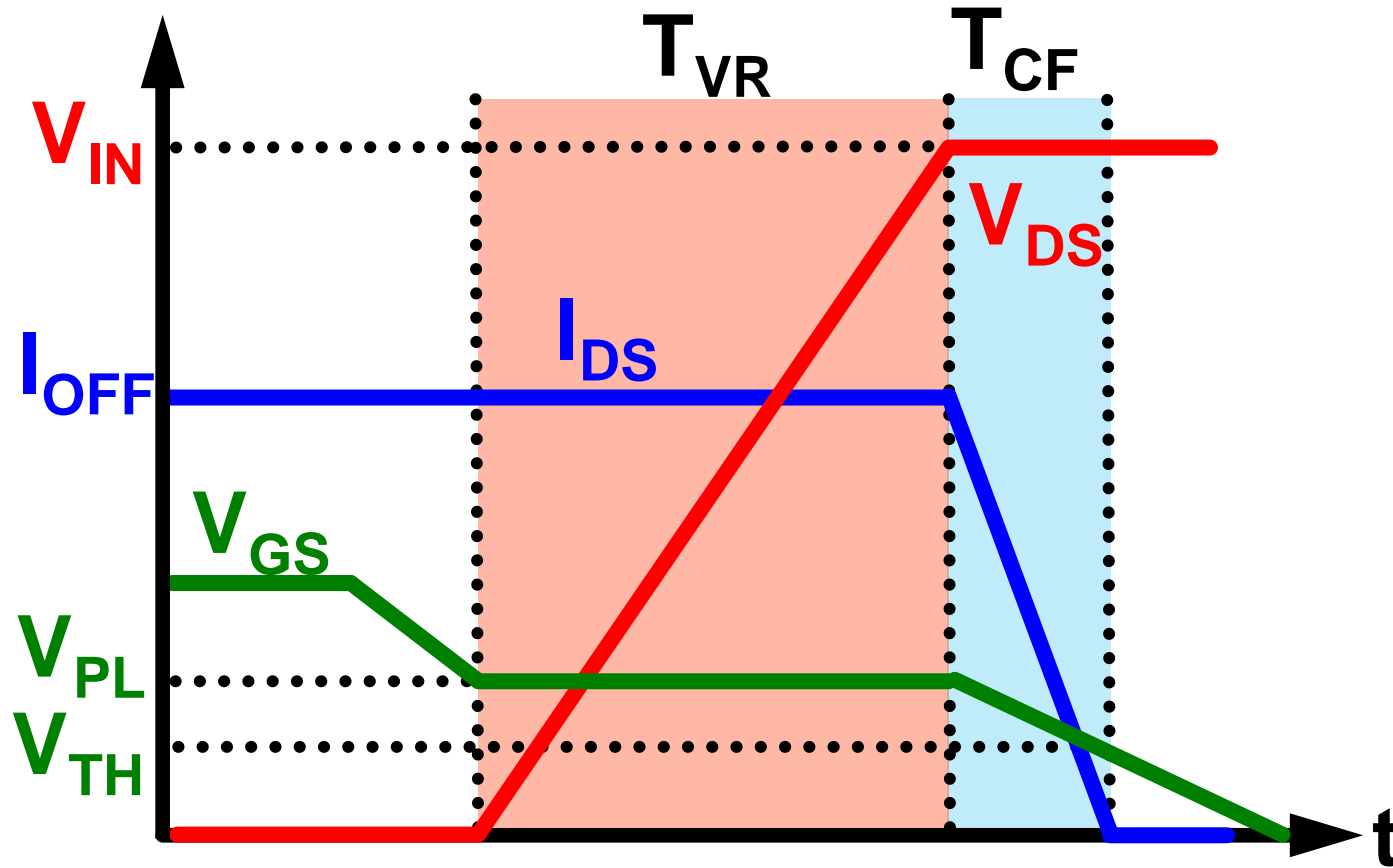
AC input: 90~265 V



## 2MHz GaN Based 12 V 3D POL

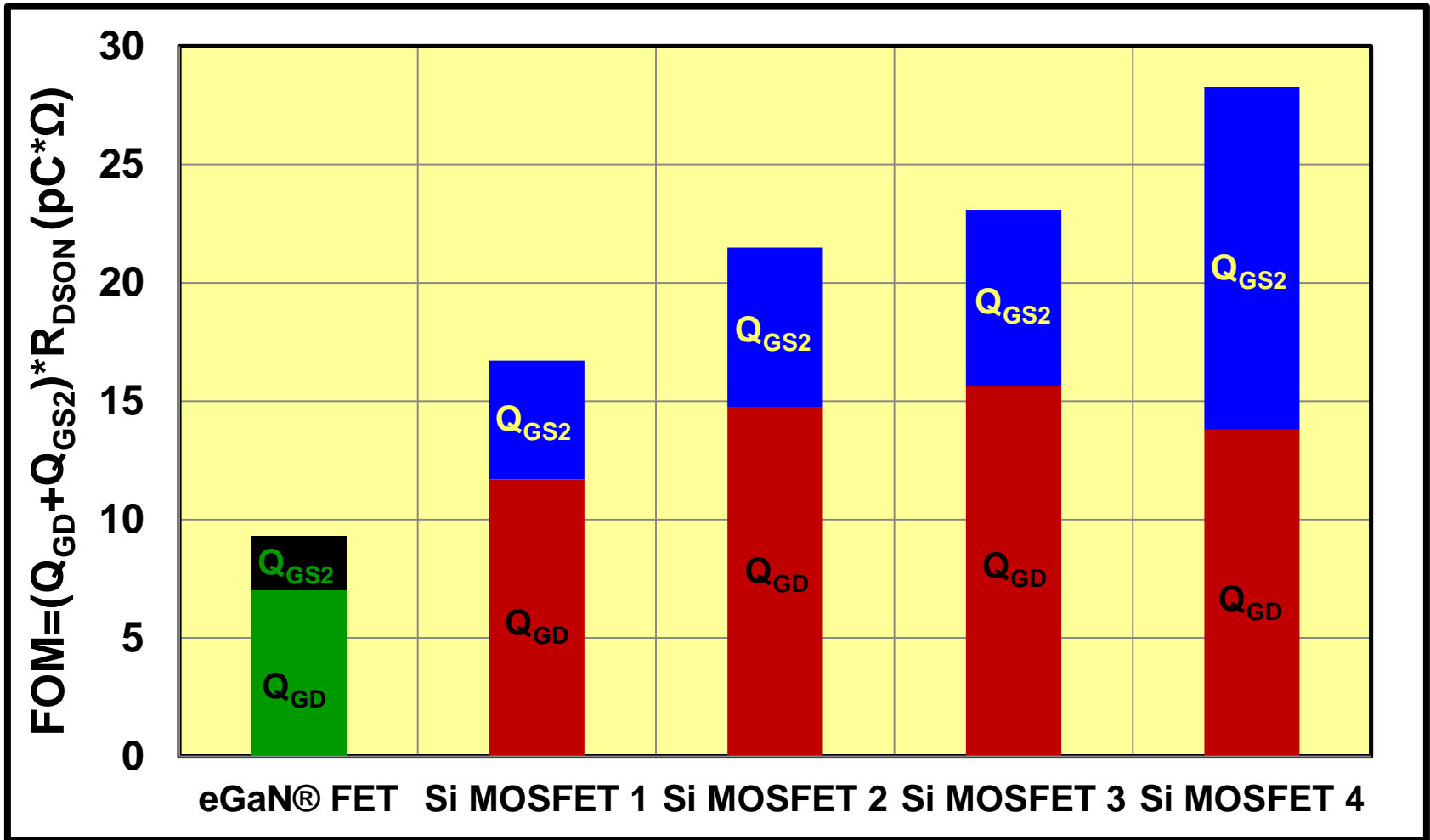
Ref: [ece.vt.edu](http://ece.vt.edu)



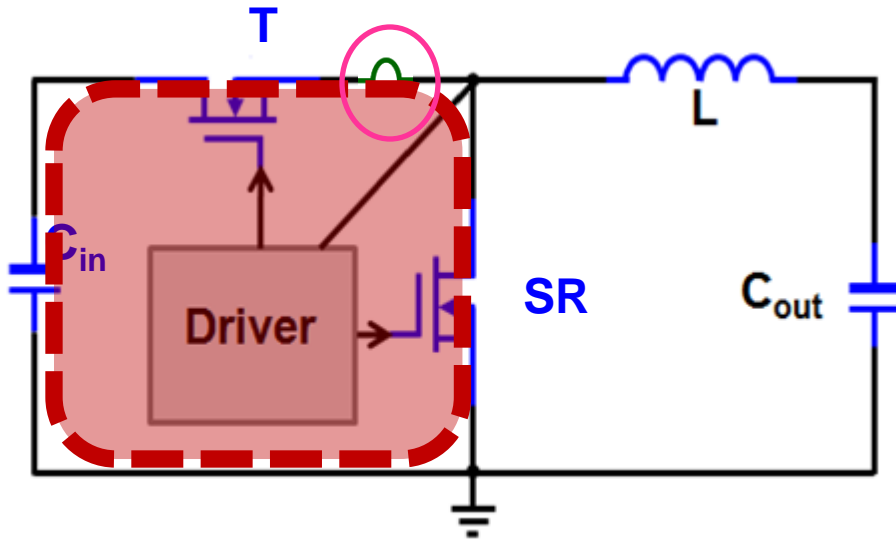


$$P_{T_{VR}} \approx \frac{V_{IN} * I_{OFF} * Q_{GD}}{2 * I_G}$$

$$P_{T_{CFB}} \approx \frac{V_{IN} * I_{OFF} * Q_{GS2}}{2 * I_G}$$

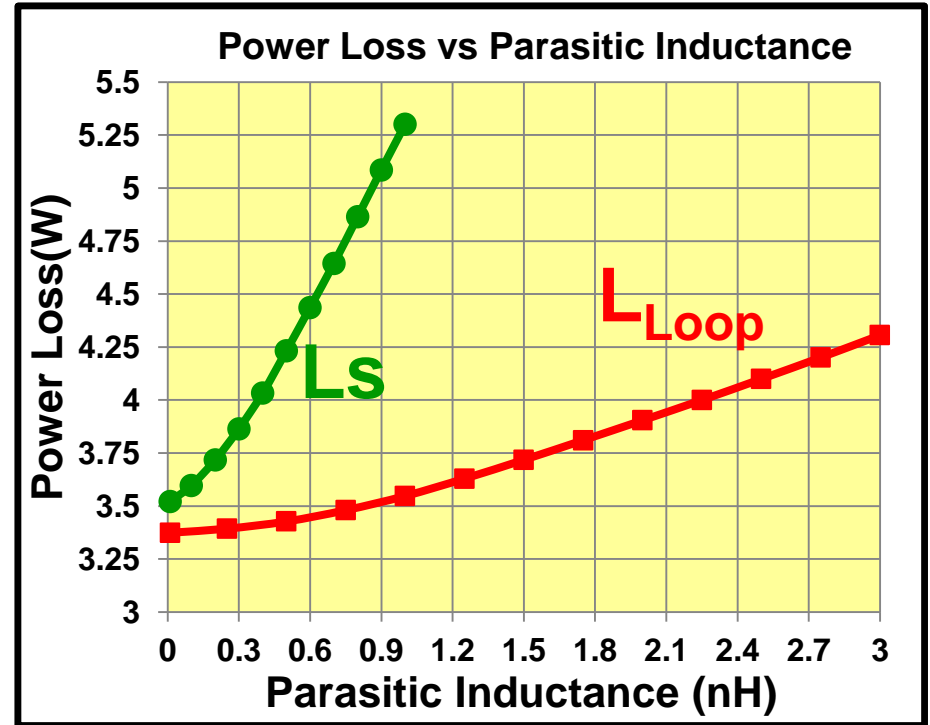


$V_{DS}=20\text{ V}, I_{DS}=20\text{ A}$

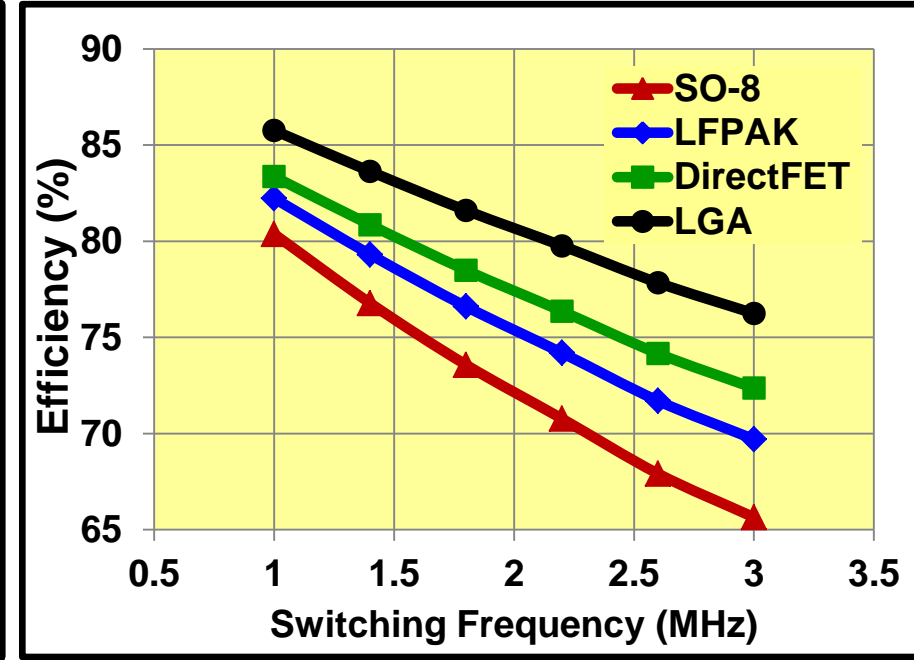
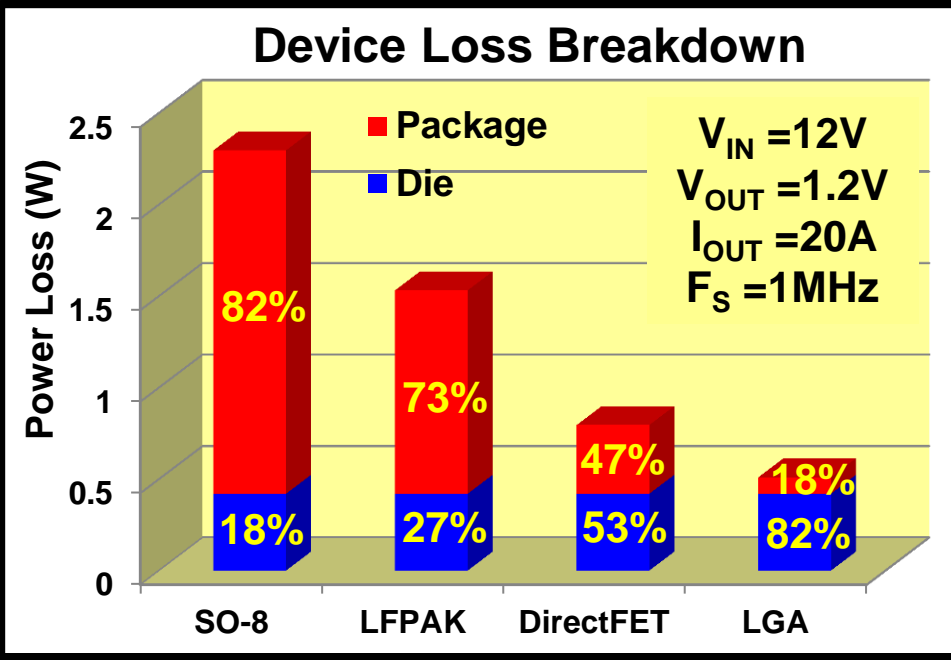
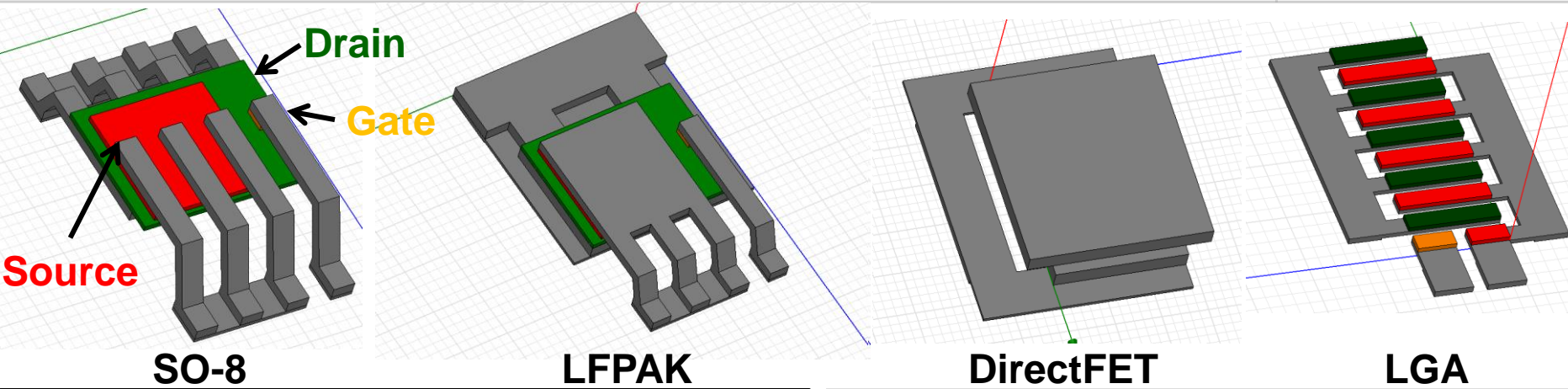


$L_S$ : Common Source Inductance

$L_{Loop}$ : High Frequency Power Loop Inductance

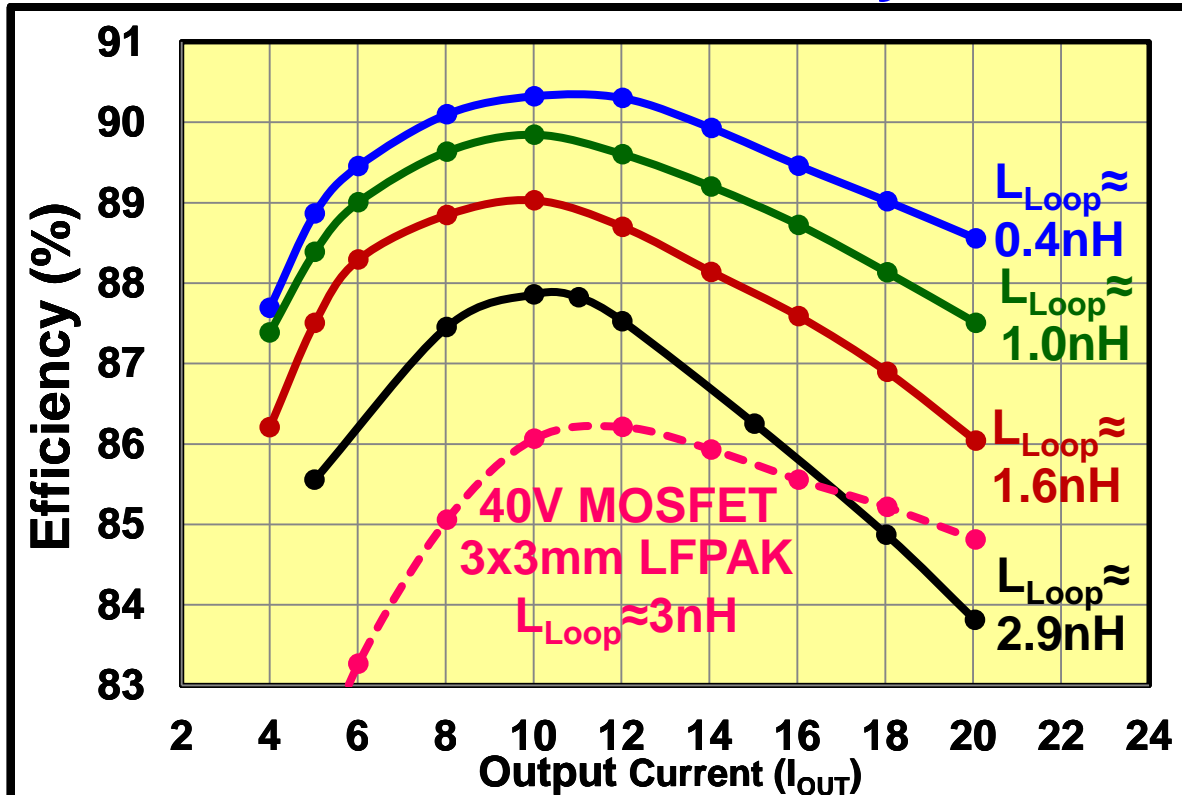


$V_{IN}=12\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  
 $F_S=1\text{ MHz}$ ,  $I_{OUT}=20\text{ A}$





## Measured Efficiency



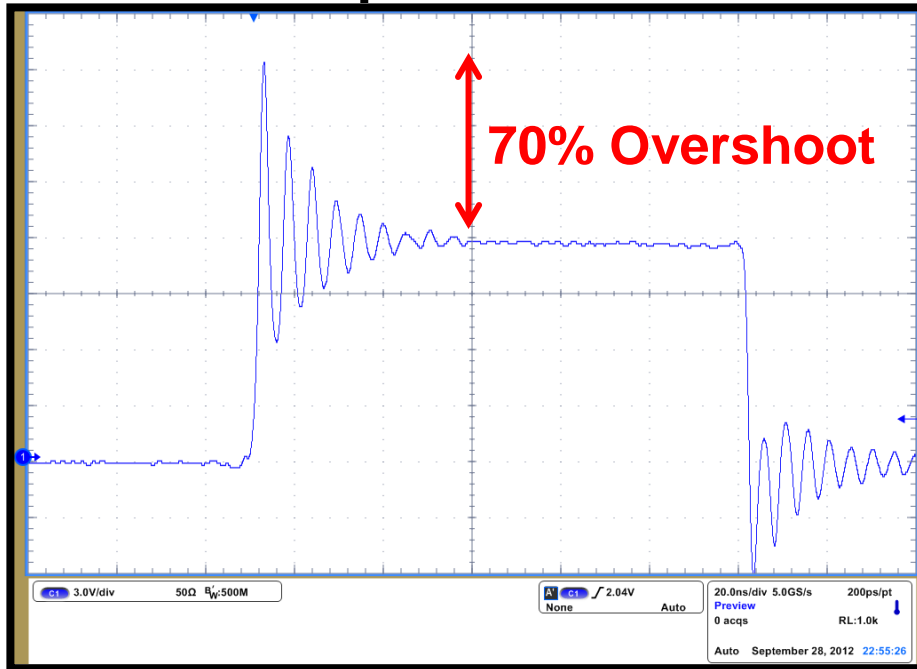
Experimental Prototype  
 $L_{LOOP} \approx 0.4 \text{ nH}$



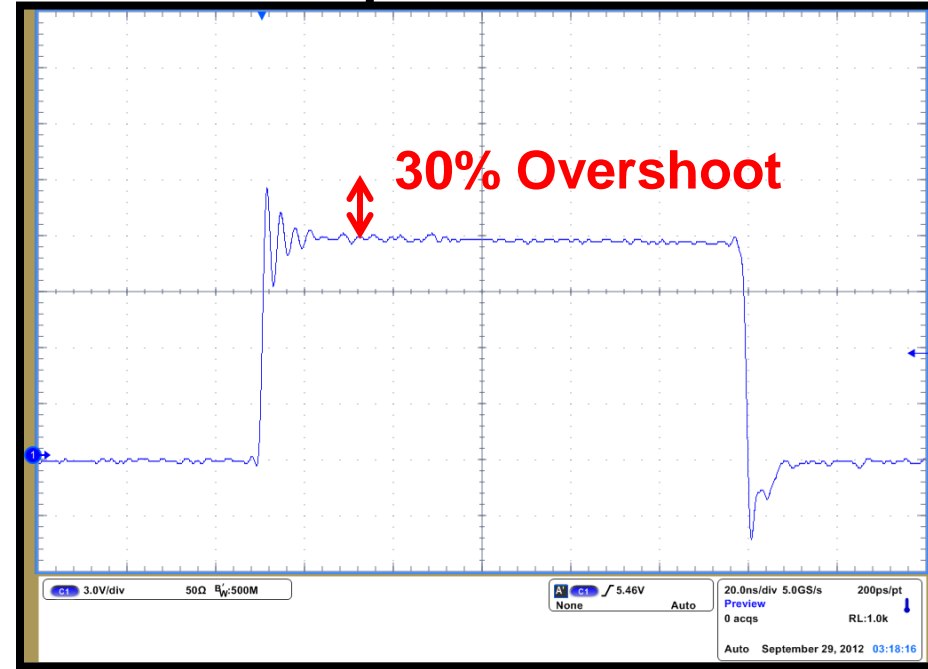
$V_{IN} = 12 \text{ V}$ ,  $V_{OUT} = 1.2 \text{ V}$ ,  
 $F_S = 1 \text{ MHz}$ ,  $L = 150 \text{ nH}$



$L_{Loop} \approx 1.0 \text{ nH}$



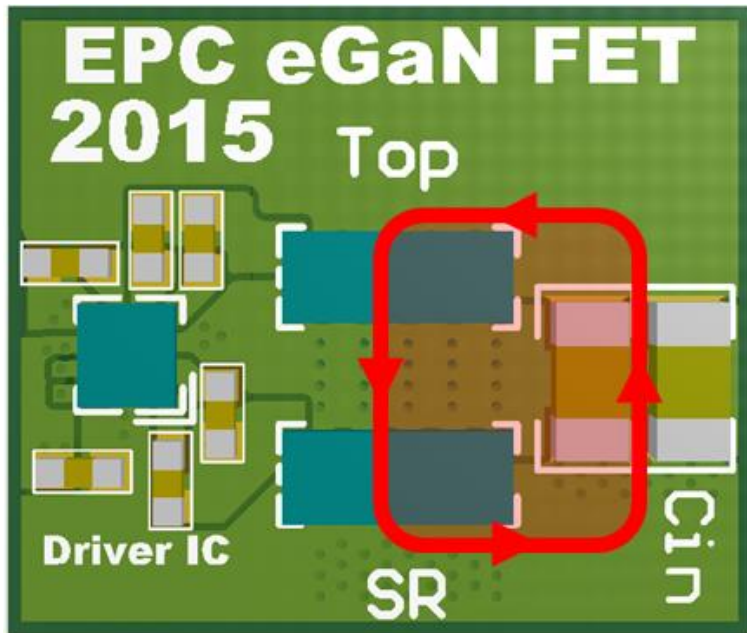
$L_{Loop} \approx 0.4 \text{ nH}$



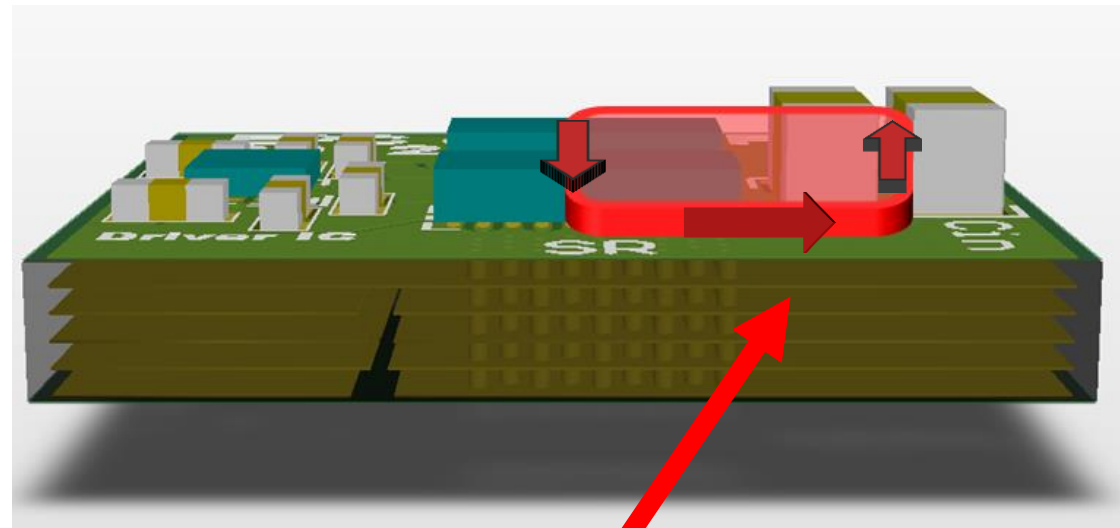
**Switching Node Voltage**

$V_{IN}=12 \text{ V } V_{OUT}=1.2 \text{ V } I_{OUT}=20 \text{ A}$   
 $F_S=1 \text{ MHz } L=150 \text{ nH}$

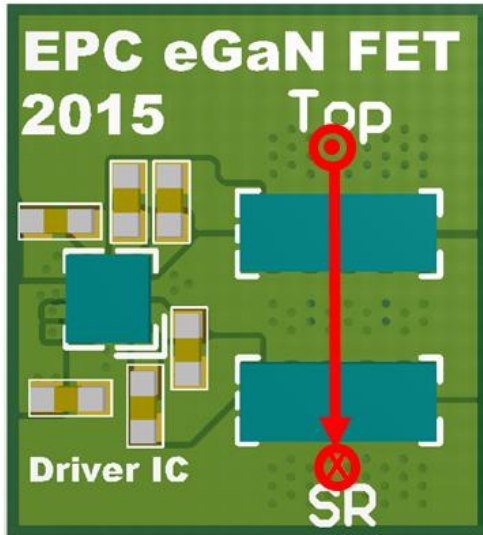
## Top View



## Side View

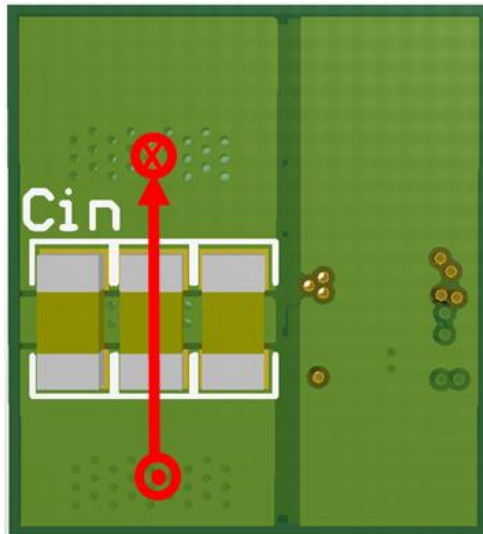
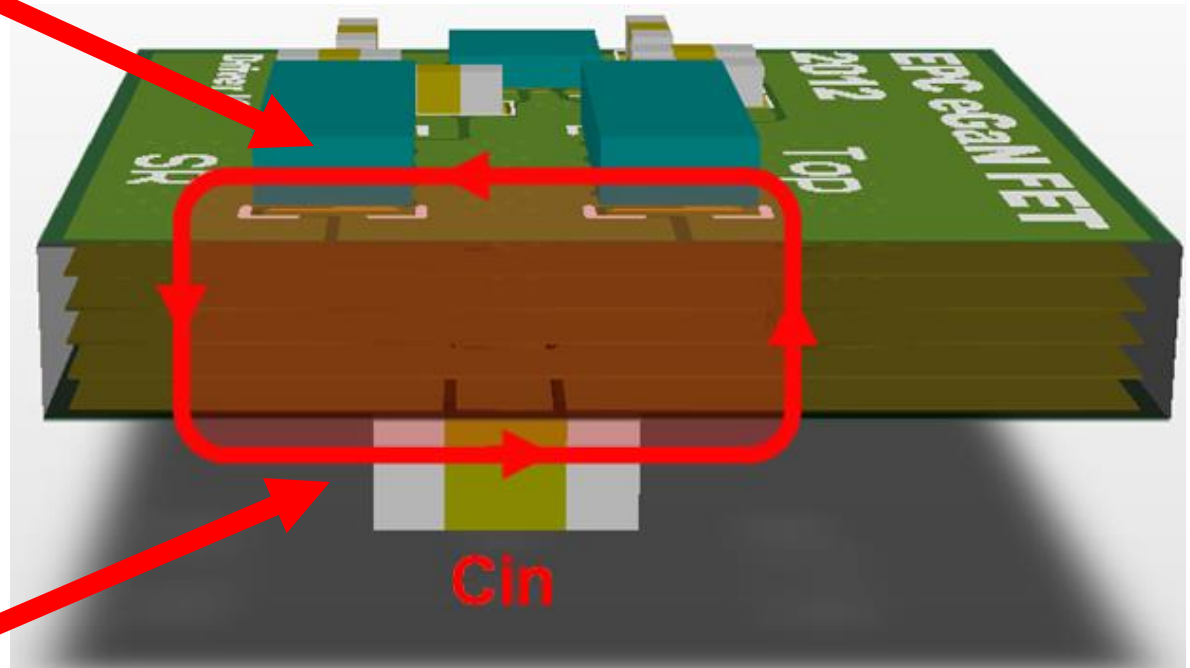


**Shield Layer**

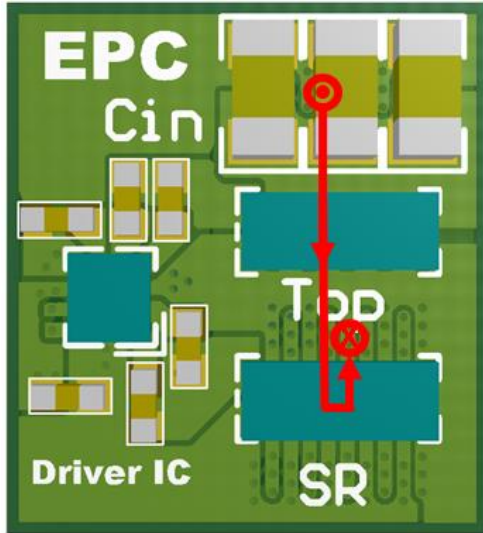


**Top View**

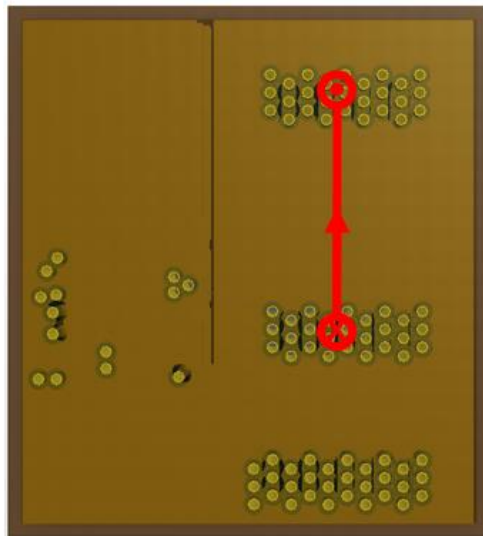
**Side View**



**Bottom View**

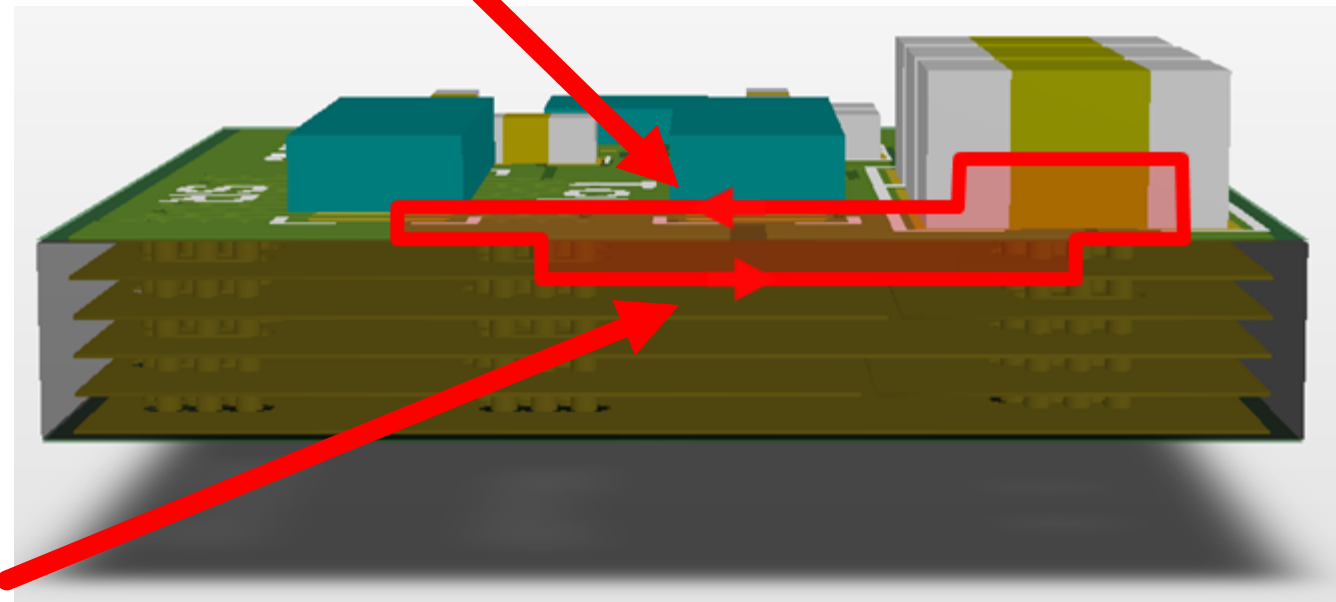


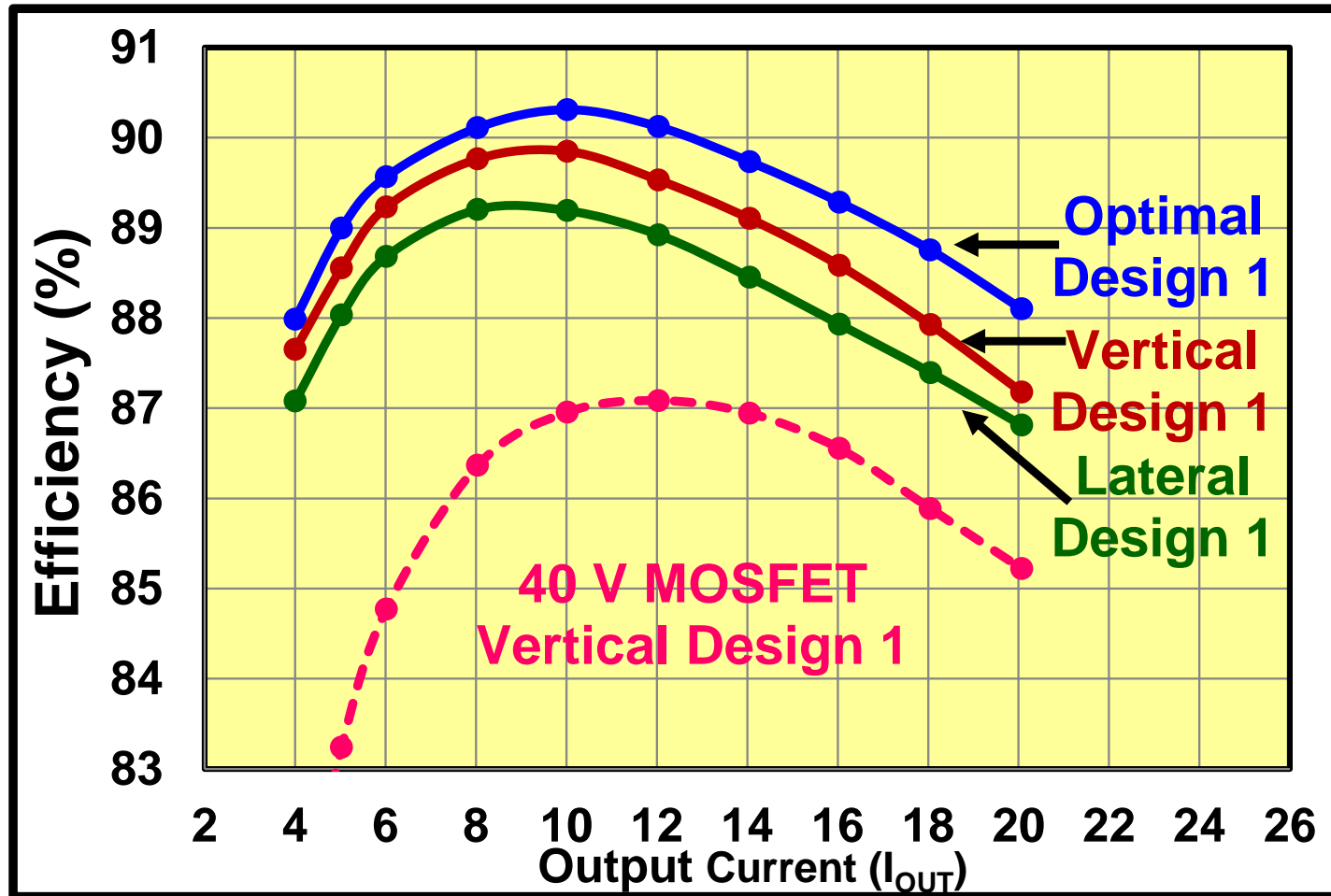
Top View



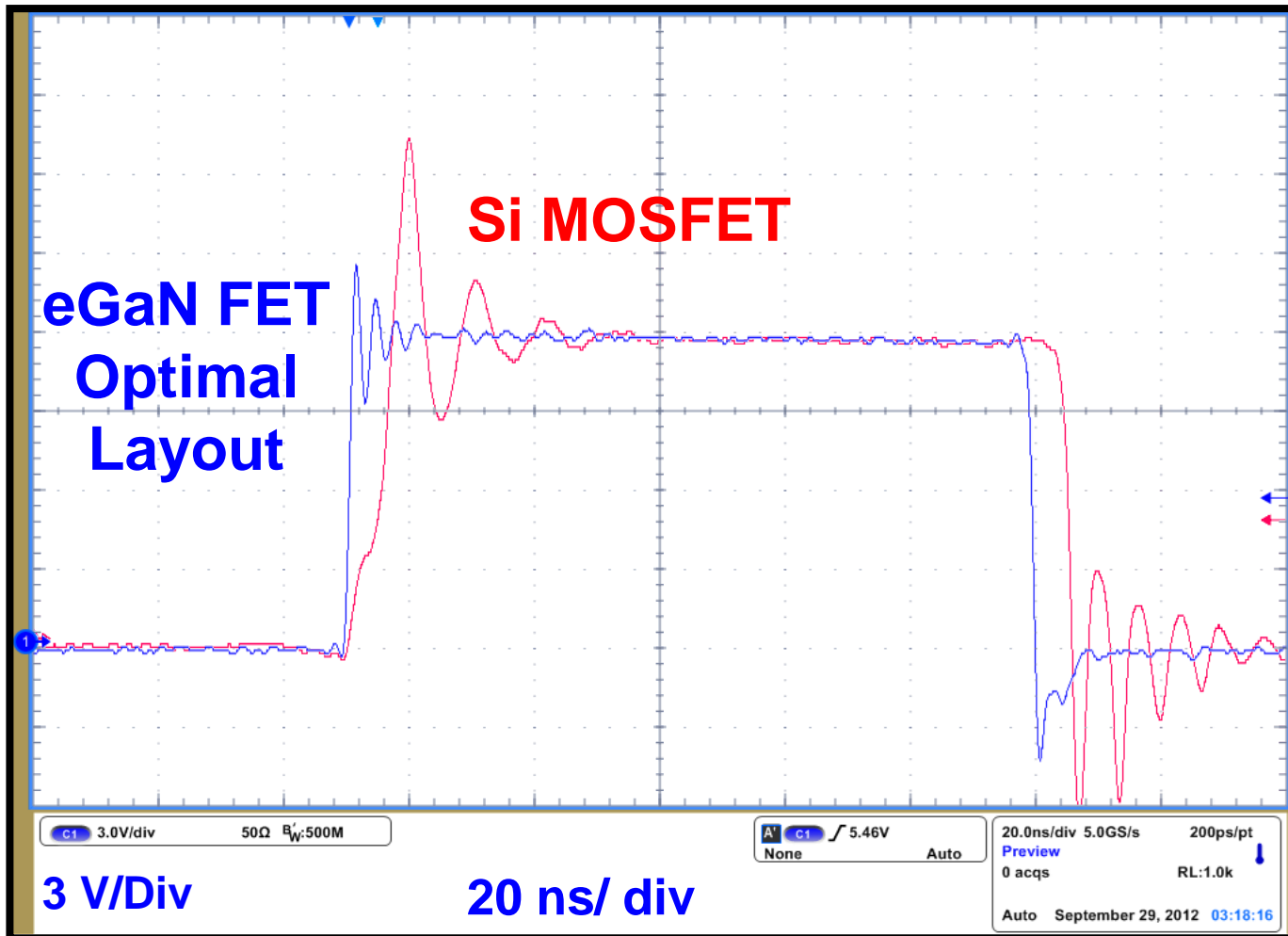
Top View  
Inner Layer 1

Side View

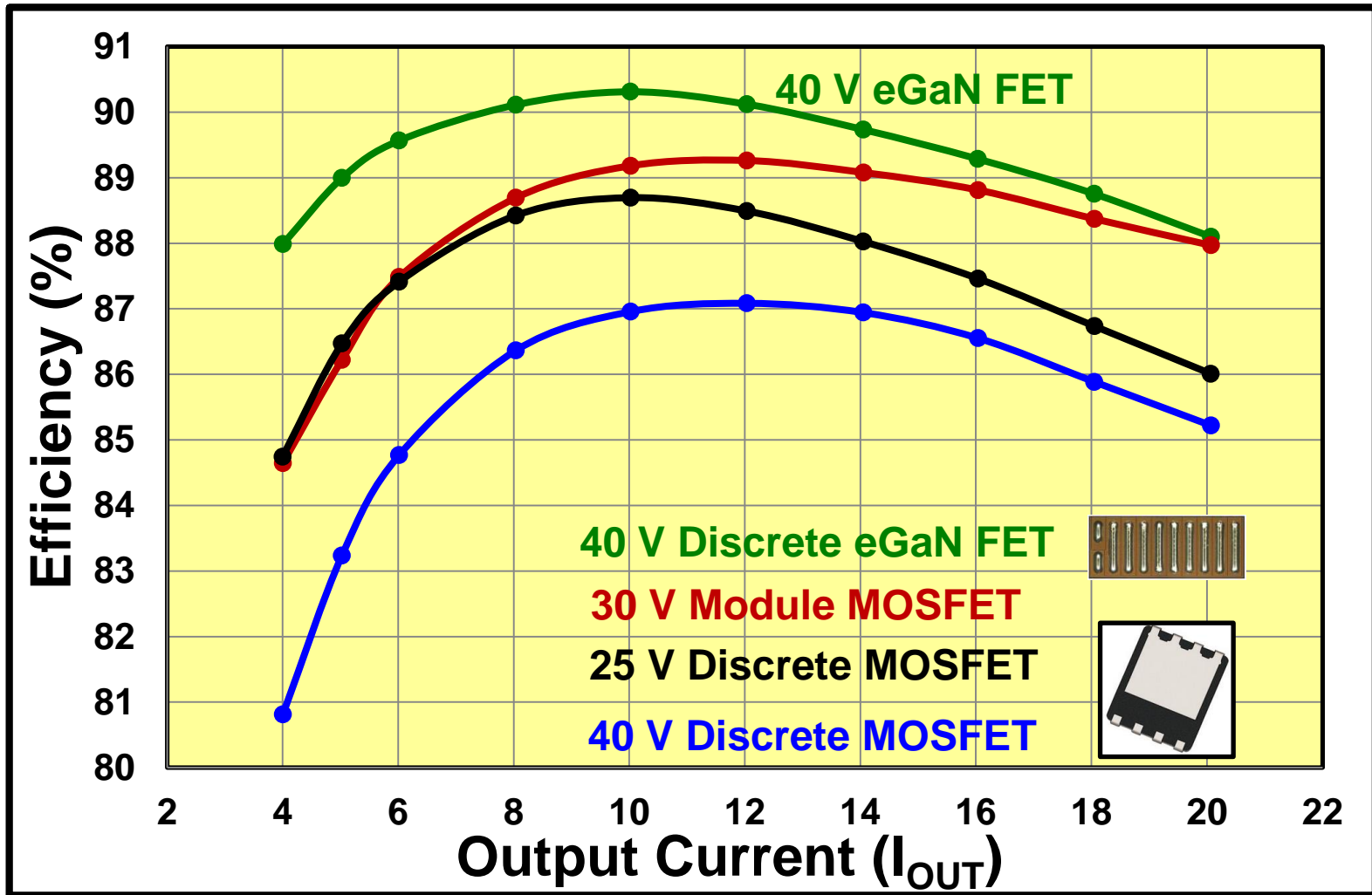




$V_{IN}=12\text{ V}$   $V_{OUT}=1.2\text{ V}$   $F_s=1\text{ MHz}$   $L=300\text{ nH}$   
 GaN T/SR: EPC2015 Driver LM5113

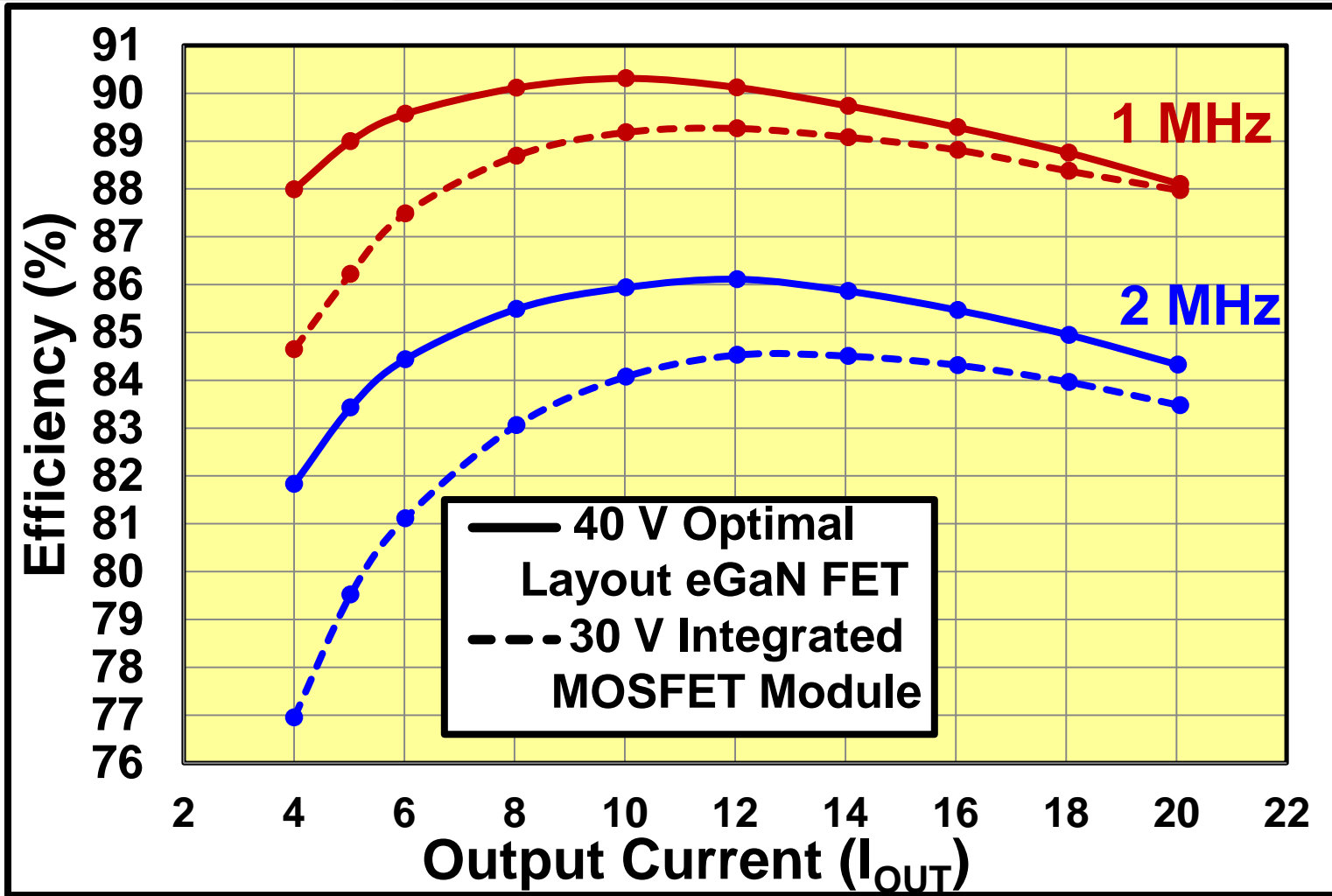


$V_{IN}=12\text{ V}$   $V_{OUT}=1.2\text{ V}$   $I_{OUT}=20\text{ A}$   $F_S=1\text{ MHz}$   $L=300\text{ nH}$  eGaN FET  
T/SR: EPC2015 MOSFET T:BSZ097N04 SR:BSZ040N04

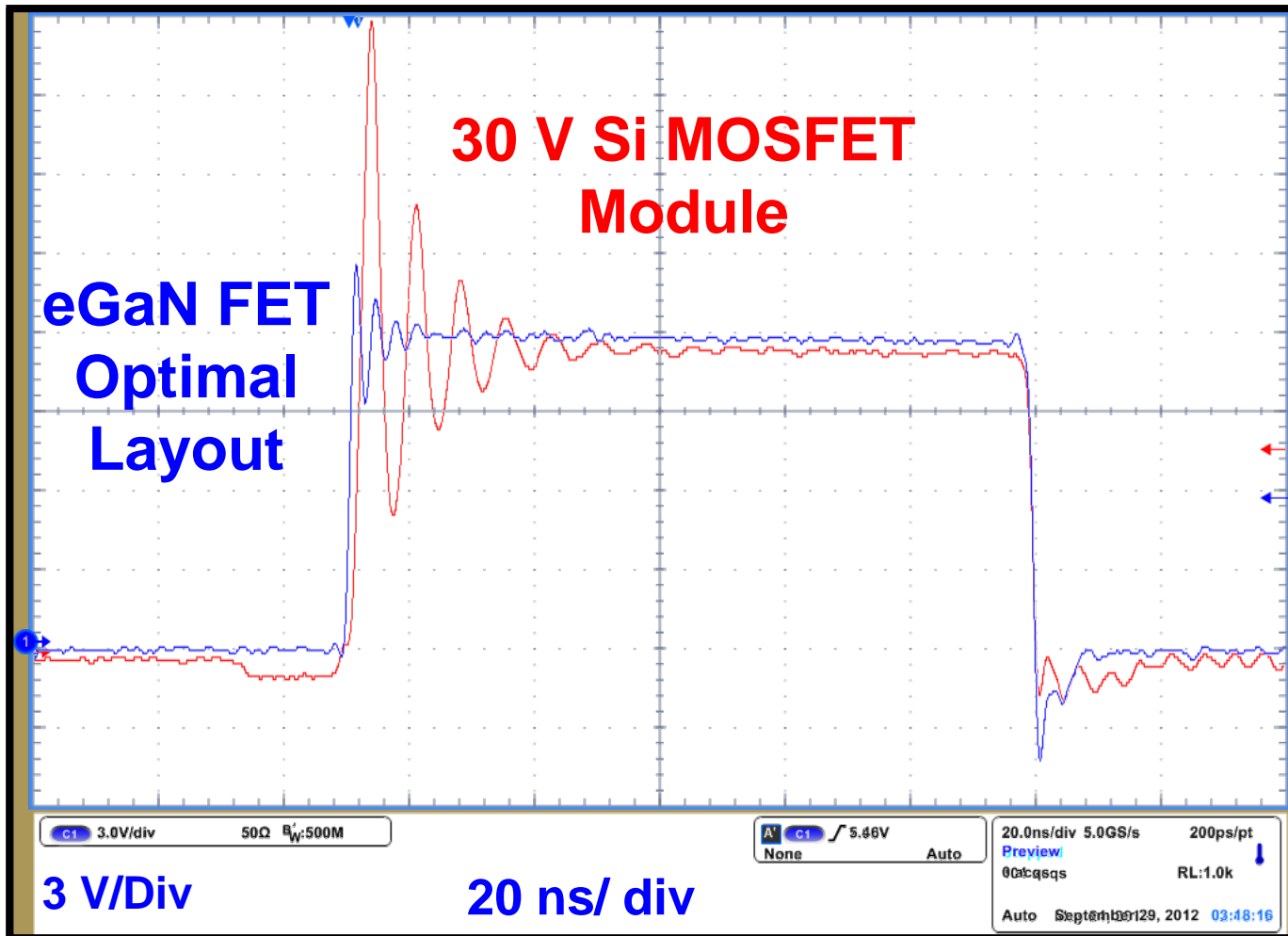


$V_{IN}=12\text{ V}$   $V_{OUT}=1.2\text{ V}$   $F_S=1\text{ MHz}$   $L=300\text{ nH}$





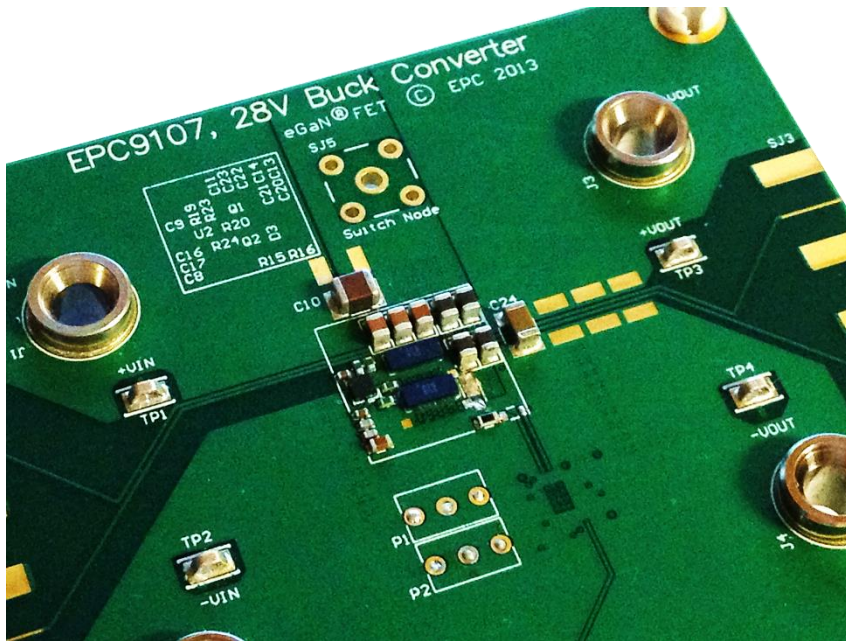
$V_{IN}=12\text{ V}$   $V_{OUT}=1.2\text{ V}$   $L=300\text{ nH}$



**$V_{IN}=12\text{ V}$   $V_{OUT}=1.2\text{ V}$   $I_{OUT}=20\text{ A}$   $F_S=1\text{ MHz}$   $L=300\text{ nH}$  eGaN FET  
T/SR: EPC2015 MOSFET Module: CSD97370Q5M**



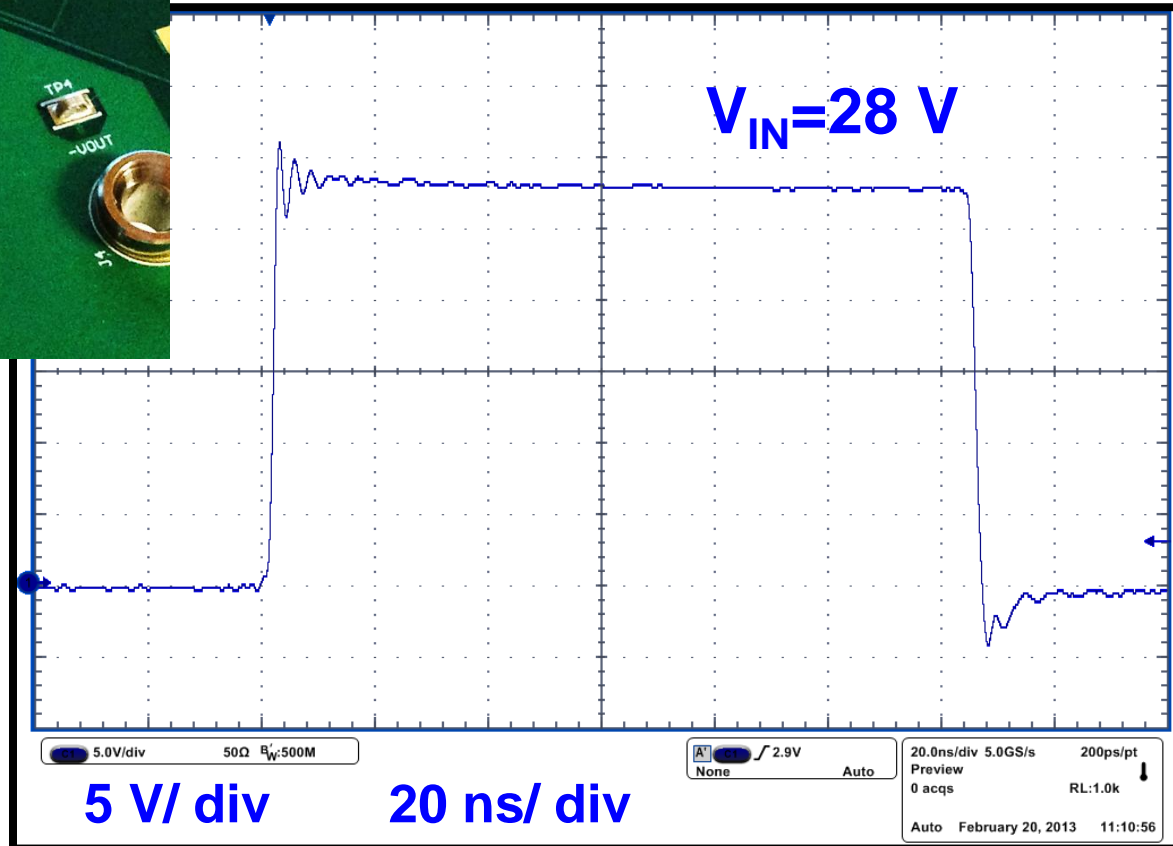
# EPC9107 Demonstration Board



$V_{IN}=12-28\text{ V}$     $V_{OUT}=3.3\text{ V}$   
 $I_{OUT}=15\text{ A}$     $F_S=1\text{ MHz}$   
2 x EPC2015

## Switching Node Voltage

$V_{IN}=28\text{ V}$     $I_{OUT}=15\text{ A}$



## eGaN FETs improve performance in high switching frequency converters:

- **Lower FOM  $(Q_{GD}+Q_{GS2}) * R_{DSON}$**
- **Lower Package Parasitics**
- **PCB Layout Limits Performance**
- **Optimizing Layout Enhances Performance**

Thank you for  
your time!  
Questions?



*The end of the road  
for silicon.....*

*is the beginning of  
the eGaN FET  
journey!*

**David.Reusch@epc-co.com**