

Product / Process Change Notification (PCN)

909 N Pacific Coast Highway, Suite 230, El Segundo, CA 90245

Notification Date: July 10, 2025

PCN Number: PCN250402

PCN Title: Manufacturing Site, Wafer Size and Process Flow Change

Product Identification:

EPC2619

Description of Change:

EPC announces the qualification EPC2619 from 6-inch platform at Episil to the 8-inch platform at Vanguard (VIS). This change includes a manufacturing site and process flow change. There will be no change to the package dimensions. Changes to the datasheet are as noted below.

Successful qualification testing was performed to ensure product quality and reliability requirements are met or exceeded.

EPC will begin production of devices using substrates from VIS for the EPC2619 starting with date code DC 2529

Process Flow Comparison:

Stage	6 inch Vendor	6 inch Process	8 inch Vendor	8 inch Process
Fab	Episil	Epi Episil Precision	VIS	Epi Episil Precision, different recipe
		Platform 2		Platform 2 VIS flow
		PCM		PCM
		Grind/stress relief etch		
		Sample probe 025C/150C		
		•		·
Bump	Raytek	6 inch bump	Raytek	8 inch bump
Final Probe	MSEC	6 inch probe	MSEC	8 inch probe
WLCSP TNR	ADT	Laser mark	ADT	Grind (no stress relief etch)
		WLCSP/TNR 6 inch		Laser mark
				WLCSP/TNR 8 inch

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Datasheet Comparison:

■ 8-inch EPC2619 has lower capacitance and charge than 6-inch EPC2619.

> C_{ISS}: 1106 pF vs 1180 pF

➤ C_{RSS}: 4 pF vs 3 pF

➤ Coss: 338 pF vs 350 pF

➤ Q_G: 8 nC vs 8.5 nC

EPC2619 8-inch EPC2619 6-inch ic Characteristics (VIS) TEST CONDITIONS MAX UNIT TYP MAX UNIT Input Capacitance 1106 1234 1180 1570 Reverse Transfer Capacitance V_{DS} = 50 V, V_{GS} = 0 V CRSS Reverse Transfer Capacitance $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$ 3.0 Output Capacitance 410 338 Coss Output Capacitance 350 Output Capacitance Effective Output Capacitance, Energy Related (Note 1) Effective Output Capacitance, Time Related (Note 2) Gate Resistance 400 Effective Output Capacitance, Energy Related (Note 2) 400 $V_{DS} = 0$ to 50 V, $V_{GS} = 0$ V $V_{DS} = 0$ to 50 V, $V_{GS} = 0$ V Effective Output Capacitance, Time Related (Note 3) 530 530 Gate Resistance 0.4 Ω Total Gate Charge $V_{DS} = 50 \text{ V}, V_{GS} = 5 \text{ V}, I_D = 16 \text{ A}$ 8.5 Total Gate Charge V_{DS} = 50 V, V_{GS} = 5 V, I_D = 16 A 9.2 QGS Gate-to-Source Charge 2.2 Gate to Source Charge Gate to Drain Charge Gate-to-Drain Charge $V_{DS} = 50 \text{ V}, I_D = 16 \text{ A}$ 1.0 QGD V_{DS} = 50 V, I_D = 16 A Gate Charge at Threshold 1.6 Gate Charge at Threshold Output Charge Qoss $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$ Output Charge $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$ 27 Source-Drain Recovery Charge Source-Drain Recovery Charge

Qualification Report

Available upon request.

Last Time Buy:

N/A

Samples

Contact EPC if samples or additional information is required.

Information Request

If there are any questions, comments or information required regarding this PCN please contact your local EPC Sales Representative

EPC CONSIDERS THIS CHANGE APPROVED IF WE DO NOT RECEIVE ANY WRITTEN OBJECTION WITHIN 30 DAYS FROM NOTIFICATION DATE OF THIS PCN LETTER.

EPC Approval:

This PCN has been reviewed and approved by EPC's Quality & Reliability department:

Quality Vice President:	Yanping Ma	
Date:	July 10, 2025	

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