EPC eGaN® FET Qualification Report EPC2057

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This report summarizes the Product Qualification results for EPC part number EPC2057. The EPC2057 meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification of EPC2057, a 50 V wafer level chip scale package (WLCSP) eGaN power transistor.

Part Number	Voltage (V)	$R_{DS(on)}$ (mΩ)	Die Size (mm x mm)	Maximum Operating Temperature (°C)
EPC2057	50	8.5	S (1.2 x 1.5)	150

Qualification Test Overview

EPC's eGaN transistors were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to an 80% of the maximum rated drain-source voltage at the maximum rated temperature (150°C).
- High temperature gate bias (HTGB): Parts are subjected to the maximum rated gate-source voltage (6 V) at the maximum rated temperature (150°C).
- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1); (3) 3 times reflow.
- Biased highly accelerated test (bHAST): Parts are soaked for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia with a constant drain-source voltage (40 V).
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -40°C to 125°C for a total of 1000 cycles.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.

The stability of the devices is verified with DC electrical tests after reliability stressing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) JESD47L[1] standard.

Parts for all tests were mounted onto high Tg FR4 adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers (1 oz. Cu per layer) were used. Kester WP616 type 4 SAC305 solder with no clean flux was used for mounting the parts onto an adaptor card.

[1] JEDEC standard, JESD47L, "Stress-Test-Driven Qualification of Integrated Circuits", DECEMBER 2022

High Temperature Reverse Bias

Parts from three lots were subjected to 80% of the maximum rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTRB	**EPC2057**	S (1.2 x 1.5)	T = 150°C, V_{DS} = 40 V	0	77 x 3	1000

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts from three lots were subjected to the maximum rated gate-source voltage at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTGB	**EPC2057**	S (1.2 x 1.5)	T = 150°C, V_{GS} = 6 V	0	77 x 3	1000

Table 2. High Temperature Gate Bias Test

Biased Highly Accelerated Test

Parts were subjected to 80% of the maximum rated drain-source voltage at a temperature of 130°C, with a relative humidity (RH) of 85%, and vapor pressure (VP) of 33.3 psia for a stress period of 96 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
bHAST	**EPC2057**	S (1.2 x 1.5)	T=130°C, RH = 85%, VP = 33.3 psia, V_{DS} = 40 V	0	77 x 3	96

Table 3. High Temperature Storage Test

Moisture Sensitivity Level

Parts from three lots were subjected to 85% RH at 85°C for a stress period of 168 hours (as defined by J-STD-020F for MSL1 products). The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	**EPC2057**	S (1.2 x 1.5)	T = 85°C, RH = 85%, 3X reflow	0	77 x 3	168

Table 4. High Temperature High Humidity Reverse Bias Test

Temperature Cycling

Parts mounted on FR4 test coupons from three lots were subjected to temperature cycling between -40°C and +125°C. A ramp rate of 15°C/min and dwell times of 5 minutes was used in accordance with the JEDEC Standard JESD22A104[2]. All parts went through pre-conditioning prior to TC.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cys)
TC	**EPC2057**	S (1.2 x 1.5)	-40 to +125°C, Air	0	77 x 1	1000

Table 4. Temperature Cycling Test

[2]JEDEC standard, JESD22-A104, "Temperature cycling", November 2020

Electrostatic Discharge (ESD) Sensitivity Testing

Parts were tested for ESD sensitivity using the human body model (HBM) according to JEDEC JS-001-2023[3] for HBM. EPC2057 passed HBM with a rating of 250 V.

As per JEDEC standard JS-002-2022[4], CDM rating is dependent upon the die size. Due to the small die size of EPC2057, EPC2057 should have a CDM rating of 1000 V by matrix[5].

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	**EPC2057**	S (1.2 x 1.5)	250 V	0	3 x 1

Table 6. ESD HBM and CDM Tests

[3] JS-001-2023, "Human Body Model (HBM) Component Level", July 2023
[4] JS-002-2022, ""Charged Device Model Testing of Integrated Circuits", December 2022
[5] EPC2218A Qualification Report, "https://epc-co.com/epc/Portals/0/epc/documents/reports/qualification/QR-EPC2218A.pdf"