

EPC eGaN[®] FET

Qualification Report

EPC2152



Dr. Shengke Zhang, VP of Reliability, Efficient Power Conversion Corporation

This report summarizes the Product Qualification results for EPC part number EPC2152 which meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification tests performed on EPC2152 for the component-level qualification. EPC2152 is an 80 V, 15 A, 5 V logic, single chip driver with eGaN FET Half-Bridge power stage integrated circuit (IC) and it uses wafer level chip scale packaging with a land grid array (LGA) configuration.

Part Number	Package Size (mm x mm)
EPC2152	L (3.85 x 2.59)

Qualification Test Overview

Devices of EPC2152 were subject to a wide variety of stress tests, according to JEDEC standard JESD47L¹. The stress tests include the following:

- High Temperature Operating Life (HTOL): Parts are subjected to recommended operating conditions at $T_j = 125^\circ\text{C}$ for 1000 hours.
- Highly Accelerated Test (HAST): Parts are soaked at 130°C and 85% humidity, and vapor pressure 33.3 psia with a constant V_{IN} voltage (60 V), V_{DD} voltage (13 V), and V_{IN} logic input (0 V).
- High Temperature Storage Life (HTSL): Parts are subjected to a bake at 150°C for 1000 hours.

- Preconditioning (PC): Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1) conditions (see MSL1 details below); (3) three times reflow.
- Temperature cycling (TC): Parts are subjected to alternating low and high temperature extremes from -40°C to $+125^\circ\text{C}$ for a total of 1000 cycles.
- MSL1: Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under Human Body Model (HBM) to assess device susceptibility to electrostatic discharge events.

All devices tested in this qualification underwent external visual inspection. Chips were inspected using an optical microscope to check for signs of physical damage to the chip-scale package, e.g., edge chipping or cracks, resulting from assembly, transit, or inadequate handling. Damaged parts were removed from the test population.

Parametric measurements were performed at 25°C on all the samples before and after the stress tests to verify compliance with the specifications listed on the product datasheet. The parameters measured include quiescent and operating currents of the driver (V_{DD}/V_{BOOT} pins), undervoltage lockout (UVLO V_{DD}/V_{BOOT} pins), input threshold voltages & hysteresis for the logic input signal (V_{IN} High Side (HS)/Low Side (LS) pins), and DC static parameters of the output transistors such as threshold voltage and drain-source leakage current.

For all the qualification tests, parts were mounted onto high Tg FR-4 adaptor cards with four layers and 1.6mm in thickness. Type-4 SAC305 solder paste with water-soluble (W/S) flux was used for mounting the parts onto the adaptor cards. After assembly, flux residue was cleaned using deionized (DI) water.

¹JESD47L, "Stress-Test-Driven Qualification of Integrated Circuits", December 2022

High Temperature Operating Life

Parts were subjected to the maximum recommended operating voltages and temperature for a stress period of 1000 hours. As shown in Table 1 below, three lots and 77 samples per lot were tested for EPC2152. Parts were mounted on high T_g FR-4 adapter cards. The test was conducted in accordance with JESD22-A108². Both capacitive and resistive loads are evaluated in a Buck Converter configuration for 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTOL	EPC2152	L (3.85 x 2.59)	$T_J = 125^\circ\text{C}$ $V_{D-D} = 13\text{ V}, V_{IN_DC} = 60\text{ V}, \text{Duty Cycle} = 25\%$ $V_{IN(HS/LS)} = 5 V_{P-P}$ (Buck Converter Capacitive Load; frequency=500 kHz)	0	77 x 2	1000
HTOL	EPC2152	L (3.85 x 2.59)	$T_J = 125^\circ\text{C}$ $V_{D-D} = 13\text{ V}, V_{IN_DC} = 60\text{ V}, \text{Duty Cycle} = 25\%$ $V_{IN(HS/LS)} = 5 V_{P-P}$ (Buck Converter Resistive Load; frequency=500 kHz)	0	77 x 1	1000

Table 1. High Temperature Operating Life Test

Highly Accelerated Test

Parts were subject to maximum recommended operating voltage and 130°C , 85%, and vapor pressure of 33.3 psia for a stress period of 96 hours. High Side and Low Side power FET were stressed independently with $V_{IN_DC} = 60\text{ V}$ and $V_{SW_DC} = 0\text{ V}$ or $V_{IN_DC} = V_{SW_DC} = 60\text{ V}, V_{IN(HS/LS)} = 0\text{ V}$ and $V_{DD} = 13\text{ V}$. The results are shown in Table 2 below, three lots and 25 samples per lot were tested. Parts were mounted on high T_g FR-4 adapter cards. Stress testing was conducted in accordance with JESD22-A101 .

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HAST	EPC2152	L (3.85 x 2.59)	$T_A = 130^\circ\text{C}, \text{RH} = 85\%, V_P = 33.3\text{ psia},$ $V_{DD} = 13\text{ V}, V_{IN_DC} = 60\text{ V}, V_{SW_DC} = 60\text{ V},$ $V_{IN(HS/LS)} = 0\text{ V}$	0*	25 x 3	96
HAST	EPC2152	L (3.85 x 2.59)	$T_A = 130^\circ\text{C}, \text{RH} = 85\%, V_P = 33.3\text{ psia},$ $V_{DD} = 13\text{ V}, V_{IN_DC} = 60\text{ V}, V_{SW_DC} = 60\text{ V},$ $V_{IN(HS/LS)} = 0\text{ V}$	0	25 x 3	96

*One out of 150 devices showed a negative UVLO (V_{DD}) shift that is below the lower specification limit, but all other parameters are normal. The device can recover in re-test.

Table 2. Temperature Humidity Bias Test

High Temperature Storage Life

Parts from one lot of EPC2152 (25 parts per lot) were exposed to ambient temperature of 150°C for a total of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTS	EPC2152	L (3.85 x 2.59)	$T_A = 150^\circ\text{C}, \text{Air}, \text{Unbiased}$	0	25 x 3	1000

Table 3. High Temperature Storage Test

² JESD22-A108, "Temperature, Bias, and Operating Life", December 2022

³ JESD22-A101, "Steady-State Temperature-Humidity Bias Life Test", January 2021

Temperature Cycling

Three lots of bare die EPC2152 (25 parts per lot) were subjected to temperature cycling between -40°C and 125°C for a total of 1000 cycles. In accordance with JEDEC Standard JESD22-A104⁴, five minutes dwell time was used in the hot and cold temperature extremes and heating/cooling rates were approximately 5°C per minute.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cys)
TC	EPC2152	L (3.85 x 2.59)	T _A = -40°C to +125°C Unbiased Bare Die	0	25 x 3	1000

Table 4. Temperature Cycling Test

Moisture Sensitivity Level

Parts were subjected to MSL1 conditions in accordance with the IPC/JEDEC joint Standard J-STD-020⁵ for Pb-free solder.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	EPC2152	L (3.85 x 2.59)	T _A = 85°C, R _H = 85%, 3x reflow	0	25 x 3	168

Table 5. Moisture Sensitivity Level Test

Electrostatic Discharge (ESD) Sensitivity

One lot of EPC2152 was subjected to ESD sensitivity test using the human body model (HBM). Testing was conducted according to JS-001-2023⁶ JEDEC standard. Device parameters were measured before and after ESD testing. Results are shown in Table 6 below. EPC2152 passed an HBM rating of 500 V. Additional HBM capability testing was conducted and EPC2152 passed 750 V.

Package size of 16 mm² or less is considered as a small package for CDM ESD per ESDA/JEDEC JTR002-01-22 . The die size of EPC2152 is less than 10 mm². Therefore, EPC2152 should be capable of 1 kV of CDM rating by matrix⁸.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	EPC2152	L (3.85 x 2.59)	500 V	0	3 x 1
ESD-HBM	EPC2152	L (3.85 x 2.59)	750 V	0	3 x 1

Table 6. Electrostatic Discharge (ESD) Sensitivity

⁴ JESD22-A104, "Temperature Cycling", April 2023

⁵ J-STD-020F, "Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)", December 2022

⁶ JS-001-2023, "Human Body Model (HBM) Component Level", July 2023

⁷ JS-002-2022, "Charged Device Model Testing of Integrated Circuits", December 2022

⁸ EPC2302 Qualification report." <https://epc-co.com/epc/Portals/0/epc/documents/reports/qualification/QR-EPC2302.pdf>"