EPC eGaN® FETs Automotive Qualification Report EPC2202–EPC2203

Robert Strittmatter, Director of Engineering, Efficient Power Conversion Corporation

This report summarizes the Product Qualification results for EPC part numbers EPC2202 and EPC2203 which meets all required AEC-Q101 requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification of EPC2202 and EPC2203 according to the component level AEC-Q101 Rev D1 testing requirements.

Part Number	Voltage (V)	$R_{DS(on)}$ (mΩ)	Die Size (mm x mm)	Maximum Operating Temperature (°C)
EPC2202	80	17	M (2.11 x 1.63)	150
EPC2203	80	80	S (0.95 x 0.95)	150

Qualification Test Overview

EPC's EPC2202 and EPC2203 eGaN FETs were subjected to a wide variety of stress tests following the specifications of AEC-Q101 (Rev D1) developed for silicon-based power MOSFETs. These tests include:

- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Senstivity Level 1 (MSL1); (3) 3 times reflow.
- Parametric Verification: Device parameters are measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet limits over the entire temperature range.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.
- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature and maximum rated voltage (80 V).
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature and maximum rated gate voltage (5.75 V).
- Unbiased highly accelerated test (uHAST): Parts are soaked for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia.
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -55°C to 150°C for a total of 1000 cycles
- High temperature high humidity reverse bias (H3TRB): Parts are subjected to 1000 hours of 85°C, 85% humidity with the drain biased at 80% of maximum rating.
- Moisture sensitivity level 1 (MSL1): Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Destructive Physical Analysis: Parts are delayered and physically analyzed looking for defects resulting from stress testing.

All devices put on test as part of this qualification underwent external visual inspection prior to test. This microscope inspection checks for physical damage to the chip-scale package, such as edge chipping or cracks, that may have resulted from assembly or transit. Damaged parts are removed from the test population.

For all qualification tests, the stability of the devices is verified with DC electrical tests before and after stress. In many cases, interim readouts are also performed. Electrical parameters are measured at room temperature. The parameters include: gate-source threshold voltage (V_{TH}), on-state resistance $R_{DS(on)}$, off-state drain leakage (I_{DSS}), and gate leakage (I_{GSS}). For V_{TH} and $R_{DS(on)}$, a failure is recorded when either of the following occurs: (i) the measurement exceeds the datasheet specifications; or (2) the measurement has changed by more than 20% of its initial value. For I_{DSS} and I_{GSS}, a failure is recorded if the measurement exceeds datasheet limit, or if it has increased by more than 5x during test. All testing requirements and specifications for AEC-Q101 (Rev D1) were followed.

For certain qualification tests, parts were mounted onto FR5 (high Tg FR4) or polyimide PCB adaptor cards. These cards simplify the process of post-screening and electrically stressing the parts. Adaptor cards (1.6 mm in thickness) with two copper layers were used. The top copper layer was 1 oz. or 2 oz., and the bottom copper layer was 1 oz. Kester NXG1 type 3 SAC305 solder no clean flux was used in mounting the part onto an adaptor card. After assembly, parts were either baked or flux-cleaned.

For other qualifications tests, including MSL1 and TC, parts were not mounted to adaptor cards. Electrical tests were performed using probe needles touching the solder pads of the bare die.

High Temperature Reverse Bias

Parts were subjected to 100% of the rated drain-source voltage (80 V) at the maximum rated temperature (150°C) for a stress period of 1000 hours. This test duration and temperature satisfies the AEC-Q101 requirements for a 125°C rating. EPC2202 (2 lots) and EPC2203 (1 lot) are qualified by matrix within the same 80V product family. Parts were mounted on FR5 adapter cards. Testing was conducted in accordance with MIL-STD-750-1 (M1038 Method A). This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 24 hours after bias has been removed.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2202	80	M (2.11 x 1.63)	T=150°C, V_{DS} = 80 V	0	77 x 2	1000
HTRB	EPC2203	80	S (0.95 x 0.95)	T=150°C, V_{DS} = 80 V	0	77 x 1	1000

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts were subjected to maximum rated gate-source bias (5.75 V) at the maximum rated temperature (150°C) for a stress period of 1000 hours. This test duration and temperature satisfies the AEC-Q101 requirements for a 150°C rating. EPC2202 (2 lots) and EPC2203 (1 lot) are qualified by matrix within the same 80V product family. Parts were mounted on FR5 adapter cards. Testing was conducted in accordance with JESD22-A108. This standard requires the parts to be under bias during temperature ramp up and cool down. In addition, post-screening must occur within 96 hours after bias has been removed.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2202	80	M (2.11 x 1.63)	T = 150°C, V_{GS} = 5.75 V	0	77 x 2	1000
HTGB	EPC2203	80	S (0.95 x 0.95)	T = 150°C, V_{GS} = 5.75 V	0	77 x 1	1000

Table 2. High Temperature Gate Bias Test

Unbiased Highly Accelerated Test

Parts were subjected to 96 hours at a temperature of 130°C, relative humidity of 85%, and vapor pressure of 33.3 psia. heat at the maximum rated temperature. Three lots were tested for both EPC2202 and EPC2203. All parts were mounted on FR5 adaptor boards. Per AEC requirements, all parts went through pre-conditioning before uHAST.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
uHAST	EPC2202	80	M (2.11 x 1.63)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 X 3	96
uHAST	EPC2203	80	S (0.95 x 0.95)	T = 130°C, RH = 85%, VP = 33.3 psia	0	77 X 3	96

Table 3. Unbiased Highly Accelerated Test

Temperature Cycling

Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles. A ramp rate of 15°C/min and a dwell time of 5 minutes were used in accordance with the JEDEC Standard JESD22A104. All parts went through pre-conditioning prior to TC.

Three lots of both EPC2202 and EPC2203 passed the automotive requirement of 1000 cycles, with die (package) loaded into trays. One lot of EPC2202 was assembled onto low CTE polyimide adaptor cards, and also passed the 1000 cycle requirement. Two lots of both EPC2202 and EPC2203 were assembled onto FR5 cards, and passed 500 cycles.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)	Format
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 3	1000	Bare Die
TC	EPC2203	80	S (0.95 x 0.95)	-55 to 150°C, Air	0	77 x 3	1000	Bare Die
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 1	1000	PCB (Arlon 85NT)
TC	EPC2202	80	M (2.11 x 1.63)	-55 to 150°C, Air	0	77 x 2	500	PCB (FR5)
TC	EPC2203	80	S (0.95 x 0.95)	-55 to 150°C, Air	0	77 x 2	500	PCB (FR5)

Table 4. Temperature Cycling Test

High Temperature High Humidity Reverse Bias

Parts were subjected to a drain-source bias of 80% maximum voltage rating, 85% RH and 85°C for a stress period of 500 or 1000 hours. The testing was done in accordance with the JEDEC Standard JESD22-A101, as required by AEC-Q101. All parts were mounted on FR5 adaptor boards. All parts went through pre-conditioning before H3TRB. The lots tested for 500 hours are continuing test until 1000 hours.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
H3TRB	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 X 3	1000
H3TRB	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 2	1000
H3TRB	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 2	500
H3TRB	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, V_{DS} = 64 V	0	77 x 1	500

Table 5. High Temperature High Humidity Reverse Bias Test

Moisture Sensitivity Level 1

Parts were subjected to 85% RH at 85°C for a soak period of 168 hours. Within 4 hours after the soak, the parts underwent three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020. These conditions correspond to a moisture sensitivity level 1, the most stringent level of moisture sensitivity testing. For this testing, parts were loaded in trays in bare die form (not attached to PCBs). Pre-screen and post-screen were performed using probe needles to contact the solder pads of the bare die.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
MSL1	EPC2202	80	M (2.11 x 1.63)	T = 85°C, RH = 85%, 3 reflow	0	77 X 3	168
MSL1	EPC2203	80	S (0.95 x 0.95)	T = 85°C, RH = 85%, 3 reflow	0	77 X 3	168

Table 6. Moisture Sensitivity Level Test

Destructive Physical Analysis

In accordance with AEC-Q101 requirements, two parts from EPC2202 and two parts from EPC2203 were selected for physical analysis after successfully completing uHAST testing. The physical analysis was conducted in three steps: (1) removal of die from PCB adapter card; (2) chemical removal of solder bumps/bars; (3) removal of top-layer passivation layers via dry etch. After each step, a high magnification optical microscope inspection was performed. No damage or abnormalities were observed as a result of prior stress testing.

Electrostatic Discharge (ESD) Sensitivity

Both EPC2202 and EPC2203 were tested for ESD sensitivity using both the human body model (HBM) and charged device model (CDM). Testing was conducted according to AEC-Q101-001 and Q101-005 standards. Device parameters were measured before and after ESD testing. Results are shown in Table 7 below. Both EPC2202 and EPC2203 passed HBM with a rating of 500 V. Both devices passed CDM with a 1000 V rating.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - HBM	EPC2202	80	M (2.11 x 1.63)	1000 V	1	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	500 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	750 V	0	10 x 1
ESD - CDM	EPC2202	80	M (2.11 x 1.63)	1000 V	0	10 x 1
ESD - HBM	EPC2203	80	S (0.95 x 0.95)	250 V	0	10 x 1
ESD - HBM	EPC2203	80	S (0.95 x 0.95)	500 V	1	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	500 V	0	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	750 V	0	10 x 1
ESD - CDM	EPC2203	80	S (0.95 x 0.95)	1000 V	0	10 x 1

Table 7. ESD HBM and CDM Tests

Parametric Verification

In accordance with AEC-Q101 requirements, device parameters were measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet specifications over the entire temperature range. Parametric verification was performed 3 lots x 25 parts, for both EPC2202 and EPC2203.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)
Parametric Verification	EPC2202	80	M (2.11 x 1.63)	T = 40°C, 25°C, 150°C	0	25 x 3
Parametric Verification	EPC2203	80	S (0.95 x 0.95)	T = 40°C, 25°C, 150°C	0	25 x 3

Table 8. Parametric Verification

Intermittent Operating Life

In accordance with MIL-STD-750 (Method 1037), parts are power cycled over a ΔTj = 125°C temperature range. Devices are heated through internal electrical power dissipation by biasing them in the linear mode, with combined gate and drain bias and a regulated drain current. With a 1-minute temperature ramp, and a 5 minute cool down, a minimum of 5000 cycles are required. Devices were assembled onto low CTE polyimide PCBs (Arlon 85NT). As seen in Table 9, two lots of EPC2202 passed 5000 cycles, and one lot of EPC2203 passed 7500 cycles (exceeding AEC requirements).

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)	Forrmat
IOL	EPC2202	80	M (2.11 x 1.63)	ΔTj = 125°C; ton / toff = 1 min /5 min	0	77 x 2	5000	PCB (Arlon 85NT)
IOL	EPC2203	80	S (0.95 x 0.95)	ΔTj = 125°C; ton / toff = 1 min /5 min	0	77 x 1	7500	PCB (Arlon 85NT)

Table 9. Intermittent Operating Life Tests