EPC eGaN® FET Qualification Report EPC2234

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This report summarizes the Product Qualification results for EPC part number EPC2234 which meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification of EPC2234 according to the component level AEC-Q101 Rev D1 requirements.

Part Number	Voltage (V)	$R_{DS(on)}$	Die Size	Maximum Operating Temperature (°C)
EPC2234	160	8	L (4.6 x 2.6)	150

Qualification Test Overview

EPC's EPC2234 eGaN FETs were subjected to a wide variety of stress tests following the specifications of AEC-Q101 (Rev D1). The following tests are included.

- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature and maximum rated voltage (160 V).
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature and maximum rated gate voltage (5.5 V).
- Biased highly accelerated test (bHAST): Parts are subjected to a drain-source voltage of 100 V for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia.
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -55°C to 150°C for a total of 1000 cycles.
- Intermittent Operating Life (IOL): Parts are temperature cycled with short period and device heating through internal electrical power dissipation.
- Moisture sensitivity level 1 (MSL1): Parts are subjected to moisture, temperature, and three cycles of reflow. MSL1 is the most stringent of the moisture sensitivity levels, requiring 85°C and 85% humidity for 168 hours.
- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1); (3) 3 times reflow.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.
- Parametric Verification: Device parameters are measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet limits over the entire temperature range.
- Destructive Physical Analysis: Parts are delayered and physically analyzed looking for defects resulting from stress testing.

All devices put on test as part of this qualification underwent external visual inspection prior to test. This microscope inspection checks for physical damage to the chipscale package, such as edge chipping or cracks, that may have resulted from assembly or transit. Damaged parts are removed from the test population.

For all qualification tests, the stability of the devices is verified with DC electrical tests before and after stress at room temperature. The parameters include gate-source threshold voltage (V_{TH}), on-state resistance ($R_{DS(on)}$), off-state drain leakage (I_{DSS}), and gate leakage (I_{GSS}). For V_{TH} and $R_{DS(on)}$, a failure is recorded when either of the following occurs: (1) the measurement exceeds the datasheet specifications; or (2) the measurement has changed by more than 20% of its initial value. For I_{DSS} and I_{GSS}, a failure is recorded if either one of the following criteria is satisfied: (1) the measurement exceeds datasheet limits; or (2) the measurement post-stress increases more than 5x compared to the initial value. One exception to the 5X I_{GSS} criterion is HTGB, where higher than 5x I_{GSS} shift, but stable over 1000 hours following an initial shift, was formally accepted by the lead customer.

For the majority of the qualification tests, parts were mounted onto FR5 (high Tg FR4) PCB adaptor cards. These cards simplify the process of electrical screening and stressing and prevent mechanically damaging the parts during handling. Adaptor cards (1.6 mm in thickness) with two copper layers were used with 1 Oz copper of the top and bottom metal layers. Kester NXG1 type 3 SAC305 solder with water soluble flux was used in mounting the part onto an adaptor card. After assembly, parts were flux-cleaned and subsequently subjected to oven bake at 125°C. For TC qualification test, parts were not mounted to adaptor cards and electrical screening was performed using sockets.

High Temperature Reverse Bias

Parts were subjected to 100% of the maximum rated drain-source voltage (160 V) at the maximum rated temperature (150°C) for a stress period of 1000 hours. The test duration and temperature meet the AEC-Q101 requirements, and the testing was conducted in accordance with MIL-STD-750-1 (M1038 Method A). The parts were under bias during temperature ramp up and cool down and post-screening was conducted within 24 hours after the bias was removed.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTRB	**EPC2234**	160	L (4.6 x 2.6)	T=150°C, V_{DS} = 160 V	0	77 x 4	1000

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts were subjected to the maximum rated gate-source bias (5.5 V) at the maximum rated temperature (150°C) for a stress period of 1000 hours. Testing was conducted in accordance with JESD22-A108, and the parts were under bias during temperature ramp up and cool down.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
HTGB	**EPC2234**	160	L (4.6 x 2.6)	T = 150°C, V_{GS} = 5.5 V	0	77 x 3	1000

Table 2. High Temperature Gate Bias Test

*I_{GSS} of three devices shifted more than the main distribution at 11x, 12x, and 24x, respectively. The I_{GSS} shift occurred in the beginning of the HTGB testing, but all parts stayed stable at the end of 1000 hours. The post-stress I_{GSS} are measured well below the 400 µA datasheet I_{GSS} limit. None of the other parameters including I_{DSS}, V_{TH}, and $R_{DS(on)}$ showed any significant shifts. Electrical and physical analyses were carried out, but no structural abnormalities were found in them. Therefore, they are not considered as failures and the explanation has been accepted by the lead customer.

Biased Highly Accelerated Test

Parts were subjected to 100 V drain-source voltage at a temperature of 130°C, with a relative humidity of 85%, and vapor pressure of 33.3 psia for a stress period of 96 hours. Drain-source bias is limited to a maximum of 100 V to prevent arcing in a high humidity chamber. Per AEC requirements, all parts went through pre-conditioning before bHAST.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
bHAST	**EPC2234**	160	L (4.6 x 2.6)	T = 130°C, RH = 85%, VP = 33.3 psia, V_{DS} =100 V	0	77 x 3	96

Table 3. High Temperature Storage Test

Temperature Cycling

Parts were subjected to temperature cycling between -55°C and +150°C for a total of 1000 cycles with die (package) loaded in trays. A ramp rate of 15°C/min and a dwell time of 10 minutes were used in accordance with the JEDEC Standard JESD22A104. All parts went through pre-conditioning prior to TC.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cys)
TC	**EPC2234**	160	L (4.6 x 2.6)	-55 to +150°C, Air	0	77 x 3	1000

Table 4. Moisture Sensitivity Level Test

Intermittent Operating Life

In accordance with MIL-STD-750 (Method 1037), parts are power cycled over a ΔT = 125°C temperature range. Devices are heated through internal electrical power dissipation by biasing them in the linear mode, with combined gate and drain bias and a regulated drain current. With a 1-minute temperature ramp, and a 5-minute cool down, a minimum of 5000 cycles are required. Parts were assembled onto FR5 (high Tg FR4) adapter board with underfill material applied. (Underfill manufacturer: Henkels and part number: ECCOBOND-UF1173).

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Cycles)
IOL	EPC2234	160	L (4.6 x 2.6)	ΔT_J =125°C; t_{on} / t_{off} = 1 min /5 min	0	77 x 3	5000

Table 5. Temperature Cycling Test

Moisture Sensitivity Level

Parts were subjected to 85% RH at 85°C for a soak period of 168 hours. Within 4 hours after the soak, the parts underwent three cycles of reflow in accordance with the IPC/JEDEC joint Standard J-STD-020. These conditions correspond to moisture sensitivity level 1 (MSL1), the most stringent level of moisture sensitivity testing.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	EPC2234	160	L (4.6 x 2.6)	T = 85°C, RH = 85%, 3X reflow	0	77 x 3	168

Table 6. Moisture Sensitivity Level Test

Electrostatic Discharge (ESD) Sensitivity

EPC2234 was tested for human body model (HBM) ESD sensitivity following AEC Q101-001 standards and passed with a rating of 500 V, equivalent of component classification of H1B. EPC2234 has a die area of 11.96 mm^2 that is less than the small packages definition (16 mm^2 or less) specified by JEDEC standard[1], where CDM ESD testing is no longer required. In addition, EPC2234 should also pass 1000 V CDM ESD rating by testing matrix of a larger qualified device[2].

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	EPC2234	160	L (4.6 x 2.6)	500 V	0	10 x 1

Table 7. Electrostatic Discharge Sensitivity Test

Parametric Verification

In accordance with AEC-Q101 requirements, device parameters were measured at -40°C, 25°C, and 150°C to ensure compliance with datasheet specifications over the entire temperature range.

Stress Test	Part Number	Voltage (V)	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
PV	EPC2234	160	L (4.6 x 2.6)	T = -40°C, T = 25°C, T = 150°C	0	25 x 3

Table 8. Parametric Verification Test

Destructive Physical Analysis

In accordance with AEC-Q101 requirements, two parts from EPC2234 were submitted for destructive physical analysis after successfully completing TC testing. The physical analysis was conducted in three steps: (1) removal of the devices from the PCB adapter card; (2) chemical removal of solder bumps; (3) removal of top-layer passivation layers via wet and dry etch. Subsequently, optical microscope inspection was performed at 50x magnification. No damage or abnormalities were observed.

[1] JEDEC standard, JTR002-01-22, "Charged Device Model Testing of Integrated Circuits", December 2022

[2] EPC2302 Qualification Report, "https://epc-co.com/epc/Portals/0/epc/documents/reports/qualification/QR-EPC2302.pdf"