EPC eGaN® FET Qualification Report EPC2304 and EPC2307

Dr. Shengke Zhang, VP of Reliability, Efficient Power Conversion Corporation

This report summarizes the Product Qualification results for EPC part numbers EPC2304 and EPC2307 which meets all required qualification requirements and is released for production.

Scope

The testing matrix in this qualification report covers the qualification of EPC2304 and EPC2307, 200 V eGaN power transistors in a QFN package with exposed silicon on top for low thermal resistance from junction to top side heatsink sharing the same device design and fabrication process. EPC2304 die size is twice that of EPC2307 sharing the same QFN package design.

Part Number	Voltage (V)	Max $R_{DS(on)}$ (mΩ)	Package Size (mm x mm)
EPC2304	200	5	L (3 x 5)
EPC2307	200	10	L (3 x 5)

Qualification Test Overview

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- High temperature reverse bias (HTRB): Parts are subjected to an 80% of the maximum rated drain-source voltage at the maximum rated temperature (150°C).
- High temperature gate bias (HTGB): Parts are subjected to the maximum rated gate-source voltage (6 V) at the maximum rated temperature (150°C).
- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1); (3) 3 times reflow.
- Biased highly accelerated test (bHAST) Parts are subjected to a constant drain-source voltage (100 V) for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia.
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -40°C to 125°C for a total of 1000 cycles.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) to assess device susceptibility to electrostatic discharge events.

The stability of the devices is verified with DC electrical tests after reliability stressing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the data sheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) JESD47L[1] standard.

Parts for all tests were mounted onto high Tg FR4 adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used, the top and bottom copper layer thickness is 2 oz. Kester WP616 type 4 SAC305 solder with no clean flux was used for mounting the parts onto an adaptor card.

[1] JESD47L, "Stress-Test-Driven Qualification of Integrated Circuits", December 2022

High Temperature Reverse Bias

Parts from two lots of EPC2304 and one lot of EPC2307 were subjected to 80% of the maximum rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours. Two failures out of a total of 884 devices from EPC2304 and EPC2307 were found. This failure rate satisfies the acceptance criteria of LTPD less than 1 based on the JEDEC standard (JESD47L) and EPC's internal quality standard. One lot each of EPC2304 and EPC2307 were also tested at 100% rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours with zero failures.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2304	T = 150°C, V_{DS} = 160 V	2*	398 x 2	1000
HTRB	EPC2307	T = 150°C, V_{DS} = 160 V	0	88 x 1	1000
HTRB	EPC2304	T = 150°C, V_{DS} = 200 V	0	88 x 1	1000
HTRB	EPC2307	T = 150°C, V_{DS} = 200 V	0	88 x 1	1000

*Potential failure root causes have been isolated, and fixes are currently under verification.

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts from three lots were subjected to 6 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2304	T = 150°C, V_{GS} = 6 V	0	77 x 2	1000
HTGB	EPC2307	T = 150°C, V_{GS} = 6 V	0	77 x 1	1000

Table 2. High Temperature Gate Bias Test

Moisture Sensitivity Level

Parts from six lots were subjected to 85% RH at 85°C for a stress period of 168 hours (as defined by J-STD-020F[2] for MSL1 products). The parts were also subjected to three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	EPC2304	T = 85°C, RH = 85%, 3 reflow	0	77 x 4	168
MSL1	EPC2307	T = 85°C, RH = 85%, 3 reflow	0	77 x 3	168

Table 3. Moisture Sensitivity Level Test

Biased Highly Accelerated Test

Parts were subjected to 100 V drain-source voltage at a temperature of 130°C, with a relative humidity of 85%, and vapor pressure of 33.3 psia for a stress period of 96 hours. Drain-source bias is limited to a maximum of 100 V to prevent arcing in a high humidity chamber.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
bHAST	EPC2304	T = 130°C, RH = 85%, VP = 33.3 psia, V_{DS} = 100 V	0	77 x 2	96
bHAST	EPC2307	T = 130°C, RH = 85%, VP = 33.3 psia, V_{DS} = 100 V	0	77 x 1	96

Table 4. Biased Highly Accelerated Test

[2] J-STD-020F, "Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)", December 2022

Temperature Cycling

Parts mounted on FR4 test coupons from two lots of each part were subjected to temperature cycling between -40°C and +125°C. A ramp rate of 15°C/min and dwell times of 10 minutes was used in accordance with the JEDEC Standard JESD22A104[3] . All parts went through pre-conditioning prior to TC with MSL1 conditions.

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2304	-40 to + 125°C, Air	0	77 x 2	1000
TC	EPC2307	-40 to + 125°C, Air	0	77 x 2	1000

Table 5. Temperature Cycling Test

Electrostatic Discharge (ESD) Sensitivity

Parts were tested for ESD sensitivity using the human body model (HBM). Testing was conducted according to JEDEC JS-001-2023[4] for HBM. Device parameters were measured before and after ESD testing. EPC2304 passed HBM with a rating of 1000 V.

EPC2302 passed CDM with a rating of 1000 V. As per JEDEC standard JS-002-2022[5] . CDM rating is dependent upon the die size. Therefore, EPC2304 should have a CDM rating of 1000 V by matrix[6].

Stress Test	Part Number	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	EPC2304	500 V	0	3 x 1
ESD-HBM	EPC2304	1000 V	0	3 x 1
ESD-HBM	EPC2307	500 V	0	3 x 1

Table 6. ESD HBM Test

[3]JEDEC standard, JESD22-A104, "Temperature cycling", November 2020

[4]JS-001-2023, "Human Body Model (HBM) Component Level", July 2023

[5]JS-002-2022, ""Charged Device Model Testing of Integrated Circuits", December 2022

[6]EPC2302 Qualification report." https://epc-co.com/epc/Portals/0/epc/documents/reports/qualification/QR-EPC2302.pdf"