EPC eGaN® FETs Qualification Report EPC2367

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This report summarizes the Product Qualification results for EPC part number EPC2367 which meets all required qualification requirements and is released for production.

Scope

This qualification report covers the qualification of EPC2367, a 100 V_{DS}-rated eGaN power transistor in a QFN package with exposed silicon on top for low thermal resistance from junction to top-side heatsink.

Part Number	Voltage (V)	$R_{DS(on)}$ (mΩ)	Die Size (mm x mm)
EPC2367	100	1.2	M (3.3 x 3.3)

Qualification Test Overview

EPC's eGaN FETs were subjected to a wide variety of stress tests under conditions that are typical for silicon-based power MOSFETs. These tests included:

- Preconditioning: Parts undergo the following steps in sequence: (1) 125°C bake for a minimum of 24 hours; (2) Moisture Sensitivity Level 1 (MSL1); (3) 3 times reflow.
- High temperature reverse bias (HTRB): Parts are subjected to a drain-source voltage at the maximum rated temperature (150°C) and 80% of the maximum rated voltage.
- High temperature gate bias (HTGB): Parts are subjected to a gate-source voltage at the maximum rated temperature (150°C) and the maximum rated gate voltage (6V).
- Biased highly accelerated test (bHAST): Parts are soaked for 96 hours at 130°C, 85% humidity, and vapor pressure 33.3 psia with a constant drain-source voltage at 80% of the maximum rated voltage.
- Temperature cycling (TC): Parts are subjected to alternating high and low temperature extremes from -40°C to 125°C.
- Moisture sensitivity level (MSL): Parts are subjected to moisture, temperature, and three cycles of reflow.
- Electrostatic Discharge (ESD) Characterization: Parts are tested under both Human Body Model (HBM) and Charged Device Model (CDM) to assess device susceptibility to electrostatic discharge events.

The stability of the devices is verified with DC electrical tests after stress biasing. The electrical parameters are measured at time-zero and at interim readout points at room temperature. Electrical parameters such as the gate-source leakage, drain-source leakage, gate-source threshold voltage, and on-state resistance are compared against the datasheet specifications. A failure is recorded when a part exceeds the datasheet specifications. eGaN FETs are stressed to meet the latest Joint Electron Device Engineering Council (JEDEC) JESD47L standard.

Parts for all tests were mounted onto high Tg FR4 adaptor cards. Adaptor cards of 1.6 mm in thickness with two copper layers were used. The top and bottom copper layer was 1 oz each. Kester Type 4 SAC305 solder paste with water soluble flux was used for mounting the parts onto adaptor cards.

High Temperature Reverse Bias

Parts from three lots for EPC2367 were subjected to 80% of the maximum rated drain-source voltage at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTRB	EPC2367	M (3.3 x 3.3)	T = 150°C, V_{DS} = 80 V	0	77 x 3	1000

Table 1. High Temperature Reverse Bias Test

High Temperature Gate Bias

Parts from three lots for EPC2367 were subjected to 6 V gate-source bias at the maximum rated temperature for a stress period of 1000 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Hrs)
HTGB	EPC2367	M (3.3 x 3.3)	T = 150°C, V_{GS} = 6 V	0	77 x 3	1000

Table 2. High Temperature Gate Bias Test

Biased Highly Accelerated Test

Parts from three lots for EPC2367 were subjected to 80 V drain-source voltage at a temperature of 130°C, with a relative humidity of 85%, and vapor pressure of 33.3 psia for a stress period of 96 hours.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
bHAST	EPC2367	M (3.3 x 3.3)	T = 130°C, RH = 85%, VP = 33.3 psia, V_{DS} = 80 V	0	77 x 3	96

Table 3. Biased Highly Accelerated Test

Temperature Cycling

Parts were subjected to temperature cycling between -40°C and +125°C for a total of 1000 cycles. A ramp rate of 15°C/min and a dwell time of 10 minutes were used in accordance with the JEDEC Standard JESD22-A104[1]. All parts went through pre-conditioning prior to TC.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (sample x lot)	Duration (Cys)
TC	EPC2367	M (3.3 x 3.3)	-40 to +125°C, Air	0	77 x 3	1000

Table 4. Temperature Cycling Test

Moisture Sensitivity Level 1

Parts were subjected to 85% RH at 85°C for a soak period of 168 hours. The parts underwent three cycles of Pb-free reflow in accordance with the IPC/JEDEC joint Standard J-STD-020F[2]. These conditions correspond to moisture sensitivity level 1, the most stringent level of moisture sensitivity testing.

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)	Duration (Hrs)
MSL1	EPC2367	M (3.3 x 3.3)	T = 85°C, RH = 85%, 3X reflow	0	77 x 6	168

Table 5. Moisture Sensitivity Level Test

Electrostatic Discharge (ESD) Sensitivity

The eGaN FETs were tested for human body model (HBM) ESD sensitivity following the JS-001-2023 standard.

The package size is less than the small packages definition (16 mm^2 or less) by JEDEC standard[3], where CDM ESD testing is no longer required. Therefore, EPC2367 should pass 1000 V CDM ESD rating by matrix[4].

Stress Test	Part Number	Die Size (mm x mm)	Test Condition	# of Failure	Sample Size (unit x lot)
ESD-HBM	**EPC2367**	M (3.3 x 3.3)	1000 V	0	3 x 1

Table 6. ESD HBM Test

[1]JEDEC standard, JESD22-A104, "Temperature cycling", November 2020
[2]J-STD-020F, "Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)", December 2022
[3]JEDEC standard, JTR002-01-22, "Charged Device Model Testing of Integrated Circuits", December 2022
[4]EPC2302 Qualification report. "https://epc-co.com/epc/Portals/0/epc/documents/reports/qualification/QR-EPC2302.pdf"