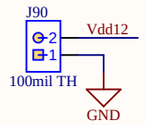
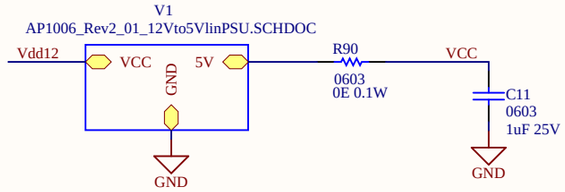
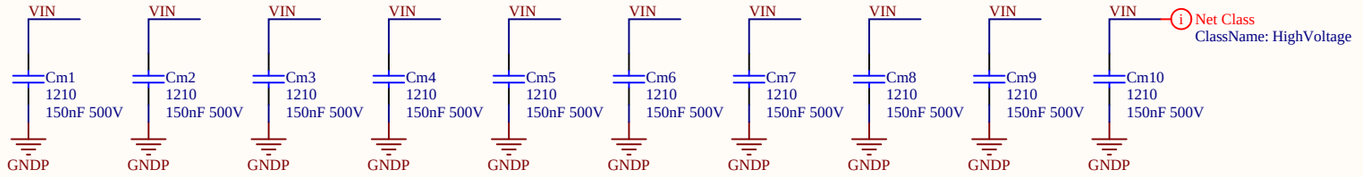


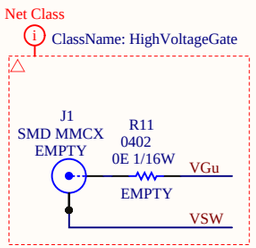
Logic Supply
10-15 VDC



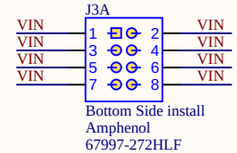
5 V Logic Regulator



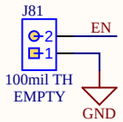
Intermediate Capacitors

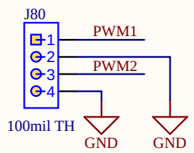


Upper Gate

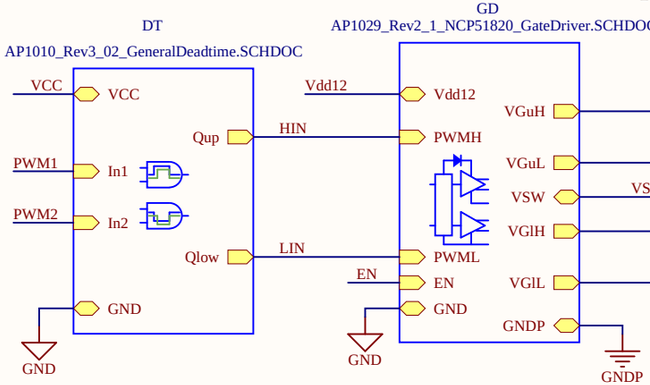


Main Supply Input

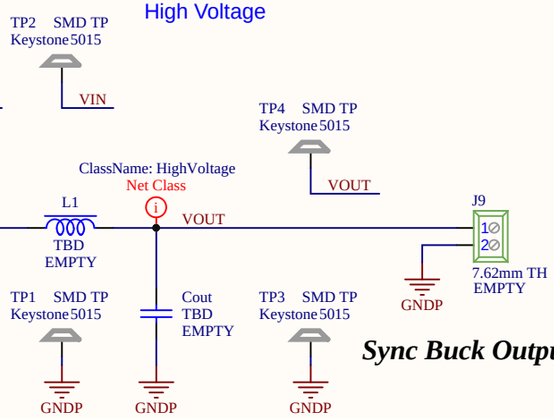




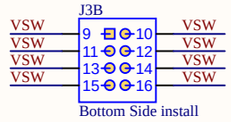
Signal Inputs



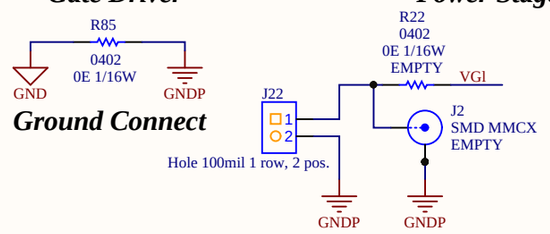
dead-time and buffers
Gate Driver
Power Stage



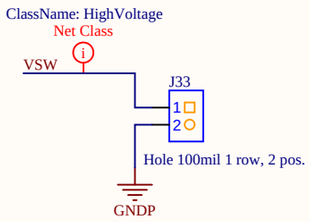
Sync Buck Output



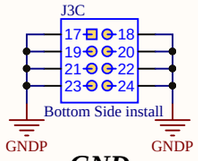
SW Output



Ground Connect
Lower Gate



Switch-node

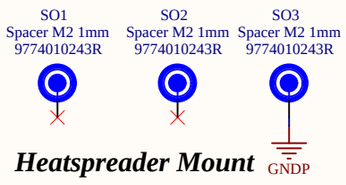


GND

For evaluation only;
not FCC approved for resale

PCB Fiducial

EPC90140 B5269 Rev. 1.0

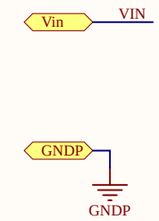


Heatspreader Mount

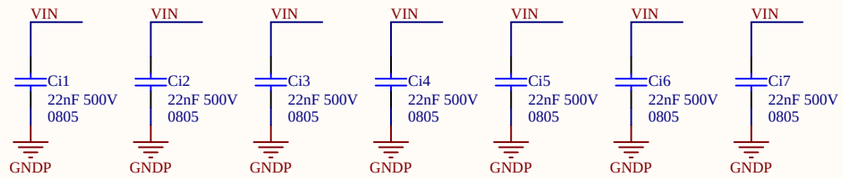
eGaN® FET

Evaluation Board for EPC2304

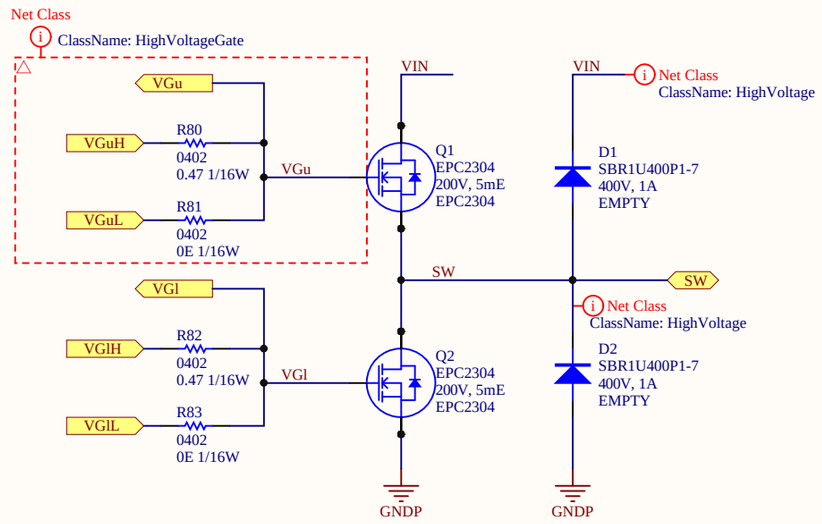
Title: EPC90140 B5269 Rev 1.0		Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com	
Size: A	1	Revision: 1	
Date: 11/3/2022		Sheet 1 of 5	
File: EPC90140_B5269_Rev1_0.SCHDOC			



DC Input
160 Vmax.

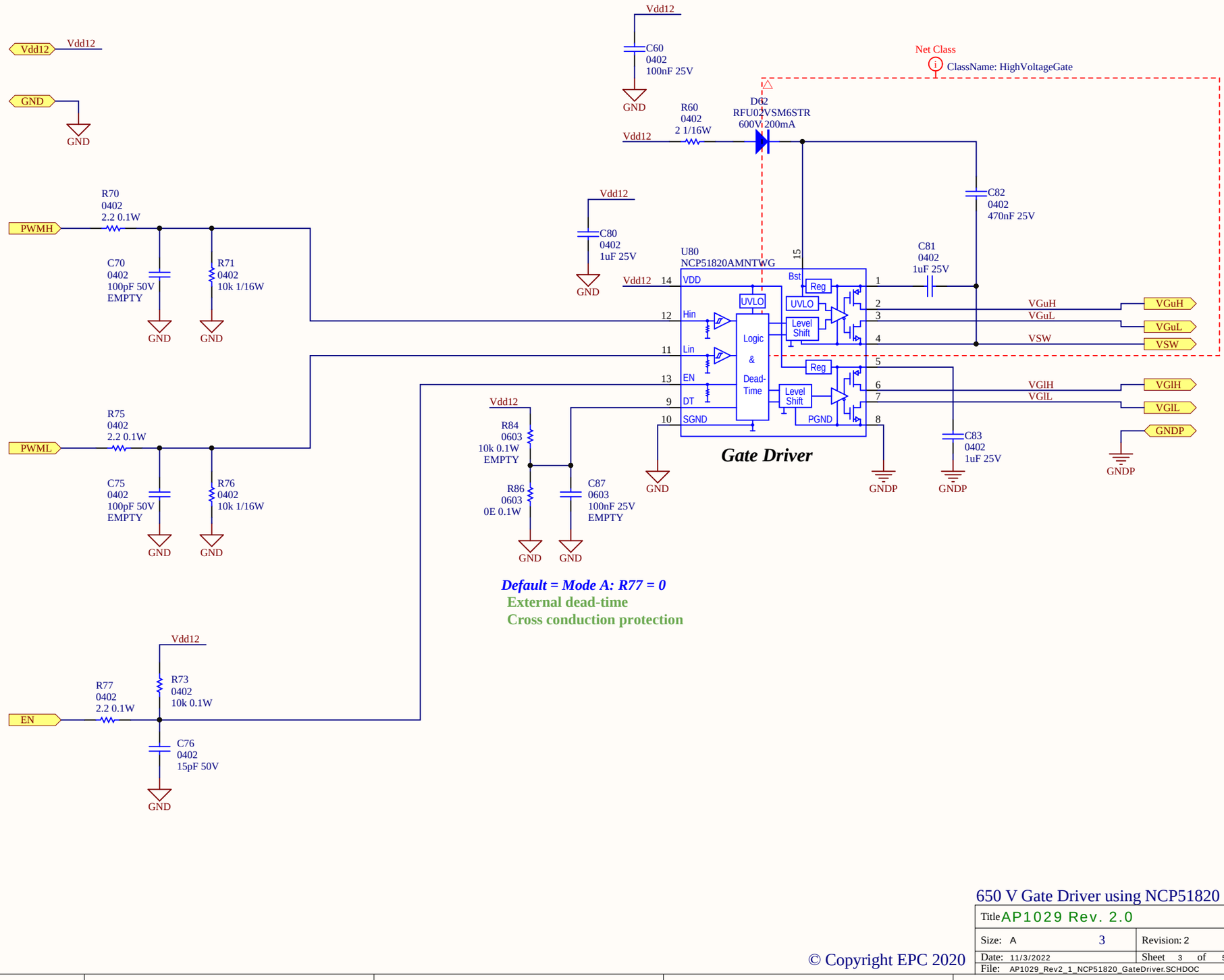


HF loop Capacitors



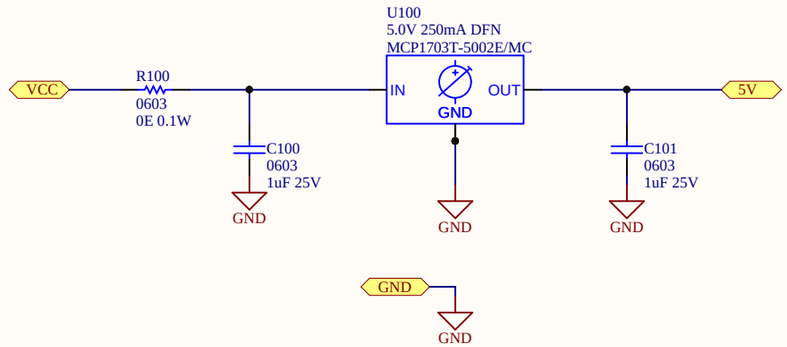
Power Stage ***Optional Diodes***

Title EPC2304 Phase Leg Rev. 1.0		Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com	
Size: A	2	Revision: 1	
Date: 11/3/2022		Sheet 2 of 5	
File: EPC2304_Rev1_0_PhaseLeg.SCHDOC			



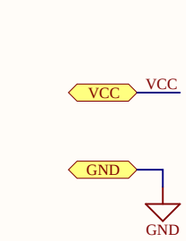
650 V Gate Driver using NCP51820

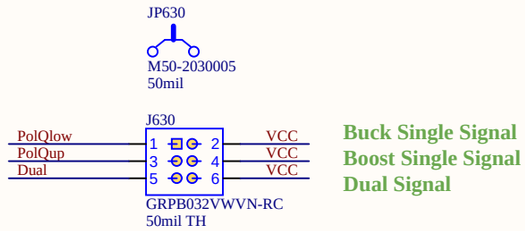
Title AP1029 Rev. 2.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	3	Revision: 2	
Date: 11/3/2022		Sheet 3 of 5	
File: AP1029_Rev2_1_NCP51820_GateDriver.SCHDOC			



12 V to 5 V LDO power supply

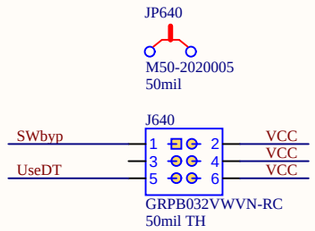
Title AP1006 Rev. 2.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	4	Revision: 1	
Date: 11/3/2022		Sheet 4 of 5	
File: AP1006_Rev2_01_12Vto5VlinPSU.SCHDOC			





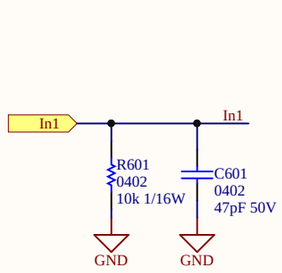
Buck Single Signal
Boost Single Signal
Dual Signal

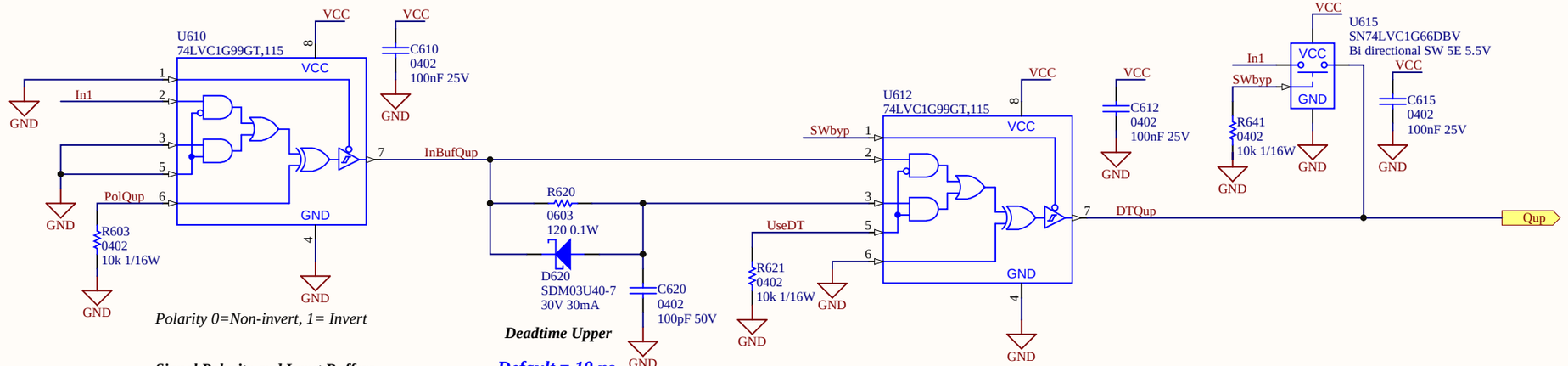
Dual/Single PWM, Buck, and Boost Mode Selector



Full Bypass
DT Bypass
No Bypass

Bypass Mode Select





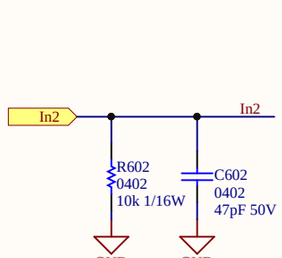
Polarity 0=Non-invert, 1= Invert

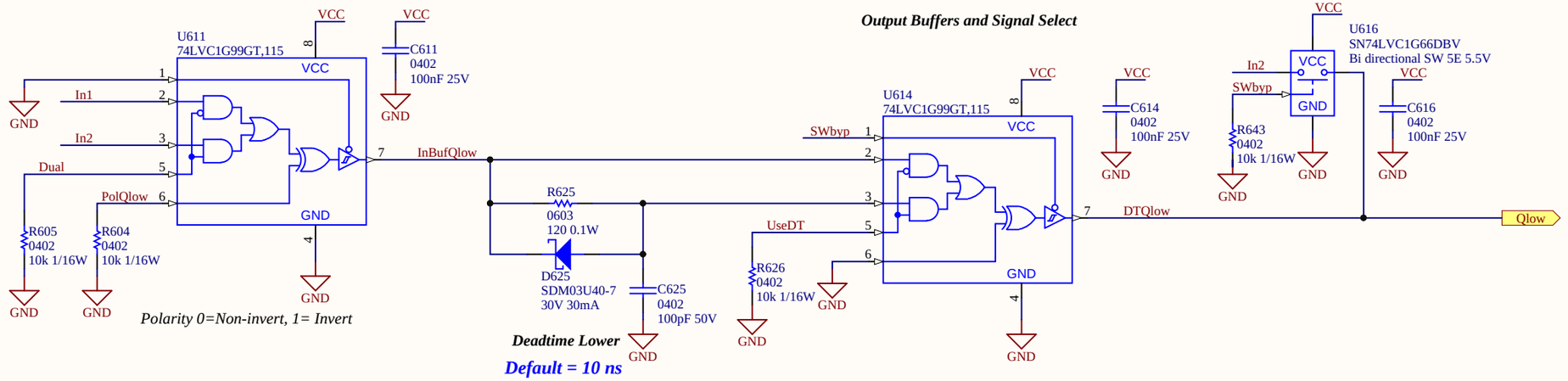
Signal Polarity and Input Buffers

Deadtime Upper

Default = 10 ns

Output Buffers and Signal Select





Polarity 0=Non-invert, 1= Invert

Deadtime Lower

Default = 10 ns

Output Buffers and Signal Select

General Dead-time with Polarity Changer and Bypass

Title AP1010 Rev. 3.0			Efficient Power Conversion 909 N. Pacific Coast Hwy, Ste. 23 El Segundo, CA 90245 United States www.epc-co.com
Size: A	5	Revision: 1	
Date: 11/3/2022		Sheet 5 of 5	
File: AP1010_Rev3_02_GeneralDeadtime.SCHDOC			