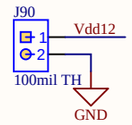
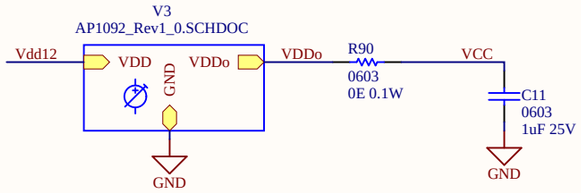
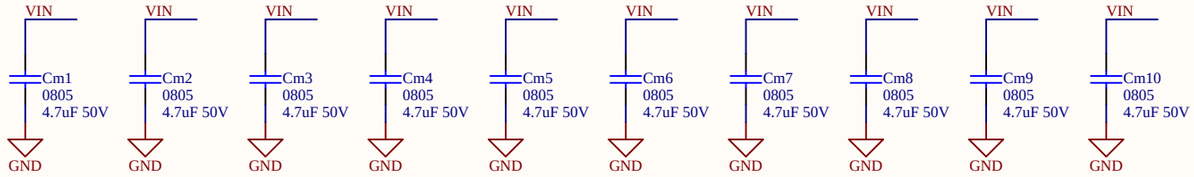


Logic Supply

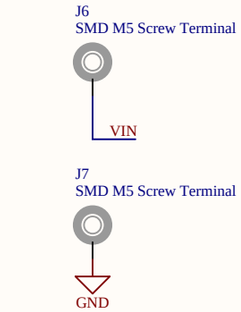
12VDC

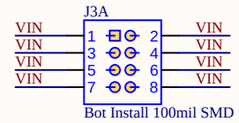


VCC Supply

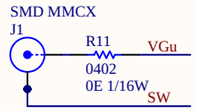


Intermediate Capacitors

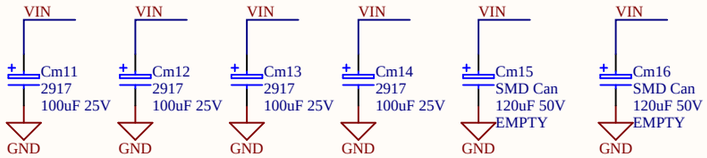


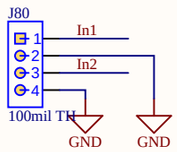


Main Supply Input

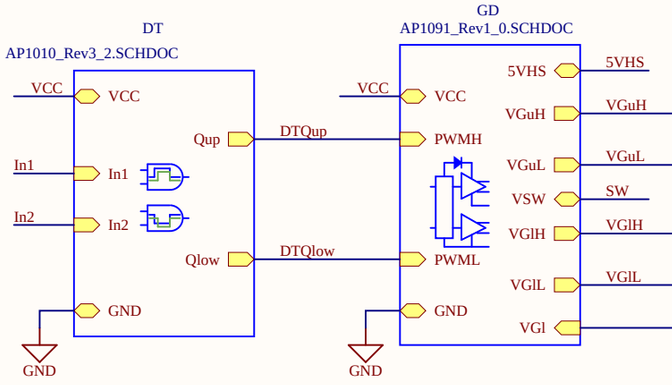


Upper Gate





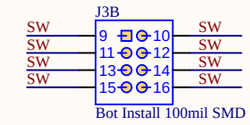
Signal Inputs



dead-time and buffers

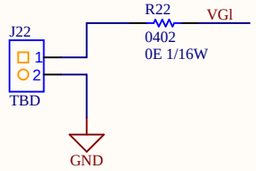
Gate Driver

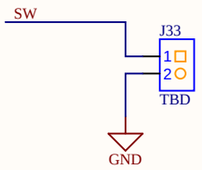
Power Stage



SW Output

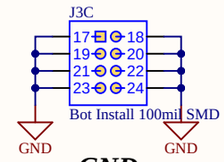
Sync Buck Output



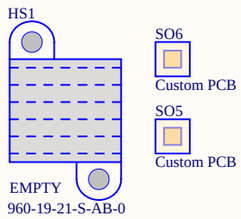


Lower Gate

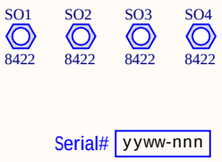
Switch-node

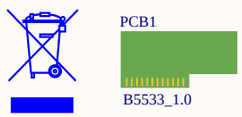


GND



Heatspreader





For evaluation only;
not FCC approved for resale

Title: Main Schematic			© EPC 2025
Design #: EPC90168		PCB #: B5533	
Revision 1.0		Revision: 1.0	
Date: 7/15/2026		Sheet 1 of 5	
File: D1123_B5533_Rev1_2.SCHDOC			

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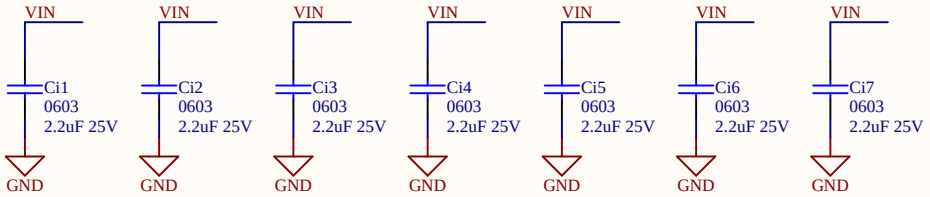
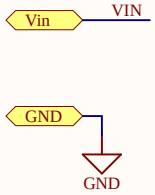
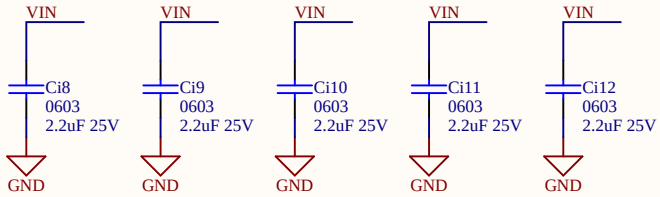
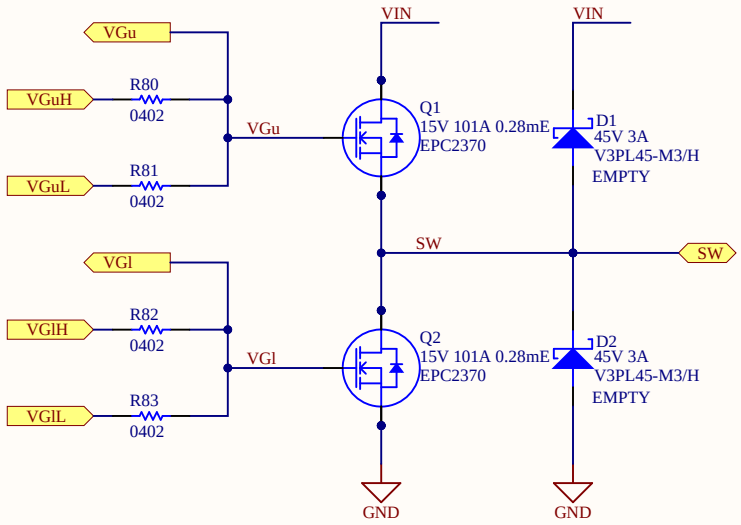


HF loop Capacitors







Power Stage ***Optional Diodes***

Title:	HB Sub Schematic - Phase Leg		© EPC 2025
Design #:	D1123 Phase Leg		
Revision	1.0	P/N#:	EPC2370
Date:	7/15/2026	Sheet	2 of 5
File:	D1123_B5533_Rev1_2_PhaseLeg.SCHDOC		

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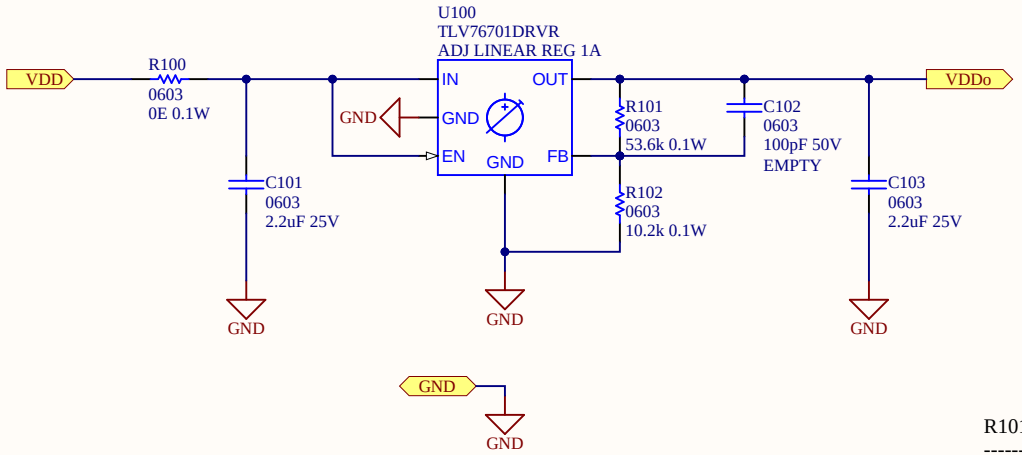

R101	R102	VDDo
53.6k	10.2k	5V
54.9k	10.2k	5.1V
56.2k	10.2k	5.2V
54.9k	9.76k	5.3V
56.2k	10.2k	5.4V
60k	10.2k	5.5V

Title: 16 V to 5 V, 1 A Linear Regulator

Design #: AP1092

Revision 1.0

Date: 7/15/2026 | Sheet 3 of 5

File: AP1092_Rev1_0.SCHDOC

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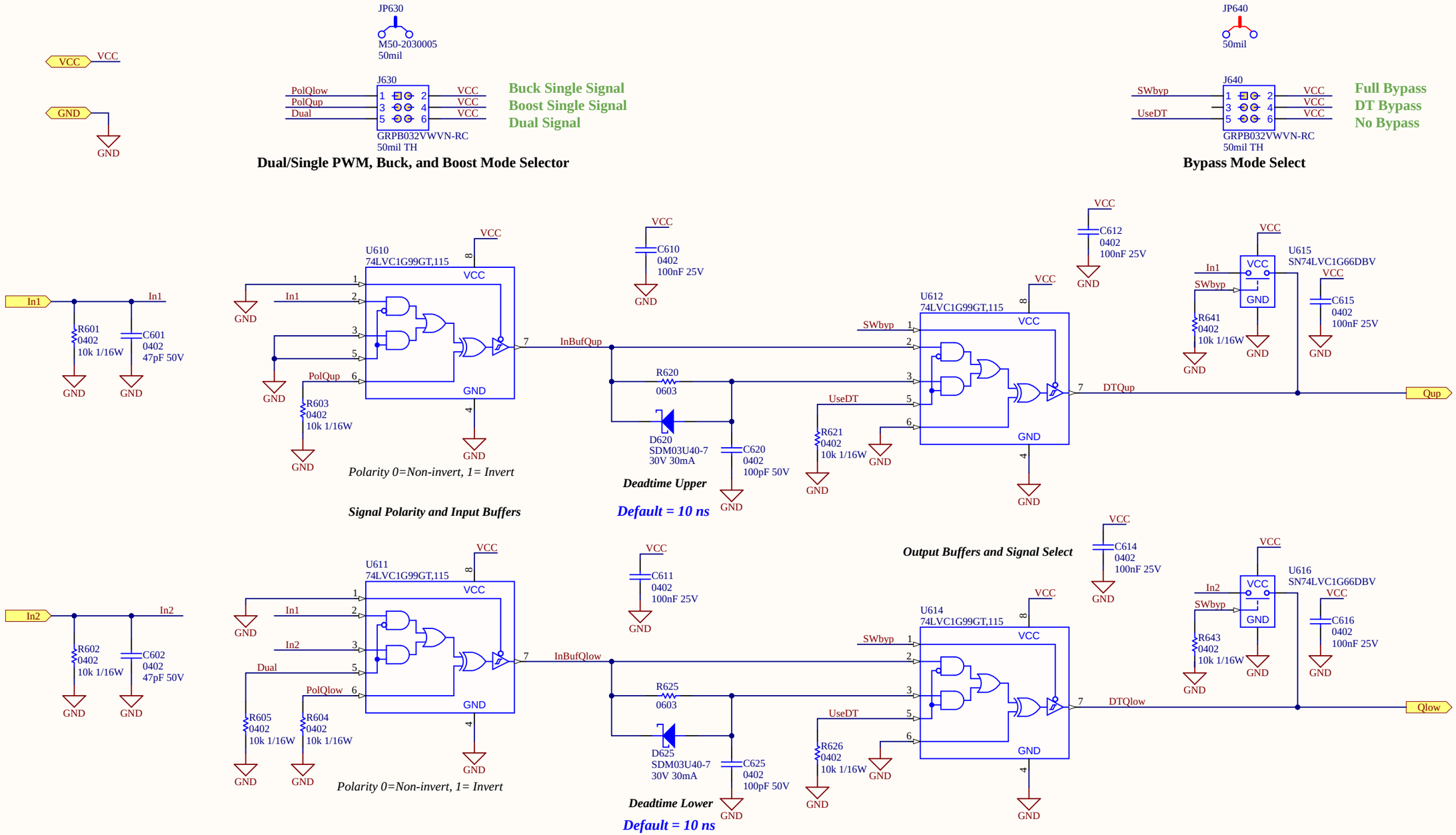

Title:	General Dead-time with Polarity Changer and Bypass
Design #:	AP1010
Revision	3.1
Date:	7/15/2026
Sheet	4 of 5
File:	AP1010_Rev3_2.SCHDOC

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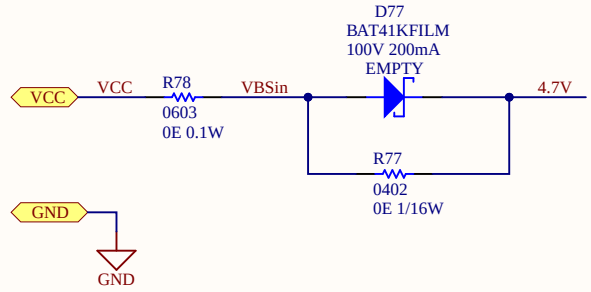
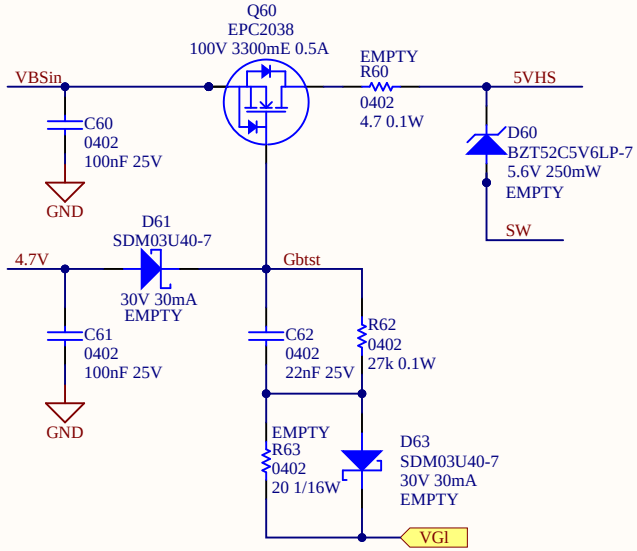
Sync Boot = Install R60, D60 and D77, remove R77

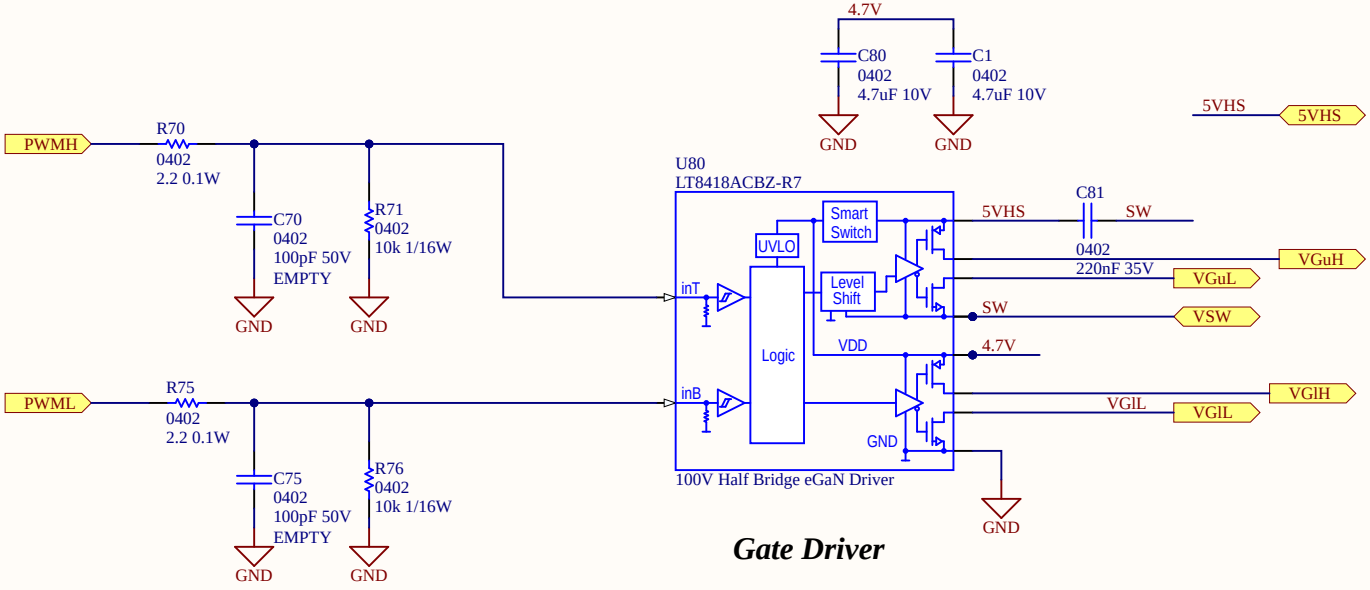
No Sync Boot = Install R77, remove R60, D60 and D77

Default = No Sync Boot





Synchronous Boostrap Power Supply



Gate Driver

Title:	100 V HB Gate Driver with Synchronous Bootstrap	© EPC 2025
Design #:	AP1091	Efficient Power Conversion 909 Pacific Coast Hwy. Ste 230 El Segundo, CA 90245 U.S.A. www.epc-co.com
Revision	1.0	
Date: 7/15/2026	Sheet 5 of 5	
File: AP1091_Rev1_0.SCHDOC		