Chasing the Speed of Light

As the level of automation increases in machines, detailed awareness of the surroundings becomes necessary. Time-of-flight based 3D imaging systems have become the eyes of machines. eGaN® technology has been the workhorse of laser drivers for these systems, enabling the resolution to make intelligent decisions.

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When you are chasing the speed of light, at 10s to 100s of amps, from 10s to 100s of volts, there is little room for parasitic capacitance and inductance. This article explains the detailed mechanisms for driving lasers, and why eGaN FETs and eToF™ ICs have been and will continue to be the best choice for these demanding applications. It should be noted that the concepts presented in this article can be applied to most power switching applications.

Fundamentally, the circuit for driving a pulsed laser for time-of-flight lidar is simple, as shown in Figure 1. While other circuits are possible, they need more and larger components and have higher cost. With optical power being related to laser current, the electrical objective is to achieve the required peak current in a time on the order of the speed of light relative to the required resolution. Considering light travels 0.3 m in 1 ns, inductance must be kept on the order of hundreds of pH in order to keep the driving voltage at a practical level, and the driving voltage must be applied in hundreds of ps.

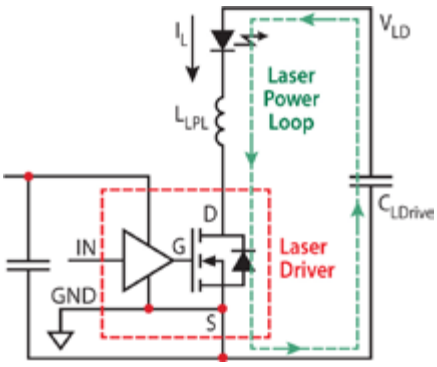


Figure 1: Basic laser driver circuit

Much has been written of techniques to reduce inductance to hundreds of pH using short, wide traces and inductance cancellation [1], [2], [3]. The focus is on the laser driver, which must apply the voltage to the power loop inductance fast enough to achieve the required peak current. In the sub nanosecond timeframe, at the currents required to achieve the distance and field of view needed by the system, the charging and discharging of the multiple capacitances, and their overlapping loops must be considered in detail as shown in Figure 2.

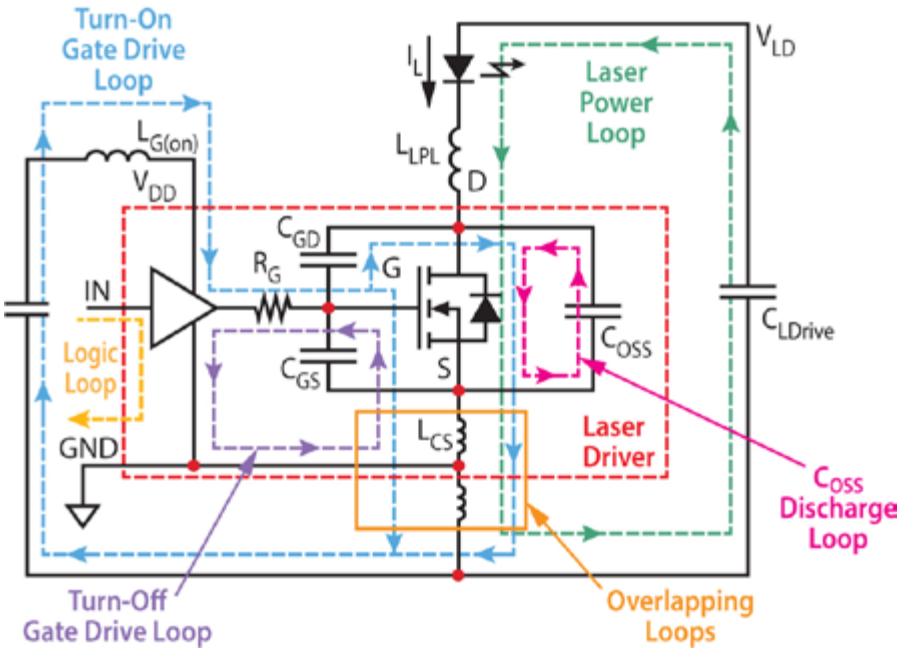


Figure 2: Detail of laser driver loops and stray elements

Figure 3 shows an approximation of key waveforms for a turn-on event for the circuit of Fig. 2. Turn-on starts with the logic input going high. After some propagation delay, the gate voltage starts to rise with C_{GS} charging through the various impedances of the turn-on gate drive loop as shown by Stage 1. Even with the gate voltage rising, there is negligible impact on the laser power loop until V_{GS} reaches a value where the output FET begins to conduct. With the extreme di/dt and dv/dt of a laser driver, the input loop must be decoupled from all other loops through layout and/or filter to prevent false triggering. It should be noted that that the return to the gate drive capacitor in the turn-on gate drive current loop comes from the power FET source and not the gate driver as shown in Figure 2. Figure 4 shows the transfer characteristics of the EPC2204 [4]. This curve defines the V_{GS} necessary to begin conduction as well as the V_{GS} necessary to drive required current. In this example, 1.75 V is necessary to begin conduction. This is where stage 2 of Figure 3 begins.

With the FET channel beginning to conduct current, C_{OSS} starts to discharge and V_{DS} begins to fall. Driven as a step pulse, V_{DS} must collapse rapidly to present a high voltage across the power loop inductance that drives the di/dt of the resonant circuit that determines the magnitude and duration of the pulse for the application. Since channel current, hence dv/dt, is controlled by the transfer characteristics curve, V_{GS} must

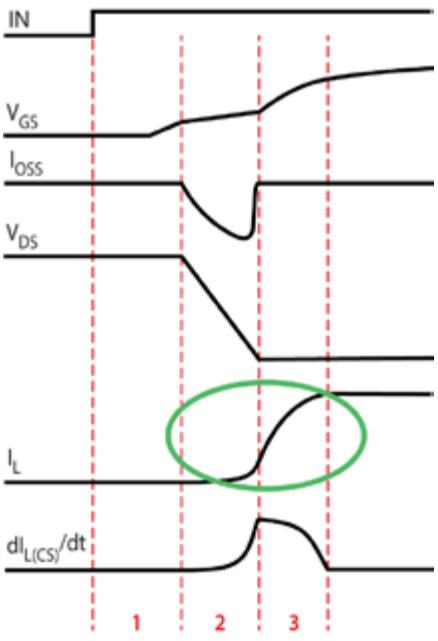


Figure 3: Theoretical waveforms, laser driver turn-on

continue to increase to accelerate C_{OSS} discharge. In this stage, discharging C_{GD} is added to the burden of the gate drive loop. As soon as V_{DS} begins to fall, laser current begins to rise. At this point, there is interaction between the gate drive and power loops. Inductance common to these loops, known as common source inductance (L_{CS}), carries the di/dt of the power loop resulting in a voltage drop that is subtracted from the gate drive potential, slowing the gate capacitance charging. It is critical to separate these loops as much as possible, as even common source inductance values of 100 pH can result in large increases in turn-on time

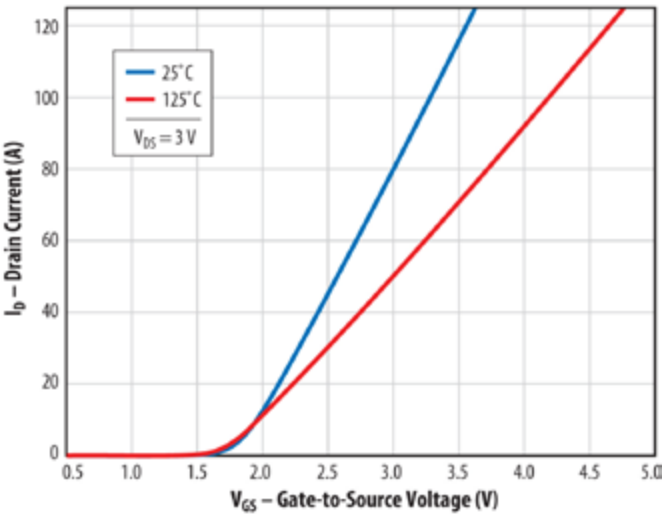


Figure 4: Transfer Characteristics of EPC2204

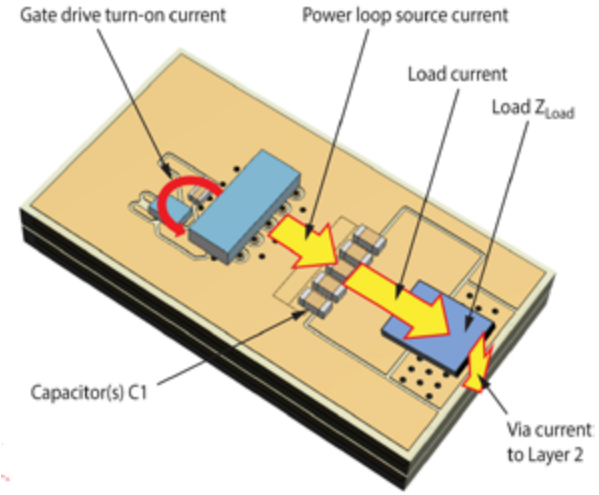
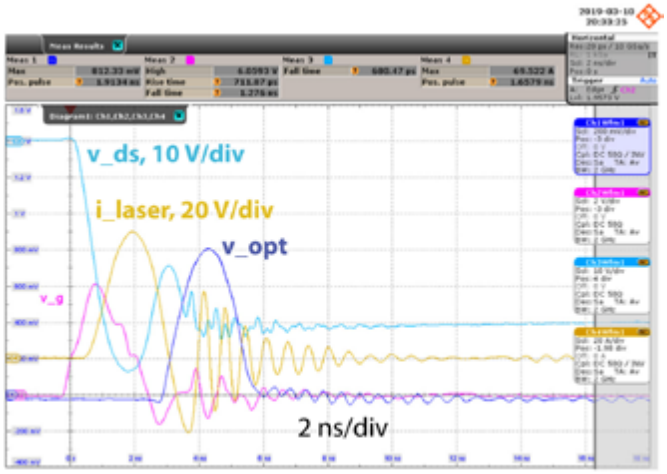


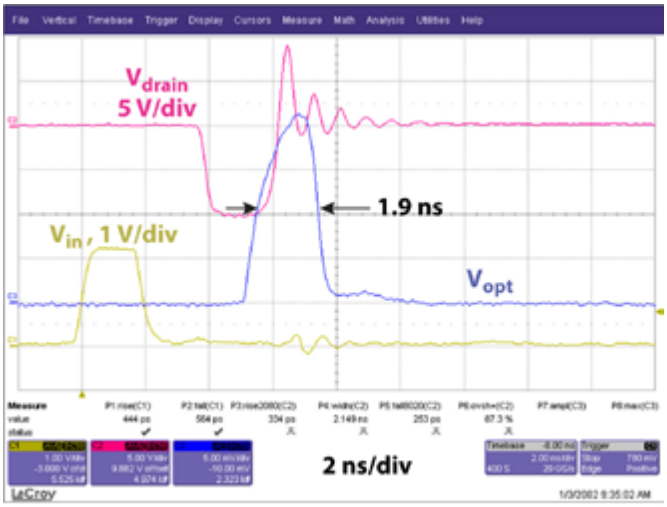
Figure 5: Top board layer layout

Stage 2 is completed when C_{OSS} is discharged and V_{DS} has collapsed completely. At this point, full laser drive voltage is applied across the power loop inductance resulting maximum di/dt. Minimizing L_{CS} is very important because with 25 pH at 100 A/ns gives a 2.5 V drop. For a 5 V gate drive, this leaves 2.5 V of gate drive potential, which will limit gate current and switching speed. Achieving a low L_{CS} requires a low inductance package and careful attention to layout where the two loops that contribute to common source inductance need to be separated right at the package, as shown in Figure 5. In addition wire bonds and clips in the source add inductance and thus not suitable packaging options.

Stage 3 requires the current in the laser to reach the required value and thus V_{GS} must continue to rise past the voltage necessary to achieve full current based on the transfer characteristics curve. Taking EPC2204 as an example, 80 A requires V_{GS} > 3 Vat 25 °C and > 3.7 at 125 °C, stressing that the voltage induced by the power di/dt over L_{CS} will be subtracted from V_{GS}. Stage 3 is completed when the laser achieves the full required current, typically at the peak of a resonant pulse in the case of a resonant laser drive topology where the laser drive capacitance and the power loop inductance form an LC tank. In this case, the LC determines the pulse width, and together with the laser drive voltage, controls the peak current and optical power [5]. In the case of an active turn-off topology, full current is reached when the laser voltage plus the laser driver voltage equals the laser drive source voltage. Figure 6a shows example waveforms of a resonant discharge laser driver with the yellow trace being laser current and dark blue trace representing optical power. Figure 6b shows example waveforms of an active turn-off laser driver with the blue trace representing optical power and the red trace being drain voltage.



(a)



(b)

Figure 6: Laser driver waveforms of a. resonant discharge topology and b. active turn-off topology

For turn-off, in the resonant case, the laser driver is turned off close to or at zero current and must be low enough that the drain capacitance is mostly discharged but does not ring. Active turn-off manifests as a classic ZVS turn-off, with the laser driver disrupting the power loop, diverting current of the power loop into the C_{OSS}. Its rise in voltage across the power loop inductance drives the turn-off of current. A similar loop analysis to turn-on must be made for proper design.

Laser driver selection

Laser driver selection starts with determining the best semiconductor technology and packaging for extreme combination of speed and power. Packaging must have low inductance, but more critically, low common source inductance. Wafer level packaging provides the minimum inductance possible. Integrating the gate drive with the power FET, such as EPC's EPC21701 eToF™ laser driver, shown in Figure 7, reduces the number of package connections and board traces, reducing inductance and greatly reducing common source inductance. It also matches the gate driver to the power FET, which can enhance performance and reduce cost. It also reduces the size of the laser driver circuitry, which is especially important for multi-channel lidar systems.

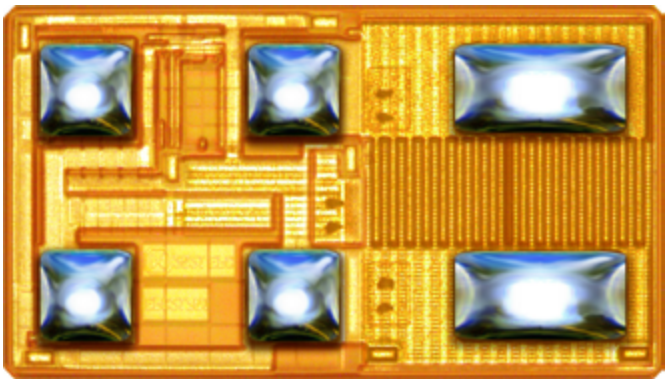


Figure 7: Bump side image of 1.7 mm x 1 mm EPC21701

The semiconductor technology chosen must have the lowest capacitance per peak current for the required voltage. eGaN® technology has Q_{GS} and Q_{GD} an order of magnitude lower than comparable silicon MOSFETs, and about half the Q_{OSS}, which together with the low resistance of the metal gate, ensures the fastest possible switching speed [6]. Once the technology is selected, peak current must be correctly sized. A device that is too small does not provide sufficient output power; a device too large results in a slower driver due to excess capacitance (and higher cost). The transfer characteristics curve, over the necessary temperature range, drives the selection.

Conclusions

Fundamentally, eGaN technology has vastly lower capacitance when compared with silicon MOSFET alternatives. Integration of the gate driver and chip-scale packaging greatly reduces inductance and allows one to take full advantages of their inherently high speed. Along with a low inductance layout, one can increase power and reduce pulse width of the optical pulse resulting in increased resolution, range, and field of view while reducing power consumption in ToF imaging systems, where the metric is the speed of light.

References

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