EPC2111 – Enhancement-Mode GaN Power Transistor Half-Bridge

V_{DS} , 30 V

$R_{DS(on)}$, 19 mΩ (Q1), 8 mΩ (Q2)

I_D , 16 A (Q1), 16 A (Q2)

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised June 19, 2020

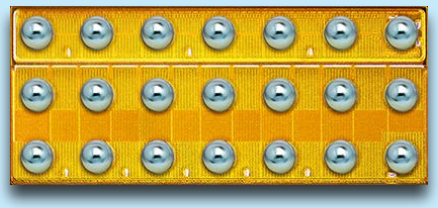
Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

Maximum Ratings				
DEVICE	**PARAMETER**		**VALUE**	**UNIT**
Q1	V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	36	
	I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 15°C/W)	16	A
		Pulsed (25°C, T_{PULSE} = 300 µs)	50	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	T_J	Operating Temperature	–40 to 150	°C
	T_{STG}	Storage Temperature	–40 to 150	
Q2	V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	36	
	I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 36°C/W)	16	A
		Pulsed (25°C, T_{PULSE} = 300 µs)	140	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	-4	
	T_J	Operating Temperature	–40 to 150	°C
	T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	6.6	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	58	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



Die size: 3.5 x 1.5 mm

EPC2111 eGaN® ICs are supplied only in passivated die form with solder bumps.

Applications

- High frequency DC-DC
- Point-of-load (POL) converters

Benefits

- High frequency operation (up to 10 MHz)
- Low inductance package
- High density footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2111

Static Characteristics							
DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.25 mA	30			V
	I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 24 V		0.002	0.15	mA
	I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.004	2	mA
		Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.002	0.15	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 2 mA	0.8	1.4	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 15 A		14	19	mΩ
	V_{SD}	Source-Drain Forward Voltage	V_{GS} = 0 V, I_S = 0.5 A		1.8		V
Q2	BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.4 mA	30			V
	I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 24 V		0.005	0.3	mA
	I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	4.5	mA
		Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.005	0.3	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 5 mA	0.8	1.4	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 15 A		6	8	mΩ
	V_{SD}	Source-Drain Forward Voltage	V_{GS} = 0 V, I_S = 0.5 A		1.8		V

Dynamic Characteristics							
DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V		190	230	pF
	C_{RSS}	Reverse Transfer Capacitance			8		
	C_{OSS}	Output Capacitance			170	255	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 15 V		204		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			217		
	R_G	Gate Resistance			0.5		
	Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 15 V, I_D = 15 A		1.7	2.2	nC
	Q_{GS}	Gate-to-Source Charge	V_{DS} = 15 V, I_D = 15 A		0.6		
	Q_{GD}	Gate-to-Drain Charge			0.3		
	$Q_{G(TH)}$	Gate Charge at Threshold			0.4		
	Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 15 V		3.3	5	
	Q_{RR}	Source-Drain Recovery Charge			0		
Q2	C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 15 V		495	595	pF
	C_{RSS}	Reverse Transfer Capacitance			21		
	C_{OSS}	Output Capacitance			490	735	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V , V_{DS} = 0 to 15 V		590		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			637		
	R_G	Gate Resistance			0.4		
	Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 15 V, I_D = 15 A		4.5	5.8	nC
	Q_{GS}	Gate-to-Source Charge	V_{DS} = 15 V, I_D = 15 A		1.4		
	Q_{GD}	Gate-to-Drain Charge			0.8		
	$Q_{G(TH)}$	Gate Charge at Threshold			1		
	Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 15 V		9.6	15	
	Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1a (Q1): Typical Output Characteristics at 25°C

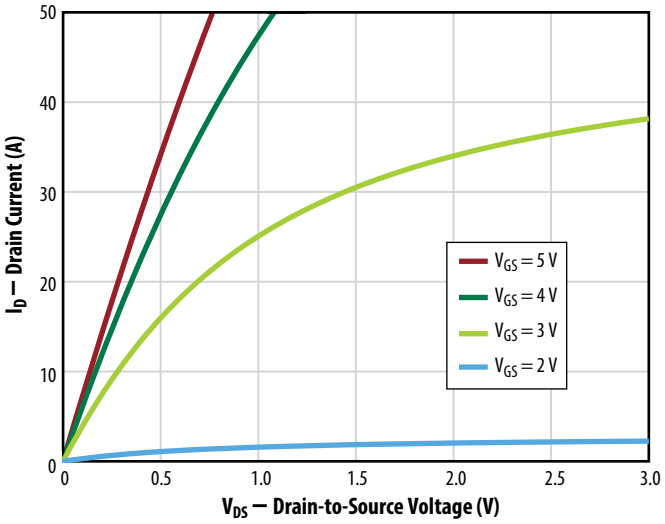


Figure 1b (Q2): Typical Output Characteristics at 25°C

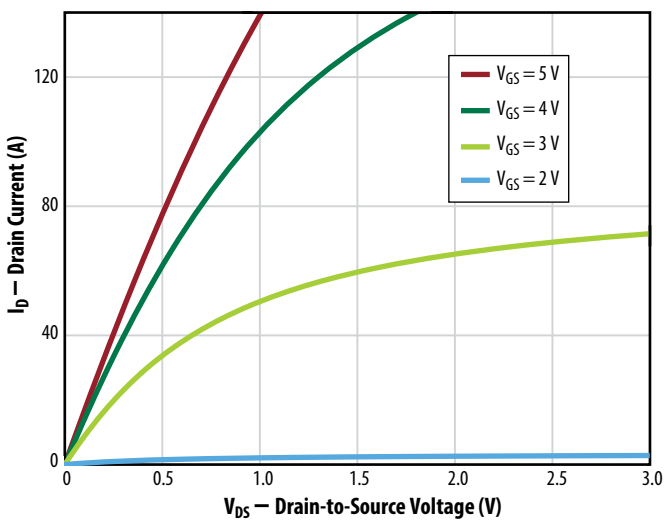


Figure 2a (Q1): Typical Transfer Characteristics

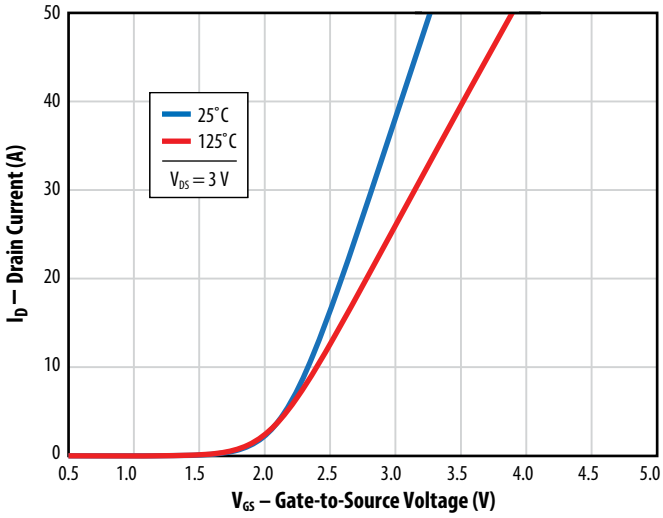


Figure 2b (Q2): Typical Transfer Characteristics

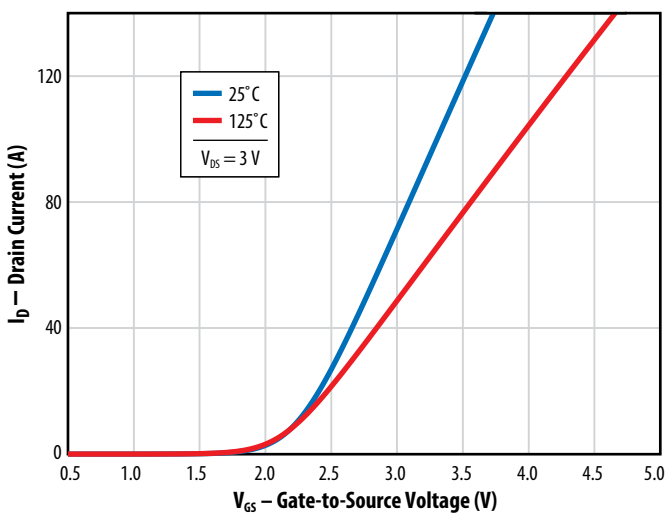


Figure 3a (Q1): Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

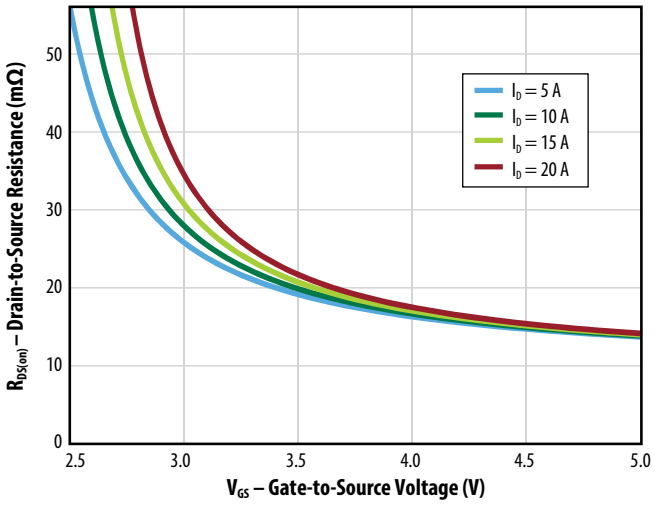


Figure 3b (Q2): Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

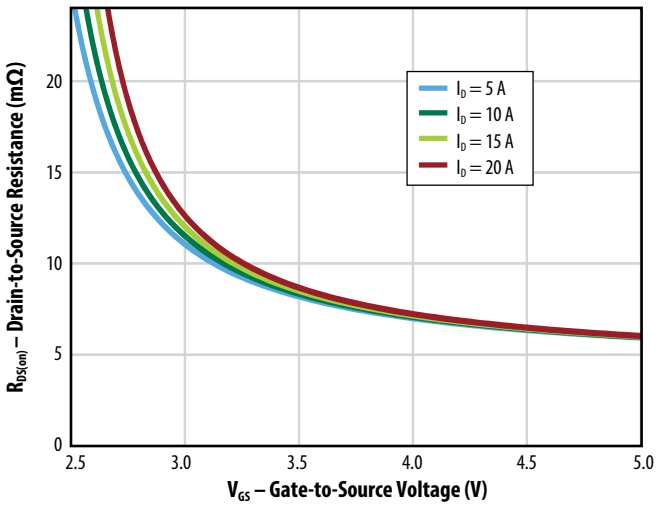


Figure 4a (Q1): Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

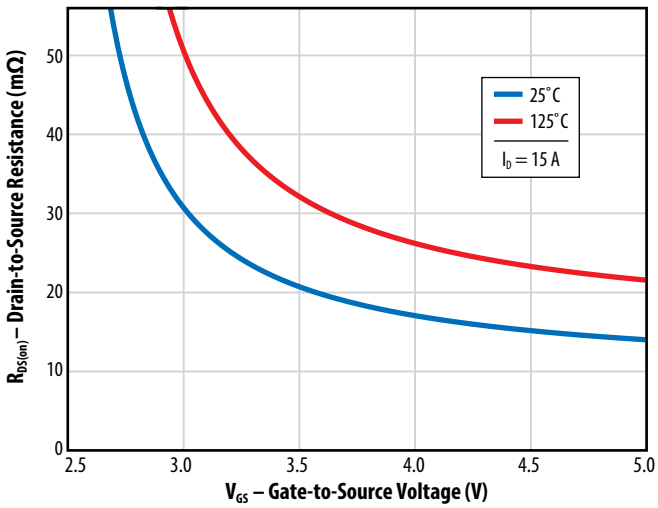


Figure 4b (Q2): Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

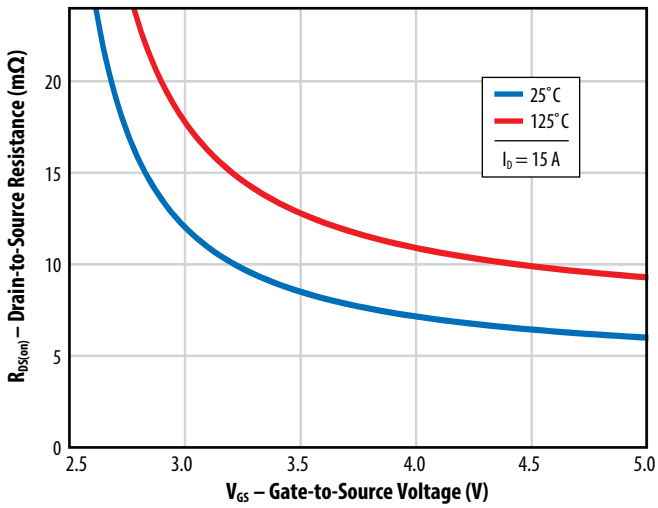


Figure 5a (Q1): Typical Capacitance (Linear Scale)

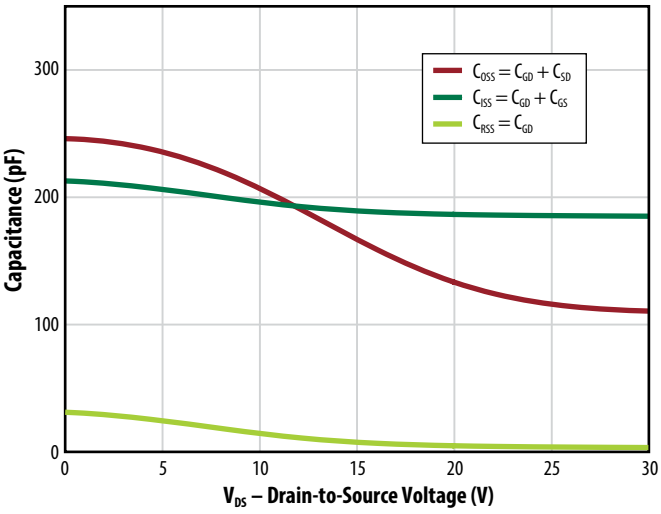


Figure 5b (Q2): Typical Capacitance (Linear Scale)

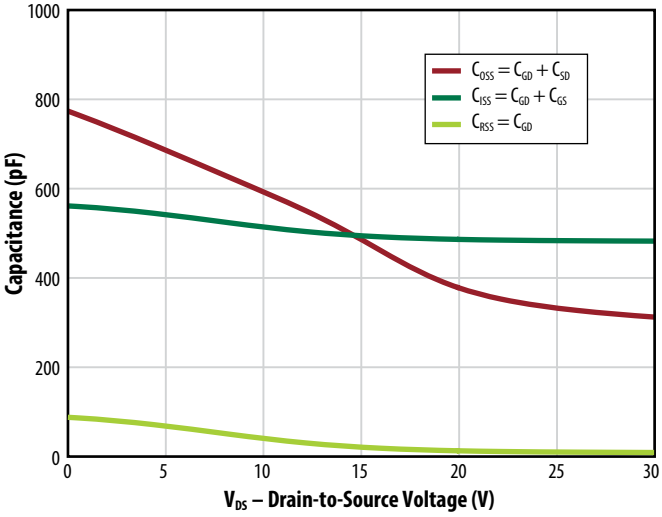


Figure 6a (Q1): Typical Output Charge and C_{OSS} Stored Energy

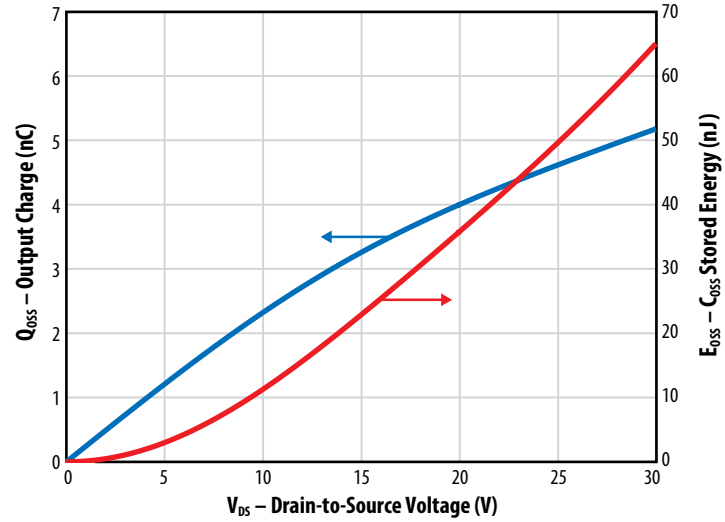


Figure 6b (Q2): Typical Output Charge and C_{OSS} Stored Energy

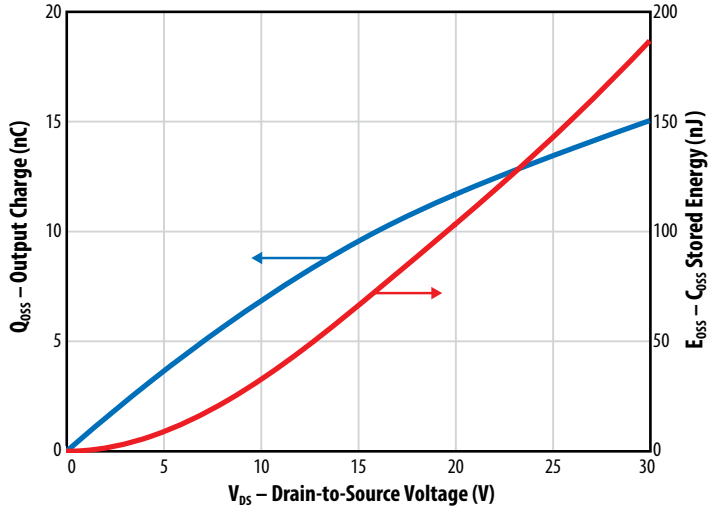


Figure 7a (Q1): Typical Gate Charge

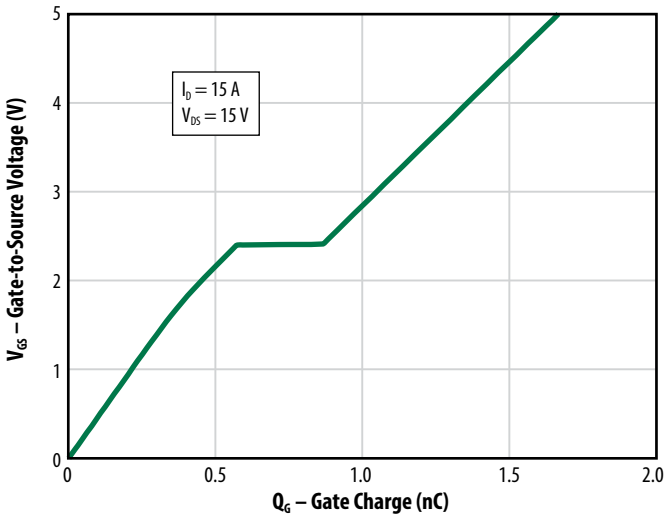


Figure 7b (Q2): Typical Gate Charge

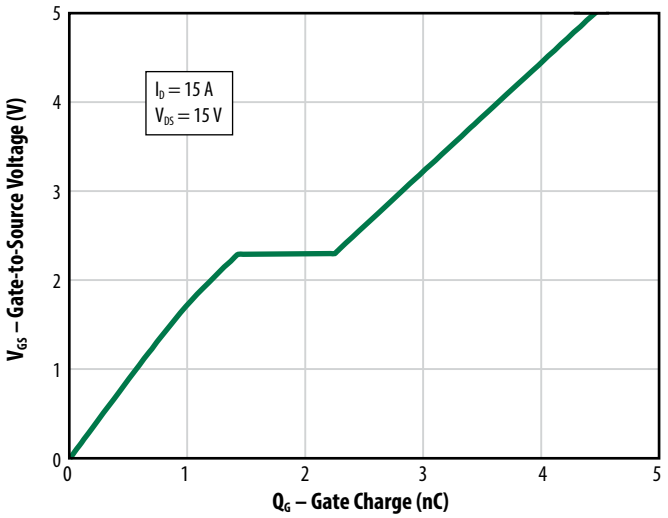
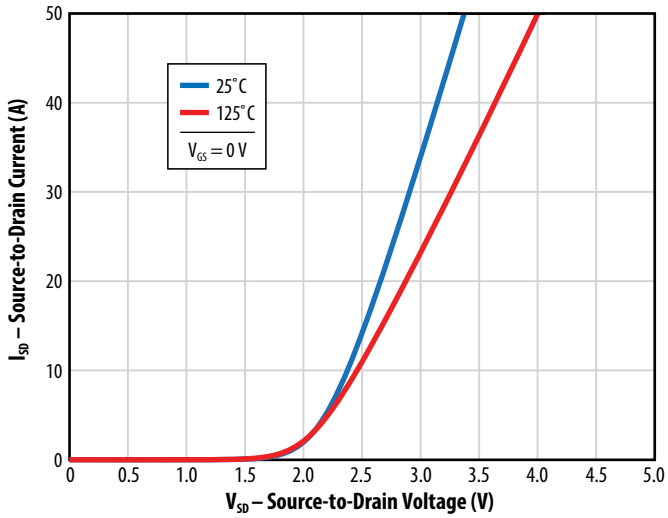
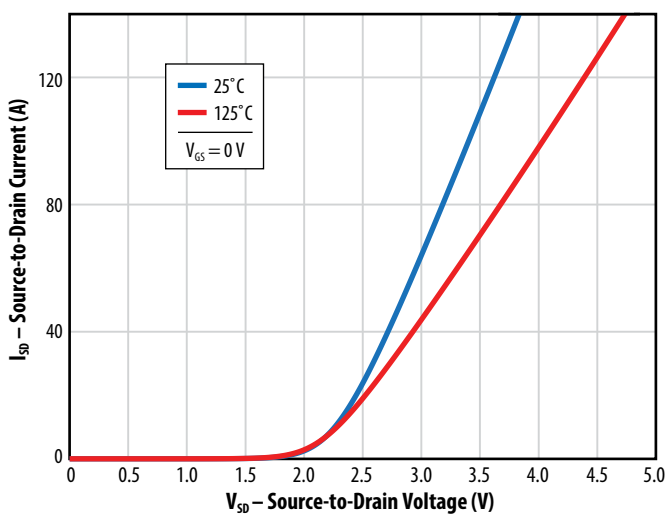


Figure 8a (Q1): Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8b (Q2): Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 9a (Q1): Typical Normalized On-State Resistance vs. Temperature

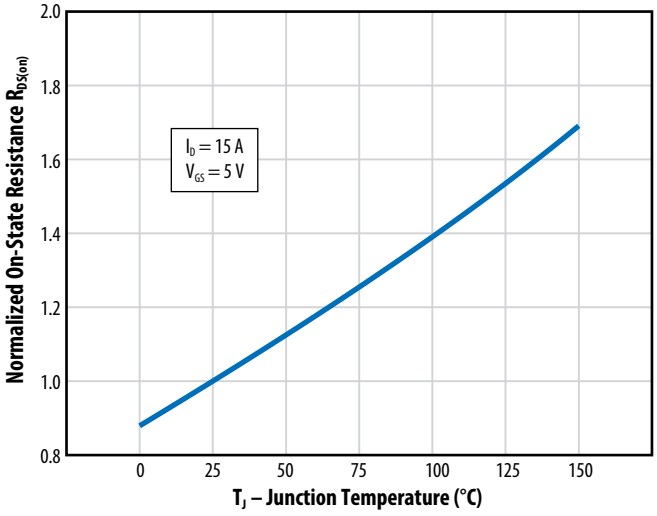


Figure 9b (Q2): Typical Normalized On-State Resistance vs. Temperature

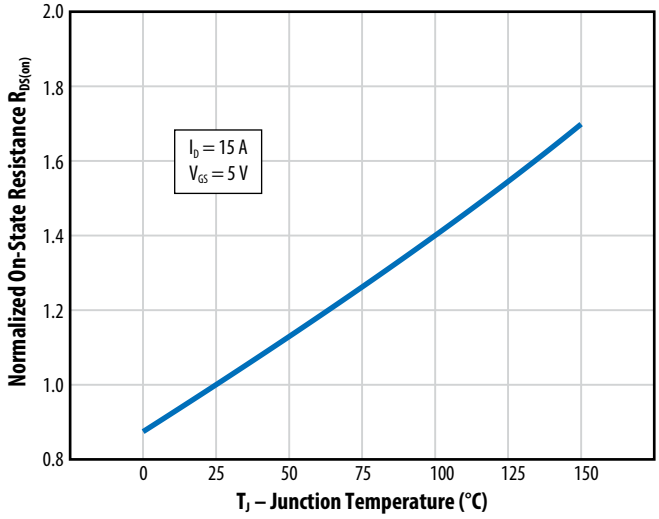


Figure 10a (Q1):
Typical Normalized Threshold Voltage vs. Temperature

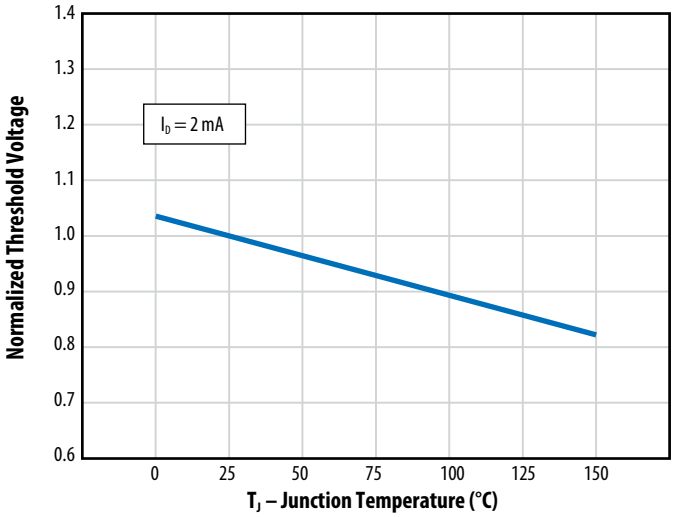


Figure 10b (Q2):
Typical Normalized Threshold Voltage vs. Temperature

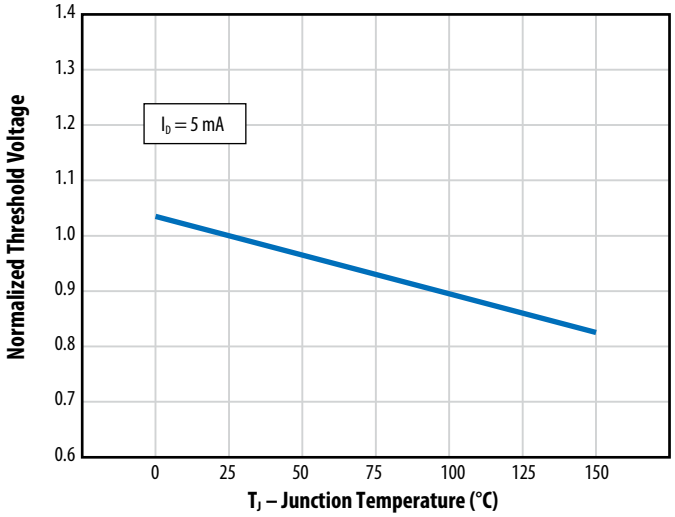


Figure 11a (Q1): Safe Operating Area

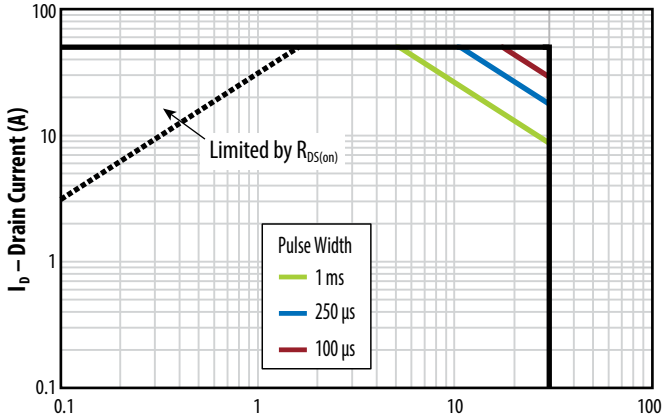
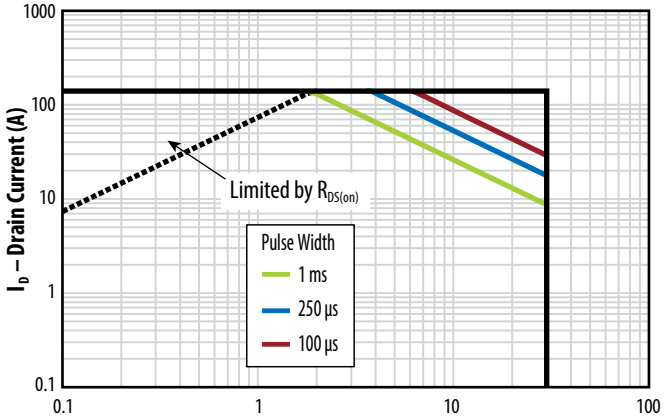


Figure 11b (Q2): Safe Operating Area



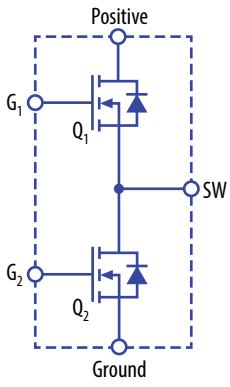


Figure 12
Typical Application Circuit

Figure 13a
Typical Transient Thermal Response Curves

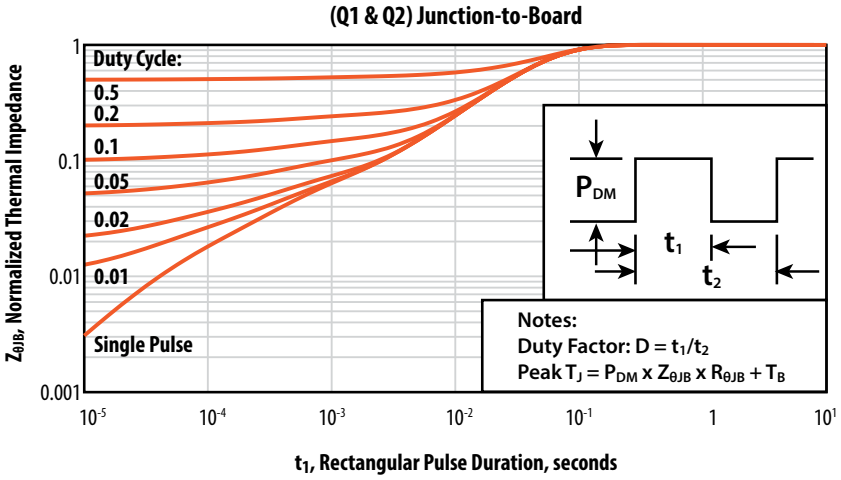
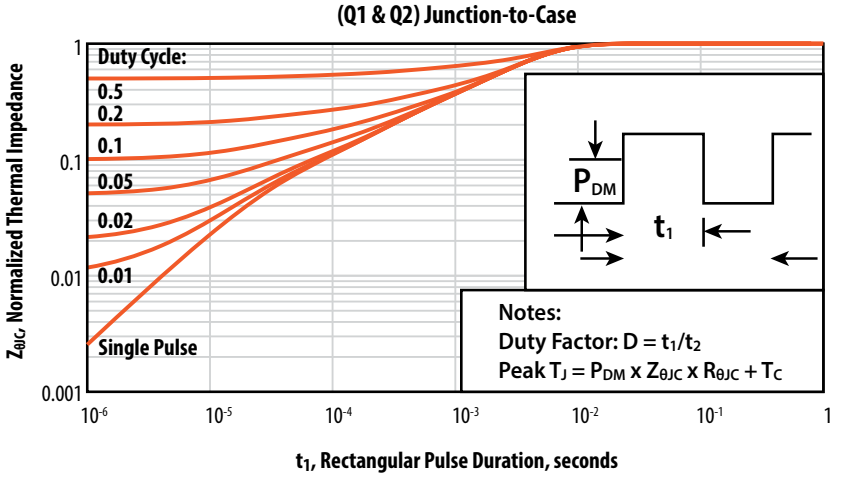
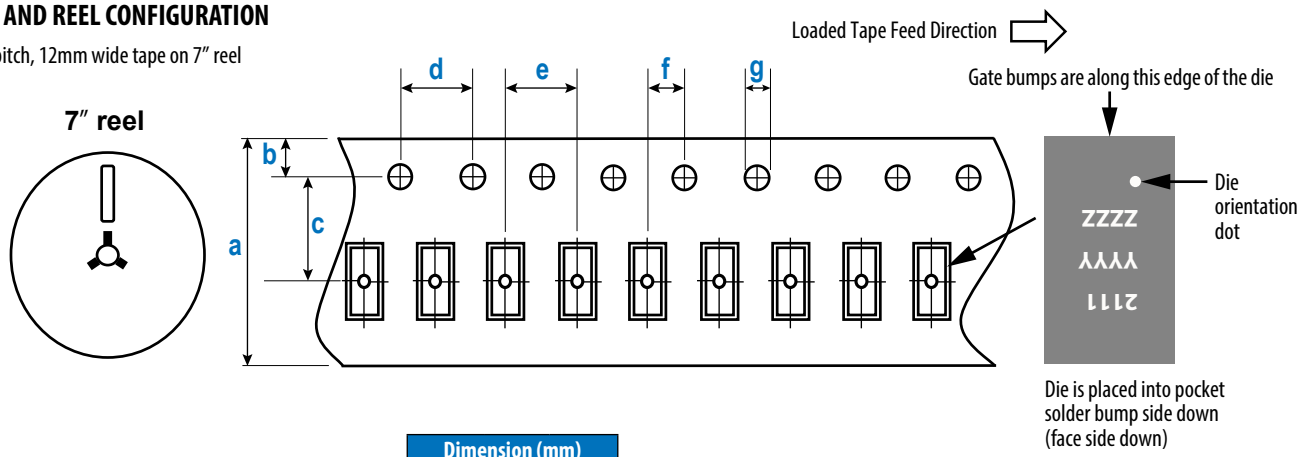


Figure 13b
Typical Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

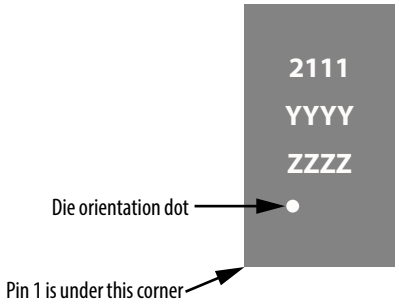


	Dimension (mm)		
EPC2111 (Note 1)	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

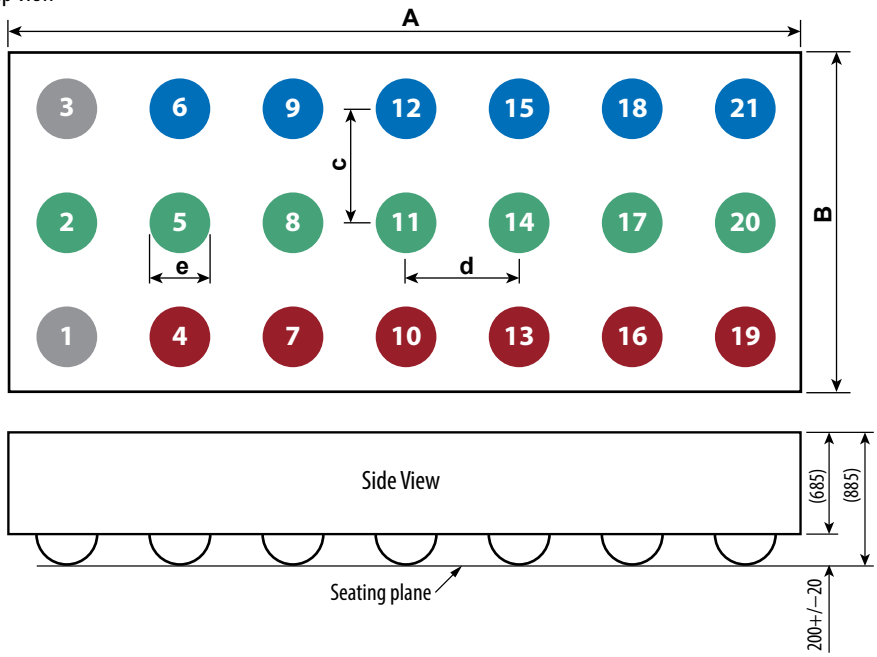
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2111	2111	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

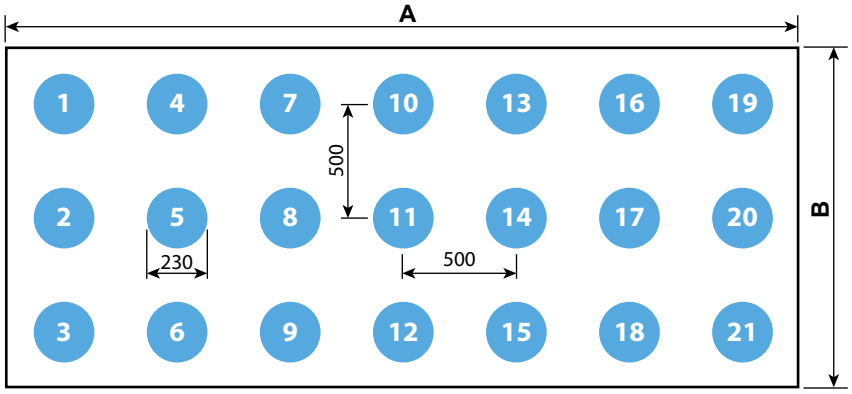


DIM	MIN	Nominal	MAX
A	3470	3500	3530
B	1470	1500	1530
c	500	500	500
d	500	500	500
e	238	264	290

Pad 1 is G1; Pad 3 is G2;
Pads 4, 7, 10, 13, 16, 19 are V_{IN};
Pads 2, 5, 8, 11, 14, 17, 20 are SN;
Pads 6, 9, 12, 15, 18, 21 are GND

RECOMMENDED LAND PATTERN

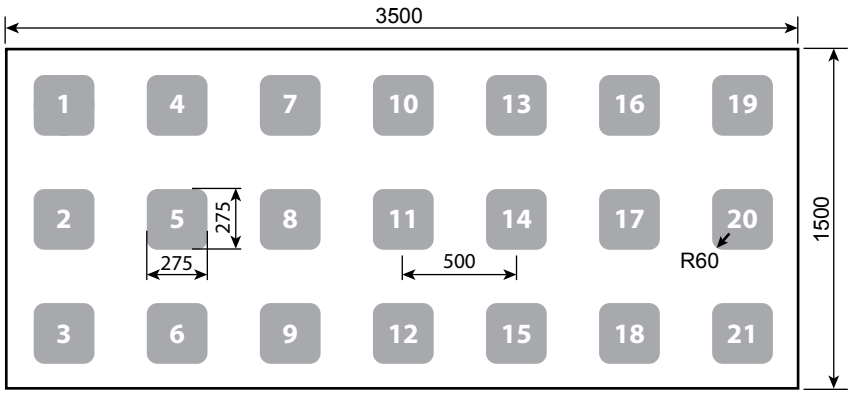
(measurements in µm)



The land pattern is solder mask defined.

RECOMMENDED STENCIL DRAWING

(measurements in µm)



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: https://epc-co.com/epc/design-support